NKK

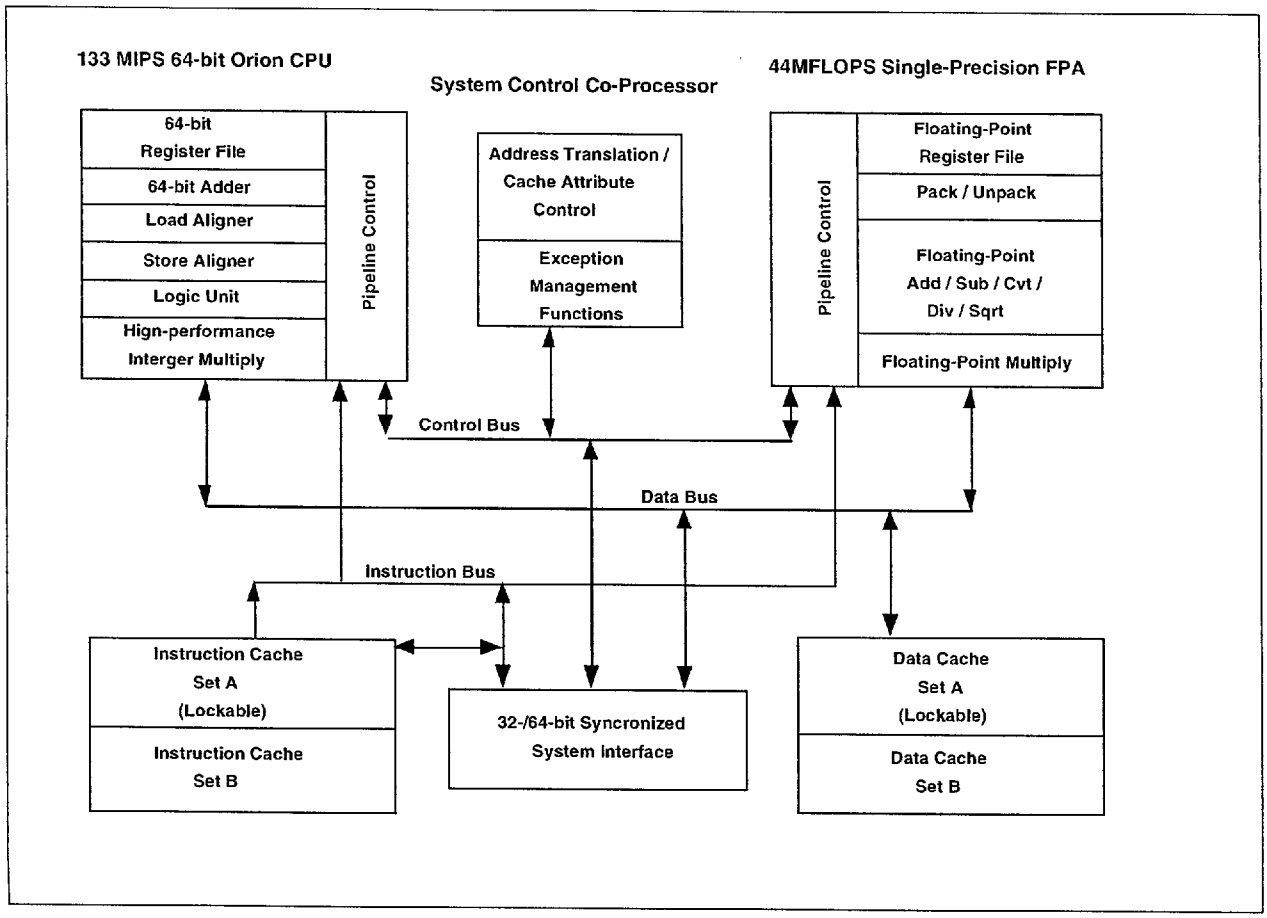
64 bit RISC Embedded Controller NR4650G

PRELIMINARY

■ FEATURES

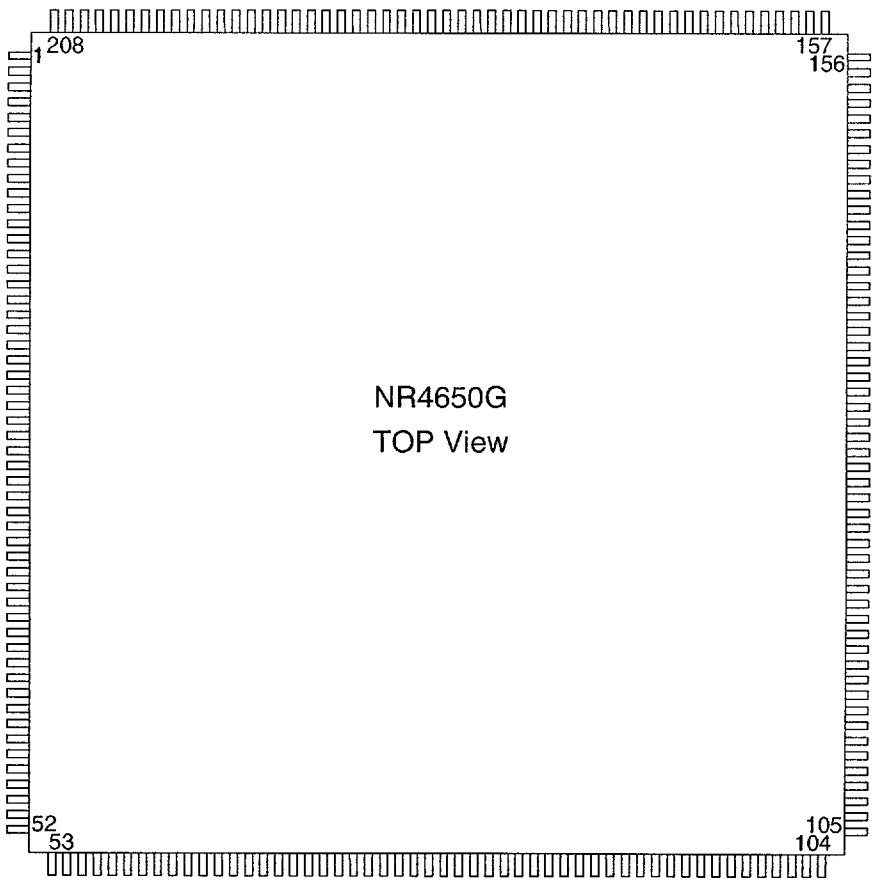
- High-performance embedded 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit registers
  - 100MHz, 133MHz operation frequency
- High-performance microprocessor
  - 133MIPS at 133MHz
  - 66.7M Mul-Add/second at 133MHz
  - 44M FLOPS/sec at 133MHz
  - >300,000 dhrystone/sec capability at 133MHz (175 dhrystone MIPS)
  - Separate 8KB Instruction and Data caches
- Low-power operation
  - Less than 3W peak internal power at 100MHz
  - Active power management powers-down inactive units
  - Standby mode power consumption <200mW
- Large, efficient on-chip caches
  - Separate 8KB Instruction and Data caches
  - Over 1500MB/sec bandwidth from internal caches
  - 2-way set associative
  - Write-back and write-through support
  - Cache locking to facilitate deterministic response
- Bus compatible with NR4600/ORION family
  - System interfaces to 67MHz, provides bandwidth up to 533MB/sec
  - Direct interface to 32-bit or 64-bit wide systems
- 5V Tolerant I/O
  - 5V Input Enable
  - High Level 2.4V Output
- Improved real-time support
  - Fast interrupt decode
  - Optional cache locking

■ Block Diagram



■ PHYSICAL SPECIFICATIONS

208-PIN PQFP



■ NR4650G PQFP package pin-out

Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	NC	53	NC	105	NC	157	NC
2	NC	54	NC	106	NC	158	NC
3	NC	55	NC	107	NC	159	SysAD59
4	NC	56	NC	108	NC	160	$\overline{\text{ColdReset}}$
5	NC	57	SysCmd2	109	NC	161	SysAD28
6	NC	58	SysAD36	110	NC	162	VCC
7	NC	59	SysAD4	111	NC	163	VSS
8	NC	60	SysCmd1	112	NC	164	SysAD60
9	NC	61	VSS	113	NC	165	$\overline{\text{Reset}}$
10	SysAD11	62	VCC	114	SysAD52	166	SysAD29
11	VSS	63	SysAD35	115	$\overline{\text{ExtRqst}}$	167	SysAD61
12	VCC	64	SysAD3	116	VCC	168	SysAD30
13	SysCmd8	65	SysCmd0	117	VSS	169	VCC
14	SysAD42	66	SysAD34	118	SysAD21	170	VSS
15	SysAD10	67	VSS	119	SysAD53	171	SysAD62
16	SysCmd7	68	VCC	120	$\overline{\text{RdRdy}}$	172	SysAD31
17	VSS	69	SysAD2	121	Modein	173	SysAD63
18	VCC	70	$\overline{\text{Int5}}$	122	SysAD22	174	VCC
19	SysAD41	71	SysAD33	123	SysAD54	175	VSS
20	SysAD9	72	SysAD1	124	VCC	176	VccOK
21	SysCmd6	73	VSS	125	VSS	177	SysADC3
22	SysAD40	74	VCC	126	$\overline{\text{Release}}$	178	SysADC7
23	VSS	75	$\overline{\text{Int4}}$	127	SysAD23	179	NC
24	VCC	76	SysAD32	128	SysAD55	180	NC
25	SysAD8	77	SysAD0	129	$\overline{\text{NMI}}$	181	NC
26	SysCmd5	78	$\overline{\text{Int3}}$	130	VCC	182	NC
27	SysADC4	79	VSS	131	VSS	183	NC
28	SysADC0	80	VCC	132	SysADC2	184	NC
29	VSS	81	$\overline{\text{Int2}}$	133	SysADC6	185	VssP
30	VCC	82	SysAD16	134	SysAD24	186	VccP
31	SysCmd4	83	SysAD48	135	VCC	187	MasterClock
32	SysAD39	84	$\overline{\text{Int1}}$	136	VSS	188	VCC
33	SysAD7	85	VSS	137	SysAD56	189	VSS
34	SysCmd3	86	VCC	138	SysAD25	190	SysADC5
35	VSS	87	SysAD17	139	SysAD57	191	SysADC1
36	VCC	88	SysAD49	140	VCC	192	VCC
37	SysAD38	89	$\overline{\text{Int0}}$	141	VSS	193	VSS
38	SysAD6	90	SysAD18	142	IOOut	194	SysAD47
39	ModeClock	91	VSS	143	SysAD26	195	SysAD15
40	$\overline{\text{WrRdy}}$	92	VCC	144	SysAD58	196	SysAD46
41	SysAD37	93	SyaAD50	145	IOIn	197	VCC
42	SysAD5	94	$\overline{\text{ValidIn}}$	146	VCC	198	VSS
43	VSS	95	SysAD19	147	VSS	199	SysAD14
44	VCC	96	SysAD51	148	SysAD27	200	SysAD45
45	NC	97	VSS	149	NC	201	SysAD13
46	NC	98	VCC	150	NC	202	SysAD44
47	NC	99	$\overline{\text{ValidOut}}$	151	NC	203	VSS
48	NC	100	SysAD20	152	NC	204	VCC
49	NC	101	NC	153	NC	205	SysAD12
50	NC	102	NC	154	NC	206	SysCmdP
51	NC	103	NC	155	NC	207	SysAD43
52	NC	104	NC	156	NC	208	NC

■ PIN DESCRIPTION

Pins marked with one asterisk are active when low.

Pin Name	I/O	Description
System Interface:		
$\overline{\text{ExtRqst}}$	I	External request: Signals that the system interface needs to submit an external request.
$\overline{\text{Release}}$	O	Release interface: Signals that the processor is releasing the system interface to slave state.
$\overline{\text{RdRdy}}$	I	Read Ready: Signals that an external agent can now accept a processor read.
$\overline{\text{WrRdy}}$	I	Write Ready: Signals taht an external agent can now accept a processor write request.
$\overline{\text{ValidIn}}$	I	Valid input: Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{\text{ValidOut}}$	O	Valid output: Signals that the processor is now driving a valid sddress or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	I/O	System address/data bus: A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	I/O	System address/data check bus: An 8 bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	I/O	System command/data identifier bus: A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	I/O	System command/data identifier bus parity (Reserved): For the NR4650G this signal is unused on input and zero on output.
Clock/control Interface:		
MasterClock	I	Master clock: Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization.
VccP	I	Quiet Vcc for PLL: Quiet Vcc for the intrnal phase locked loop.
VssP	I	Quiet Vss for PLL: Quiet Vss for the internal phase locked loop.
Interrupt Interface:		
$\overline{\text{Int}}$(5:0)	I	Interrupt: Six gengeral processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
$\overline{\text{NMI}}$	I	Non-maskable interrupt: Non-maskable interrupt, ORed with bit 6 of the interrupt register.
Initiallization Interface:		
VccOK	I	Vcc is ok: When asserted, this signal indicates to the NR4650L that the 3.3V power supply has been above 3.0V for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the reading of the boot-time mode control serial stream.
$\overline{\text{ColdReset}}$	I	Cold reset: This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with MasterClock.
$\overline{\text{Reset}}$	I	Reset: This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterClock.
ModeClock	O	Boot mode clock: Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
Modein	I	Boot mode data in: Serial boot-mode data input.

DESCRIPTION:

The NR4650G is a low-cost member of the NR4600 (ORION) family, targeted to a variety of performance embedded applications. The NR4650G continues the ORION tradition of high-performance through high-speed pipelines, high-bandwidth caches and bus interface, and 64-bit architecture. The NR4650G reduces the cost of this performance relative to the NR4600, by removing functional units that are frequently unneeded for many embedded applications, such as double-precision floating point arithmetic and a TLB.

The NR4650G supports a wide variety of embedded processor-based applications, such as games systems, multimedia functions, internetworking equipment, and printing systems. Upwardly software-compatible with the NR4600 family, the NR4650G will serve in many of the same applications, but, in addition supports other applications such as those requiring integer DSP functions.

The NR4650G brings ORION performance levels to lower cost systems. ORION performance is preserved by retaining large on-chip caches that are 2-way set associative, a high-speed pipeline, high-bandwidth, 64-bit execution, and facilities such as early restart for data cache misses.

The NR4650G provides complete upward applications software compatibility with the NR3000 family of microprocessors as well as the NR4600 family of microprocessors except double-precision floating point arithmetic. An array of development tools facilitates the rapid development of NR4650G-based systems, enabling a wide variety of customers to take advantage of the high-performance capabilities of the processor while maintaining short time to market goals.

The 64-bit computing capability of the NR4650G enables a wide variety of capabilities previously limited by the lower bandwidth and bit-manipulation rates inherent in 32-bit architectures. For example, the NR4650G can perform loads and stores from cached memory at the rates of 8-bytes every clock cycle, doubling the bandwidth of an equivalent 32-bit processor. This capability, coupled with the high clock rate for the NR4650G pipeline, enables new levels of performance to be obtained from embedded systems.

This data sheet provides an overview of the features and architecture of the NR4650G CPU. A more detailed description of the processor is available in the "NR4650/NR4645 Processor Hardware User's Manual".

HARDWARE OVERVIEW

The NR4650G family brings a high-level of integration designed for high-performance computing. The key elements of the NR4650G are briefly described below.

Pipeline

The NR4650G uses a 5-stage pipeline similar to the NR3000 and NR4600. The simplicity of this pipeline allows the NR4650G to be lower cost and lower power than super-scaler or super-pipelined processors. Unlike super-scalar processors, applications that have large data dependencies or that require a great deal of load/stores can still achieve performance close to the peak performance of the processor.

Figure 2 shows the NR4650G pipeline.

Integer Execution Engine

The NR4650G implements the MIPS-III Instruction Set Architecture, and thus is fully upward compatible with applica-

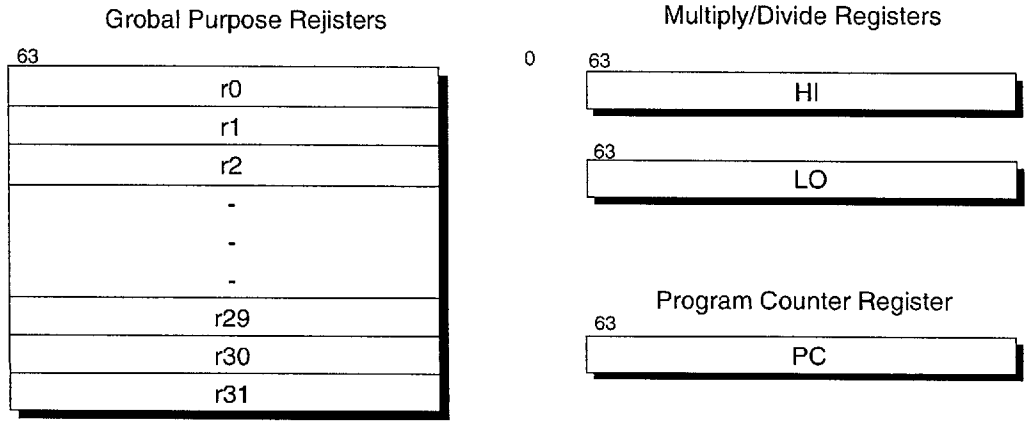
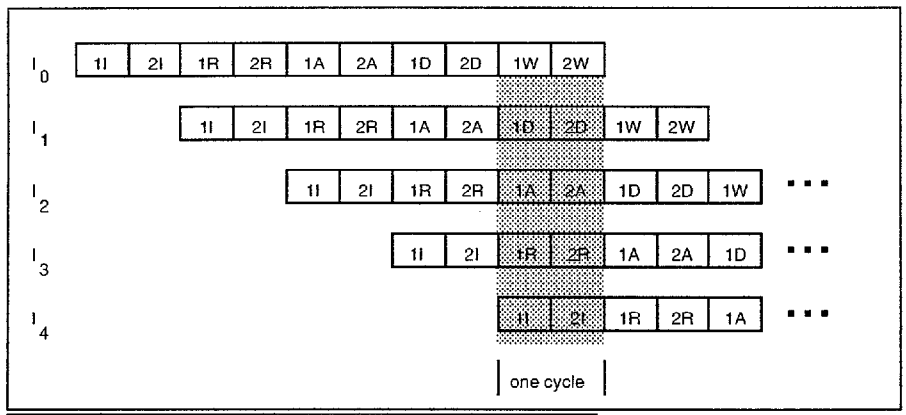


Figure 1: CPU Registers



1I-1R	Instruction cache access
2I	Instruction virtual to physical address translation
2A-2D	Data cache access and load align
1D	Data virtual to physical address translation
1D-2D	Virtual to physical address translation
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, Logical, shift
1A	Data virtual address calculation
2A	Store align
1A	Branch decision
2W	Register file write

Figure 2: NR4650G Pipeline

tions running on the earlier generation parts. The NR4650G includes the same additions to the instruction set found in the NR4600 family of microprocessors, targeted at improving performance and capability while maintaining binary compatibility with earlier NR3000 processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications.

In addition, the NR4650G also implements additional instructions, which are considered extensions to the MIPS-III architecture. These improve the multiply and multiply-add throughput of the CPU, making it well suited to a wide variety of imaging and DSP applications. These extensions, which use op-codes allocated by MIPS Technology for this purpose, are supported by a wide variety of development tools. When operating as a 32-bit processor, the NR4650G will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The 64-bit register resources include: 32 general-purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter, in addition, the on-chip floating-point coprocessor adds 32 floating-point registers, and a floating-point control/status register.

Register File

The NR4650G has 32 general-purpose 64-bit registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline. Figure 1 illustrates the NR4650G Register File.

ALU

The NR4650G ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized and can perform an operation in a single pipeline cycle.

OpCode	Operand Size	Latency	Repeat	Stall
MULT/U, MAD/U	16 bit	3	2	0
	32 bit	4	3	0
MUL	16 bit	3	2	1
	32 bit	4	3	2
DMULT, DMULTU	any	6	5	0
DIV,DIVU	any	36	36	0
DDIV, DDIVU	any	68	68	0

Table 1: NR4650G integer Multiply Operation

Integer Multiply/Divide

The NR4650G uses a dedicated integer multiply/divide unit, optimized for high-speed multiply and multiply-accumulate operation. Table 1 shows the performance, expressed in terms of pipeline clocks, achieved by the NR4650G integer multiply unit.

The MIPS-III architecture defines that the result of a multiply or divide operation are in the HI and LO registers. The values can then be transferred to the general purpose register file using the MFHI(Move From HI)/MFLO(Move From LO) instructions.

The NR4650G adds a new multiply instruction, "MUL", which can specify that the multiply results bypass the "LO" register and are placed immediately in the primary register file, and because of this, throughput of multiply-intensive operations is increased.

An additional enhancement offered by the NR4650G is an atomic "multiply-add" operation, "MAD", used to perform multiply-accumulate operations. This instruction multiplies two numbers and adds the product to the current contents of the HI and LO registers. This operation is used in numerous DSP algorithms, and allows the NR4650G to cost reduce systems requiring a mix of DSP and control functions.

Finally, aggressive implementation techniques feature low latency for these operations along with pipelining to allow new operations to be issued before a previous one has fully completed. Table 1 also shows the repeat rate (peak issue rate), latency, and number of processor stalls required for the various operations. The NR4650G performs automatic operand size detection to determine the size of the operand, and implements hardware interlocks to prevent overrun, allowing this high-performance to be achieved with simple programming.

Floating-Point Co-Processor

The NR4650G incorporates an entire single-precision floating-point co-processor on chip, including a floating-point register file and execution units. The floating-point co-processor forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

The floating-point unit of the NR4650G directly implements single-precision floating point operations. This enables the NR4650G to perform functions such as graphics rendering, without requiring extensive die area or power consumption. The single-precision unit of the NR4650G is directly compatible with the single-precision operation of the NR4600, and features the same latencies and repeat rates.

The NR4650G does not directly implement the double-precision operations found in the NR4600. However, to maintain software compatibility, the NR4650G will signal a trap when a double-precision operation is initiated, allowing the requested function to be emulated in software. Alternatively, the system architect could use a software library emulation of double-precision functions, selected at compile time, to eliminate the overhead associated with trap and emulation.

Floating-Point Units

The NR4650G floating-point execution units perform single precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined, allowing a new multiply to begin every 6 cycles.

As in the NR4600, the NR4650G maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with IEEE Standard 754. Double precision operations are not directly supported; attempts to execute double-precision floating-point operations, or refer directly to double-precision registers, result in the NR4650G signalling a "trap" to the CPU, enabling emulation of the requested function.

Operation	Instruction Latency
ADD	4
SUB	4
MUL	8
DIV	32
SQRT	31
CMP	3
FIX	4
FLOAT	6
ABS	1
MOV	1
NEG	1
LWC1,LDC1	2
SWC1,SDC1	1

Table 2: Floating-Point Operation

Table 2 gives the latencies of some of the floating-point instructions in internal processor cycles.

Floating-Point General Register File

The floating-point register file is made up of thirty-two 32-bit registers. These registers are used as source or target registers for the single-precision operations. Reference to these registers as 64-bit registers will cause a trap to be signalled to the integer unit.

The floating-point control register space contains two registers; one for determining configuration and revision information for the co-processor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

System Control Co-Processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual physical address translation and cache protocols, the exception control system, and the diagnostics capability of the processor.

In the NR4650G, significant changes in CP0 relative to the NR4600 have been implemented. These changes are designed to simplify memory management, facilitate debug, and speed real-time processing.

System Control Co-Processor Registers

The NR4650G incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's address translation is controlled, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the NR4650G includes registers to implement a real-time cycle counting facility, which aids in cache diagnostic testing, assists in data error detection, and facilitates software debug. Alternatively, this timer can be used as the operating system reference timer, and can signal a periodic interrupt.

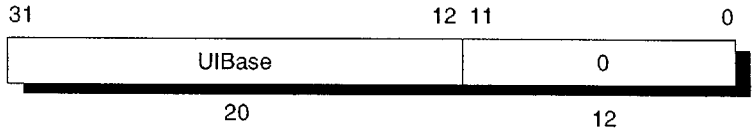
Table 3 shows the CP0 registers of NR4650G.

Number	Name	Function
0	IBase	Instruction address space base
1	IBound	Instruction address spase bound
2	DBase	Data address space base
3	DBound	Data address space bound
4 - 7	-	Reserved
8	BadVAddr	Virtual address on last address exceptions
9	Count	Counts every other cycle
10	-	Reserved
11	Compare	Generate interrupt when Count = Compare
12	Status	Miscellaneous control/status
13	Cause	Last exception/interrupt information
14	EPC	Exception Programm Counter
15	PRId	Processor Revision Identifier
16	Config	Configulation register
17	CAlg	Cache Algorithm
18	IWatch	Instruction breakpoint physical address
19	DWatch	Data breakpoint physical address
20 - 25	-	Reserved
26	ECC	Secondary-cache error checking and correcting (ECC) and Primary parity
27	CacheErr	Cache Error and Status register
28	TagLo	Cache Tag register Lo
29	-	
30	ErrorEPC	Error Exception Program Counter
31	-	Reserved

Table 3: NR4650G CP0 Registers

1. IBase(0)

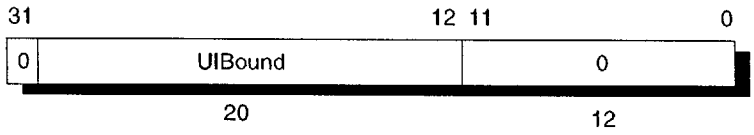
The IBase register provides the User Instruction address space Base address.



UIBase	Added to vAddr31..12 for user space to get physical address
0	reserved for future use (currently reads as 0, ignored on write)

2. IBound(1)

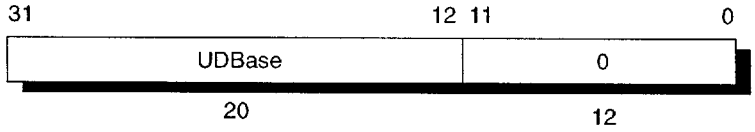
The IBound register provides the User Instruction address space Bound. Virtual addresses greater than this value cause address error exceptions.



UIBound	Compared to vAddr30..12 for user space to validate address
0	reserved for future use (currently reads as 0, ignored on write)

3. DBase(2)

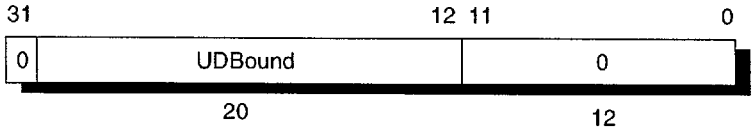
The IBase register provides the User Data address space Base address.



UDBase	Added to vAddr31..12 for user pace to get physical address
0	reserved for future use (currently reads as 0, ignored on write)

4. DBound(3)

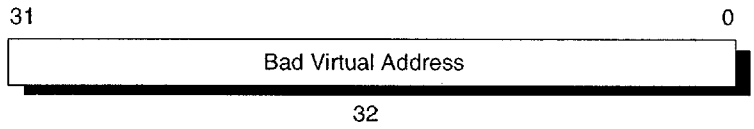
The DBound register provides the User Data address space Bound. Virtual addresses greater than this value cause address error exceptions.



UDBound	Compared to vAddr30..12 for user space to validate address
0	reserved for future use (currently reads as 0, ignored on write)

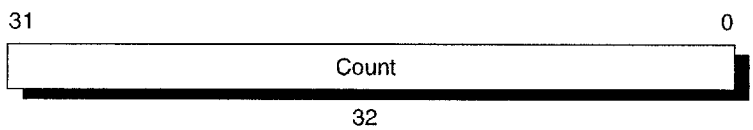
5. BadVAddr(8)

The BadVAddr register is read-only register that contains for address error and bounds exceptions, the virtual address that cause the exception. For other exceptions, the BadVAddr register is undefined.



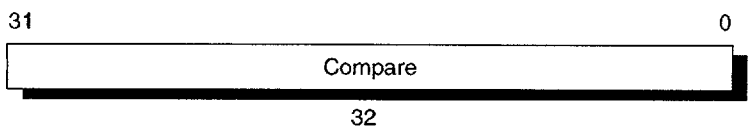
6. Count(9)

The Count register is read-write register that acts as timer, incrementing at a constant rate (half the maximum instruction issue rate). This register is used for diagnostic purposes or system initialization



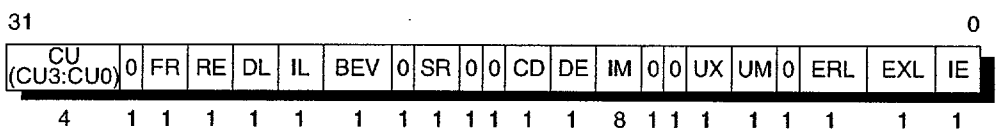
7. Compare(11)

The Compare register is read-write register that acts as timer. When the value of the Count register equals the value of the Compare register, that causes a interrupt. Writing a value to the Compare register clears the timer interrupt.



8. Status(12)

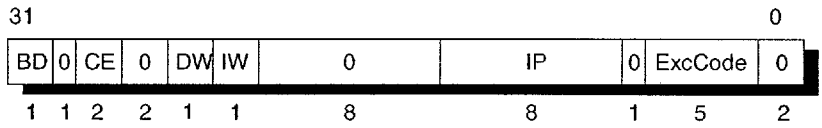
The Status register is read-write register with miscellaneous control and status bits for the processor



Field	Description
CU	Countrols the usability of reach of the four coprocessor unit numbers. CP0 is always usable when in kernel mode, regardless of the setting of CU0 bit. 1→usable 0→unusable
0	Reserved. Set to 0.
FR	Enables additional floating-point registers 0→16 registers 1→32 registers
RE	Reverse-Endian bit, valid in User mode.
DL	Data cache lock 0→normal opreation 1→refill into set A disabled
IL	Instruction cache lock: 0→normal operation, 1→refill into set A disabled 0→normal operation 1→refill into set A disabled
BEV	Control the general exception vectoes.:0→normal, 1→bootstrap 0→normal 1→bootstrap
0	Reserved. Set to 0.
SR	1→Indicates a soft reset or NMI has occurred.
0	Reserved. Set to 0.
0	Reserved. Set to 0.
CE	Contents of the ECC register set or modify the check bits of the caches when CE=1;see description of the ECC register.
DE	Specifies that cache parity errors cannot cause exceptions. 0→parity remains enabled 1→disables parity
IM	Interrupt Mask:controls the enabling of each of the external,internal,and softeare interrupts. An interrupt is taken if interrypts are enabled,and the corresponding bits are set in both the Interrupt Mask field of the Status register and the Interrupt Pending filed of the Cause register.IM[7:2] correspond to interrupts Int[5:0] and IM[1:0] to the softeare interrupts. 0→disabled 1→enabled
0	Reserved. Set to 0.
0	Reserved. Set to 0.
UX	Enables 64-bit virtual addressing and operations in User mode. 0→32-bit 1→64-bit
UM	Mode bits 0→Kernel mode 1→User mode
0	Reserved. Set to 0.
ERL	Error Level 0→normal 1→error
EXL	Exception Level 0→normal 1→exception
IE	Interrupt Enable 0→disable interrupts 1→enables interrupts

9. Cause(13)

The Cause register is read-write register that describes the nature of the last exception.

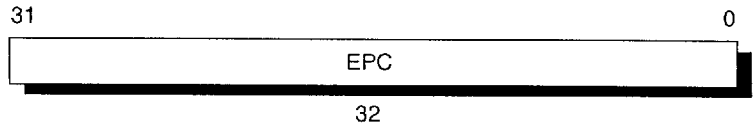


Field	Description
BD	Indicates whether the last exception taken occurredin a branch delay slot. 1→delay slot 0→normal
CE	Coprocessor unit number referenced when a Coprocessor Unusables exception is taken.
DW	On a Watch exception, this field indicates that the DWatch register mathced. On other exceptions, this field is undefined.
IW	On a Watch exception, this field indicates that the IWathc register matced. On other exceptions,this field is undefined.
IP	Indeicates an interrupt is pending. 1→interrupt pending 0→no interrupt
ExcCode	Exception code field
0	Reserved. Must bi written as zeres, and returns zeroes when read.

Exception code	Description
0	Inrerrupt
1	Reserved
2	Instruction bound exception
3	Data bound exception
4	Address error exception (load or instruction fetch)
5	Address error exception (store)
6	Bus error exception (instruction fetch)
7	Bus error exception (load or store)
8	Syscall exception
9	Breakpoint exception
10	Reserved instruction exception
11	Coprocessor Unusable exception
12	Arthmetic Overflow exception
13	Trap exception
14	Reserved
15	Floating Point exception
16-22	Reserved
23	Watch exception
24-31	Reserved

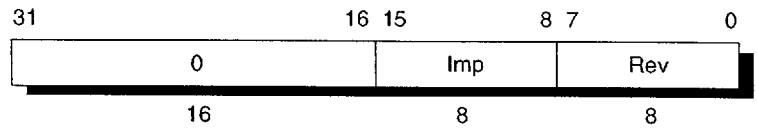
10. EPC(14)

EPC register is read-write register that contains the virtual address of the instruction that caused th last exception.



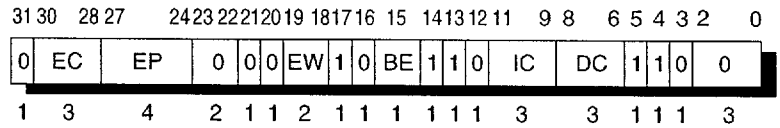
11. PRId(15)

The PRId register is a read-only register that identifies the revision level of the processor.
In the case of NR4650G PRId "Imp" value is 0x22.



12. Config(16)

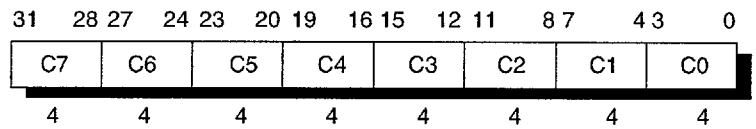
The Config register is read-only register that contains the processor's configuration.



Field	Description
EC	System clock ratio : 0 → Processor clock frequency divided by 2 1 → Processor clock frequency divided by 3 2 → Processor clock frequency divided by 4 3 → Processor clock frequency divided by 5 4 → Processor clock frequency divided by 6 5 → Processor clock frequency divided by 7 6 → Processor clock frequency divided by 8 7 → Reserved
EP	Write-back data rate : 0 → DDDD — Doublewords every cycle 1 → DDxDDx — 2 Doublewords every 3 cycles 2 → DDxxDDxx — 2 Doublewords every 4 cycles 3 → DxDxDxDx — 2 Doublewords every 4 cycles 4 → DDxxxDDxxx — 2 Doublewords every 5 cycles 5 → DDxxxxDDxxxx — 2 Doublewords every 6 cycles 6 → DxxDxxDxxDxx — 2 Doublewords every 6 cycles 7 → DDxxxxxDDxxxxx — 2 Doublewords every 7 cycles 8 → DxxxDxxxDxxxDxxx — 2 Doublewords every 8 cycles 9 - 15 — Reserved
EW	SysAD bus size 0 → 64-bits 1 → 32-bits
IC	Primary I-cache size (I-cache size = 212 + ic byte). In the NR4650G processor, this is set to 8K-byte (IC = 001)
DC	Primary D-cache size (D-cache size = 212 + ic byte). In the NR4650G processor, this is set to 8K-byte (IC = 001)
Other	Reserved. Returns indicated values when read.

13. CAlg(17)

The CAlg register is read-write register that specifies the cache algorithm for each 512MB region of the virtual address space.



C0 cache algorithm for 0x00000000 to 0x1FFFFFFF
C1 cache algorithm for 0x20000000 to 0x3FFFFFFF
C2 cache algorithm for 0x40000000 to 0x5FFFFFFF
C3 cache algorithm for 0x60000000 to 0x7FFFFFFF
C4 cache algorithm for 0x80000000 to 0x9FFFFFFF
C5 cache algorithm for 0xA0000000 to 0xBFFFFFFF
C6 cache algorithm for 0xC0000000 to 0xDFFFFFFF
C7 cache algorithm for 0xE0000000 to 0xFFFFFFFF

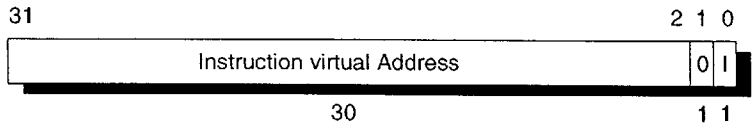
cache algorithms are as follows:

0	cached, non-coherent, write-through, no write-allocate
1	cached, non-coherent, write-through, write-allocate
2	uncached
3	cached, non-coherent, write-back, write-allocate
4-15	reserved for future use

Calg is initialized to 0x22233333 on reset.

14. IWatch(18)

The IWatch register is read-write register that contains an instruction virtual address that causes a Watch exception. When vAddr31..2 of an instruction fetch matches IvAddr of this register, and the I bit is set, a Watch exception is taken.

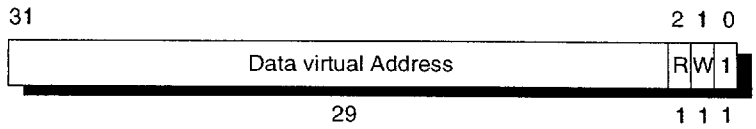


IvAddr	Instruction virtual address that cause a watch exception
I	0→IWatch disabled, 1→IWatch enabled
0	reserved for future use

I bit is cleared on reset

15. DWatch(19)

The DWatch register is read-write register that contains an data virtual address that cause a Watch exception. When vAddr31..3 of a load matches DvAddr of this register and the R bit is set, or when vAddr31..3 of a store matches DvAddr of this register and the W bit is set, a Watch exception is taken.



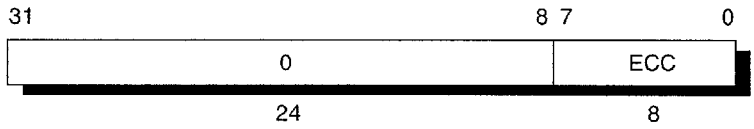
DvAddr	Data virtual address that cause a watch exception
R	0→DWatch disable for loads, 1→DWatch enabled for loads
W	0→DWatch disable for stores,1→DWatch enabled for stores
0	reserved for future use

R and W bit is cleared on reset

16. ECC(26)

The 8-bit ECC register reads or writes primary-cache data parity bit for cache initialization, cache diagnostics, or cache error processing. (Tag parity is loaded from and stored to the TagLo register.) The ECC register is loaded by the Index Load Tag CACHE operation. Content of the ECC register is:

- written into the primary data cache on store instructions (instead of the computed parity) when the CE bit of the Status register is set.
- substituted for the computed instruction parity for the CACHE operation Fill.

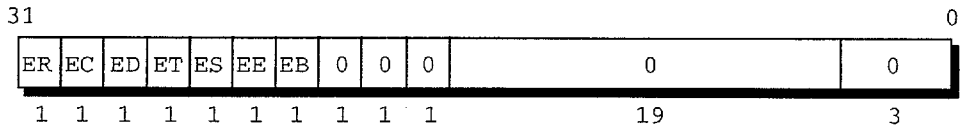


Field	Description
ECC	An 8-bit field specifying the parity bits read from or written to primary cache.
0	Reserved Must be written as zeroes, and returns zeroes when read.

17. CacheErr(27)

The CacheErr register is read-only register that processes parity errors in the primary cache. Parity errors cannot be corrected.

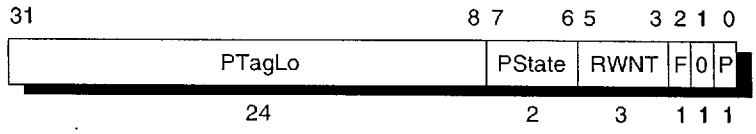
The CacheErr register holds cache index and status bits that indicate the source and nature of the error; it is loaded when a Cache Error exception is asserted.



Field	Description
ER	Type of reference 0 → instruction 1 → data
EC	Cahce level of the error 0 → primary 1 → Reserved
ED	Indicates if a data field error occurred 0 → no error 1 → error
ET	Indicates if a tag field error occurred 0 → no error 1 → error
ES	Indicates that a cache miss parity error occurred in the first doubleword of read response data (only the first doubleword erroneous data bit is checked) 0 → no cache miss parity error 1 → cache miss parity error
EE	This bit is set if the error occurred on the SysAD bus.
EB	This bit is set if a data error occurred in addition to the instruction error (indicated by the remainder of this bits). If so, this requires flushing the data cache after fixing the instruction error.
0	Reserved Must be written as zeroes, and returns zeroes when read.

18. TagLo(28)

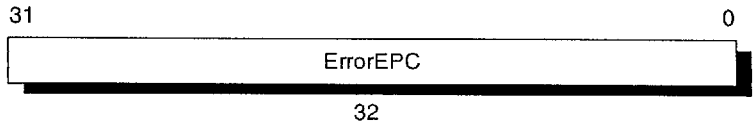
The TagLo register is read-write register that hold the primary cache tag and parity during cache initialization, cache diagnostics, or cache error processing. The TagLo register are written by the CACHE and MTC0 instructions.
The P bit of this register is ignored on Index Store Tag operations.



Field	Field
PTagLo	Specifies the physical address bits 35 : 12
PState	Specifies the primary cache state
P	Specifies the primary tag even parity bit
F	the FIFO bit used to implement FIFO refill of the cache
RWNT	Read/Write bits required for WindowsNT
0	Reserved Must be written as zeroes, and returns zeroes when read.

19. ErrorEPC(30)

The ErrorEPC register is read-write register that contains the virtual address of the instruction that caused the last parity error exception.



Operation modes

The NR4650G supports two modes operation: user mode and kernel mode. Kernel mode operation is typically used for exception handling and operating system kernel functions, including CP0 management and access to IO devices. In kernel mode, software has access to the entire address space and all of the co-processor 0 registers, and can select whether to enable co-processor 1 accesses. The processor enters kernel mode at reset, and whenever an exception is recognized.

User mode is typically used for applications programs. User mode access are limited to a subset of the virtual address space, and can be inhibited from accessing CP0 functions.

Virtual to Physical Address Mapping

The 4GB virtual address space of the NR4650G is shown in figure 3. The 4GB address space is divided into addresses accessible in either kernel or user mode (kuseg), and addresses only accessible in kernel mode (kseg2 - 0).

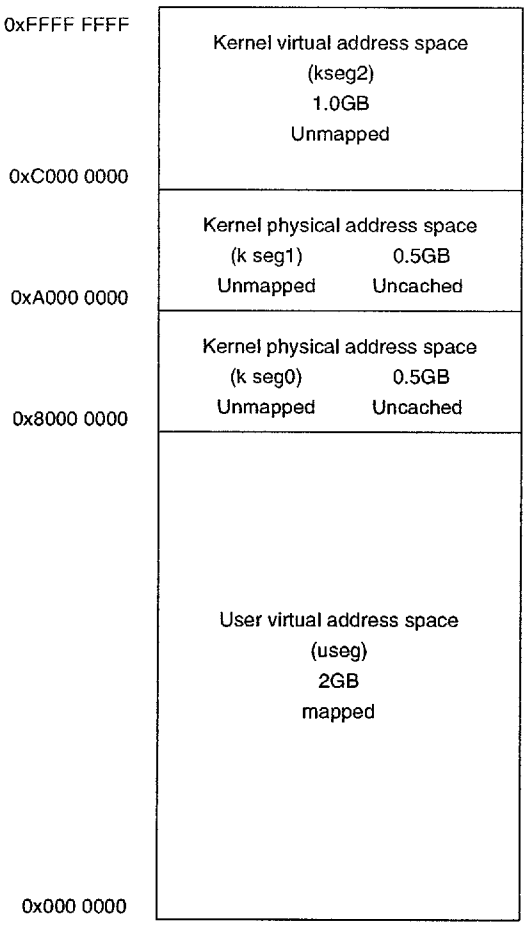


Figure 3: Mode Virtual Addressing (32-bit mode)

The NR4650G supports the use of multiple user tasks sharing common virtual address, but mapped to separate physical addresses. This facility is implemented via the "base-bounds" registers contained in CP0.

When a user virtual address is asserted (load, store, or instruction fetch), the NR4650G compares the virtual address with the contents of the appropriate "bounds" register (instruction or data). If the virtual address is "in bounds", the values of the corresponding "base" register is added to the virtual address to form the physical address for that reference. If the address is not within bounds, an exception is signed.

Kernel mode addresses do not use the base-bounds registers, but rather undergo a fixed virtual to physical address translation. The rules for this translation are also shown in figure 4.

Debug Support

To facilitate software debug, the NR4650G adds a pair of "watch" registers to CP0. When enabled, these registers will cause the CPU to take an exception when a "watched" address is appropriately accessed.

Interrupt Vector

The NR4650G also adds the capability to speed interrupt exception decoding. Unlike the NR4600, which utilizes a single common exception vector for all exception types (including interrupts), the NR4650G allows kernel software to enabled, this vector location speeds interrupt processing by allowing software to avoid decoding interrupts from general purpose exceptions.

Cache Memory

In order to keep the NR4650G's high-performance pipeline full and operating efficiently, the NR4650G incorporates on-chip instruction and data caches that can each be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of over 1500MB per second at a pipeline clock frequency of 133MHz. The cache subsystem is similar in construction to that found in the NR4600, although some changes have been implemented.

Table 11 is an overview of the caches found on the NR4650G.

Instruction Cache

The NR4650G incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 8KB in size and is parity protected.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 20-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bit wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 533MB/sec at 133MHz. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill, can write 64 bits-per-cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

In addition, the contents of one set of the instruction cache (set "A") can be "locked" by setting a bit in a CP0 register. Locking the set prevents its contents from being overwritten by a subsequent cache miss; refill occurs then only into "set B". This operation effectively "locks" time critical code into one 4KB set, while allowing the other set to service other instruction streams in a normal fashion. Thus, the benefits of cached performance are achieved, while deterministic real-time response is preserved.

Data Cache

For fast, single cycle data access, the NR4650G includes an 8KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

Characteristics	Instruction	Data
size	8 KB	8 KB
organization	2-way set associative	2-way set associative
line size	32 B	32 B
index	vAddr11..0	vAddr11..0
tag	pAddr31..12	pAddr31..12
write policy	-	writeback / writethrough
line transfer order	sub-block order	sub-block order
miss restert after transfer of	entire line	first word
parity	per-word	per-byte
Cache Locking	Set A	Set A

Table 11: NR4650G Cache Attributes

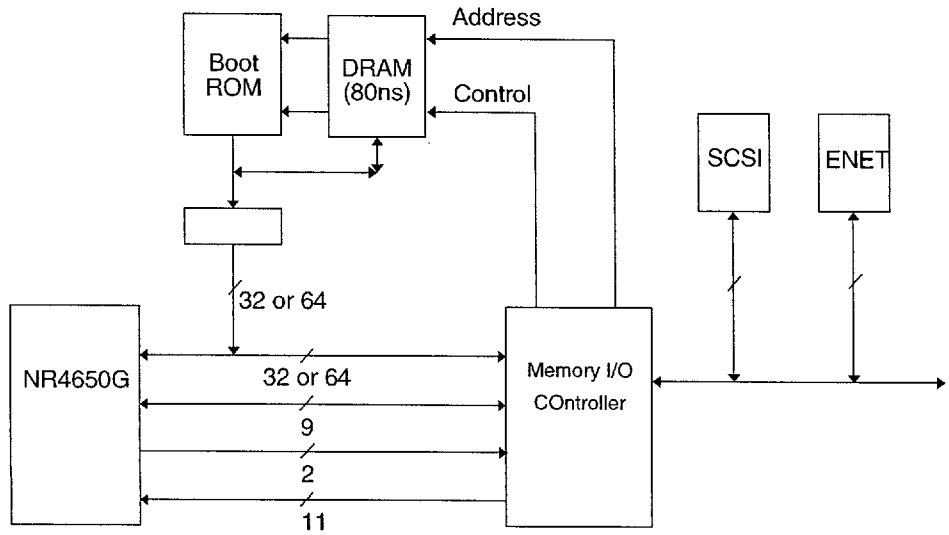


Figure 4: Typical NR4650G System Architecture

The normal write policy is write-back, which means that a store to a cache line does not immediately cause memory to be updated. On the other hand, software can however select write-through for certain address ranges, using the CAlg register in CP0. Cache protocols supported for the data cache are:

• Uncached

Addressees in a memory area indicated as uncached will not be read from the cache. Stores to such addresses will be written directly to main memory, without changing cache contents.

• Write-back

Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. ON data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents will be updated, and the cache line marked for later write-back. If the cache lookup misses, the target line is first brought into the cache before the cache is updated.

• Write-through with write allocate

Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the caches is first searched to see is the target address is cache resident. If it is resident, the cache contents will be updated and main memory will also be written; the state of the "write-back" bit of the cache line will be uncached. If the cache looks up misses, the target line is first brought into the cache before the cache is updated.

• Write-back-through without write-allocate

Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents will be updated, and the cache line marked for later Write-back. If the cache lookup misses, then only main memory is written.

Associated with the Data Cache is the store buffer. When the NR4650G executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the Data Cache in the next cycle that the Data Cache is not accessed (the next non-load cycle). The store buffer allows the NR4650G to execute a store every processor cycle and to perform back-to-back stores without penalty.

Write buffer

Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses, use the on-chip write buffer. The write buffer holds up to four address and data pairs. The entire buffer is used for a data cache Write-back and allows the processor to proceed in parallel with memory update. For uncached and write-through stores, the wrote buffer significantly increases performance over the R4000 family of processors.

System Interface

The NR4650G supports a 64-bit system inter face that is bus compatible with the NR4600 system interface. In addition, the NR4650G supports a 32-bit system interface mode, allowing the CPU to interface directly with a lower cost memory system.

The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals and 6 interrupt inputs. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 533MB/sec at 133MHz.

The NR4650G clocking interface allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock, and can be between 25 and 64MHz (somewhat dependent on maximum pipeline speed for the CPU).

An on-chip PLL (Phase-Locked-Loop) generates the pipeline clock from the system interface clock by multiplying it up an amount selected at system reset. Supported multipliers are values 2 through 8 inclusive, allowing systems to implement pipeline clocks at significantly higher frequency than the system interface clock.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the NR4650G and the rest of the system. It is protected with an 8-bit parity check bus, SysADC. When initialized for 32-bit operation, SysAD can be viewed as a 32-bit multiplexed bus, with 4 parity check bits.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The rate at which the CPU transmits data to the system interface is

programmable via boot time mode control bits. The rate at which the processor receives data is fully controlled by the external devise. Therefore, either a low cost interface requiring no read or write buffering or a faster, high performance interface can be designed to communicate with the NR4650G.

System Command Bus

The NR4650G interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates, what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this data line is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the NR4650G.

The NR4650G supports single datum (one to eight byte) and 8-word block transfers on the SysAD bus. The choice of 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles, and whether a single datum transfer lager than 4 bytes need to be broken into two smaller transfers.

Handshake Signals

There are six handshake signals on the system interface. Two of these, $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ are used by an external device to indicate to the NR4650G whether it can accept a new read or write transaction. $\overline{\text{ExtRqst}}$ and $\overline{\text{Release}}$ are used to transfer control of the SysAD and SysCmd busses between the processor and an external device. When an external device needs to control the interface, it asserts $\overline{\text{ExtRqst}}$. The NR4650G responds by asserting $\overline{\text{Release}}$ to release the system interface to slave state.

$\overline{\text{ValidOut}}$ and $\overline{\text{ValidIn}}$ are used by the NR4650G and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd busses. The NR4650G asserts $\overline{\text{ValidOut}}$ when it is driving these busses with valid command or data, and the external device drives $\overline{\text{ValidIn}}$ when it has control of the busses and is driving a valid command or data.

Read/Write Protocol

The NR4650G asserts $\overline{\text{ValidOut}}$ and simultaneously drives the address and read command on the SysAD and SysCmd busses. If $\overline{\text{RdRdy}}$ is asserted, then the processor tri-states its drivers and releases the system interface to slave state by asserting $\overline{\text{Release}}$. The external device can then begin sending the data to the NR4650G.

Figure 5 shows a processor block read request and the external agent read response. The read latency is 4 cycles ($\overline{\text{ValidOut}}$ to $\overline{\text{ValidIn}}$), and the response data pattern is DDxxDD. Figure 6 shows a processor block write.

When the NR4650G is used in 32-bit mode, Write-back pattern is follows.

64-bit → 32-bit

0 DDDD
→ WWWWWWWW

1 DDxDDx
→ WWxWWxWWxWWx

2 DDxxDDxx
→ WWxxWWxxWWxxWWxx

3 DxDxDxDx
→ WxWxWxWxWxWxWxWx

4 DDxxxDDxxx
→ WWxxxWWxxxWWxxxWWxxx

5 DDxxxxDDxxxx
→ WWxxxxWWxxxxWWxxxxWWxxxx

6 DxxDxxDxxDxx
→ WxxWxxWxxWxxWxxWxxWxxWxx

7 DDxxxxxxDDxxxxxx
→ WWxxxxxxWWxxxxxxWWxxxxxxWWxxxxxx

8 DxxxDxxxDxxxDxxx
→ WxxxWxxxWxxxWxxxWxxxWxxxWxxxWxxx

* D indicates double word (64-bit), W indicates a word (32-bit).

• Write Reissue and Pipeline Write

The NR4600 and NR4650G implement additional write protocols designed to improve performance. This implementation doubles the effective write bandwidth. The write re-issue has a high repeat rate of 2 cycles per write. A write issues if $\overline{\text{WrRdy}}$ is asserted 2 cycles earlier and is still asserted at the issue cycle. If it is not still asserted, the last write re-issue again. Pipelined writes have the same 2-cycle per write repeat rate, but can issue one more write after $\overline{\text{WrRdy}}$ de-asserts. They still follow the issue rule as R4x00 mode for other writes.

External Requests

The NR4650G responds to requests issued by an external

device. The requests can take several forms. An external device may need to supply data in response to an NR4650G read request or it may need to gain control over the system interface bus to access other resources which may be on that bus.

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost EPROM.

Immediately after the Vccok Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

Boot-Time Modes

The boot-time serial mode stream is defined in Table 12. Bit 0 is the bit presented to the processor when Vccok is asserted; bit 255 is the last.

Power Management

CP0 is also used to control the power management for the NR4650G. This is the standby mode and it can be used to reduce the power consumption of the internal core of the CPU.

Executing the WAIT instruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAD bus is currently idle, the inter-

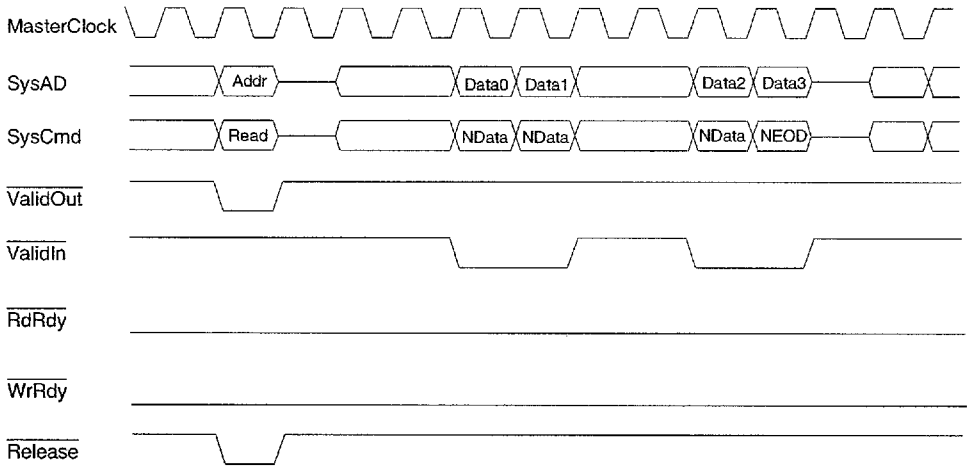


Figure 5: NR4650G Block Read Request (64-bit interface option)

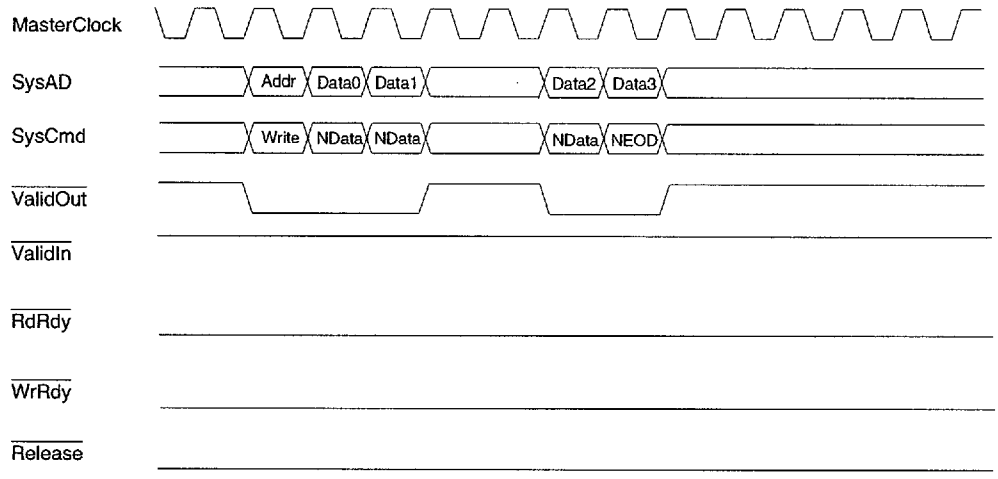


Figure 6: NR4650G Block Write Request (64-bit system interface)

nal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins ($\overline{\text{Int}}$[5:0], $\overline{\text{NMI}}$, $\overline{\text{ExtRqst}}$, and $\overline{\text{ColdReset}}$) will continue to run. If the conditions are not correct when the WAIT instruction finished the W pipe-stage (i.e. the SysAD bus is not idle), the WAIT is treated as a NOP.

Once the CPU is Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Mode bit	Value	Mode setting
0	Reserved (must be zero)	
1:4	Writeback data rate	
	0	D
	1	DDx
	2	DDxx
	3	DxDx
	4	DDxxx
	5	DDxxxx
	6	DxxDxx
	7	DDxxxxxx
	8	DxxxDxxx
	9-15	Reserved
5:7	Clock multiplier	
	0	2
	1	3
	2	4
	3	5
	4	6
	5	7
	6	8
	7	Reserved
8	Specifies byte ordering	
	0	Little-endian
	1	Big-endian
9:10	Selects the manner in which non-block writes are handled	
	0	R4000 compatible
	1	Reserved
	2	Pipelined writes
	3	Write re-issue
11	Disables the timer interrupt on Int(5)	
	0	Enabled Timer Interrupt
	1	Disabled Timer interrupt
12	Bit width of system interface	
	0	64 bit
	1	32 bit
13:14	Output driver slew rate control	
	10	100%
	11	83%
	00	67%
	01	50%
15 : 255	Reserved (must be zero)	

Table 12: Boot time mode stream

■ ABSOLUTE MAXIMUM RATINGS (1)

(VCC = 3.3V ± 5%)

Symbol	Parameter	Rating (3.3V ± 5%)	Unit
$V_{TERM(Vdd)}$	Terminal Voltage with respect to GND	-0.5 to +4.6	V
$V_{TERM(Vin)}$	Terminal Voltage with respect to GND	-0.5(2) to +5.8	V
T_C	Operating Temperature (Case)	0 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{IN}	DC Input Current	20(3)	mA
I_{OUT}	DC Output Current	50(4)	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = -2.0V for pulse width less than 15ns.
3. When VIN < 0V or VIN > VCC
4. Not more than one output should be shorted at a time. Duration of the short should not exceeded 30 seconds.

■ RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +85°C (Case)	0V	3.3V ± 5%

■ DC CHARACTERISTICS

(VCC = 3.3V ± 5%, Tcase = 0 to +85°C)

Parameter	Symbol	NR4650G 100MHz		NR4650G 133MHz		Conditions
		Minimum	Maximum	Minimum	Maximum	
Output Voltage for Low level	V_{OL}	-	0.1V	-	0.1V	|Iout| = 20µA
Output Voltage for High level	V_{OH}	Vcc - 0.1V	-	Vcc - 0.1V	-	
Output Voltage for Low level	V_{OL}	-	0.4V	-	0.4V	|Iout| = 4mA
Output Voltage for High level	V_{OH}	2.4V	-	2.4V	-	
Input Voltage for Low level	V_{IL}	-0.5V	0.7Vcc	-0.5V	0.7Vcc	
Input Voltage for High level	V_{IH}	0.7Vcc	5.8V	0.7Vcc	5.8V	
Output Voltage for High level	V_{OHC}	-	-	-	-	
Input Voltage for Low level	V_{ILC}	-	-	-	-	
Input Voltage for High level	V_{IHC}	-	-	-	-	
Input Capacitance	C_{IN}	-	10pF	-	10pF	
Output Capacitance	C_{OUT}	-	10pF	-	10pF	
I/O Leakage Current	I/O_{LEAK}	-	20µA	-	20µA	

■ POWER CONSUMPTION

Parameter		NR4650G 100MHz		NR4650G 133MHz		Conditions
		typical	Max.	typical	Max.	
System Condition		100/50MHz		133/44MHz		-
Icc	Standby	-	50mA	-	60mA	C_L = 0pF
		-	100mA	-	110mA	C_L = 50pF
	active, 64-bit bus option	475mA	700mA	625mA	925mA	C_L = 0pF No SysAD activity
		550mA	925mA	700mA	1150mA	C_L = 50pF R4x00 compatible writes Tc = 25°C
		550mA	925mA	700mA	1300mA	C_L = 50pF Pipelined write or Write re-issue, Tc = 25°C
	active, 32-bit bus option	475mA	700mA	625mA	925mA	C_L = 0pF No SysAD activity
		525mA	825mA	650mA	1050mA	C_L = 50pF R4x00 compatible writes Tc = 25°C
		525mA	825mA	650mA	1125mA	C_L = 50pF Pipelined write or Write re-issue, Tc = 25°C

■ Clock Parameters

Parameter	Symbol	Test Conditions	NR4650G 100MHz		NR4650G 133MHz		Unit
			Min.	Max.	Min.	Max.	
Pipeline Clock Frequency	P_{CLK}	-	50		50		MHz
MasterClock HIGH	t_{MCHigh}	Transition ≤ 5ns	4		3		ns
MasterClock LOW	t_{MCLow}	Transition ≤ 5ns	4		3		ns
MasterClock Frequency(5)		-	25	50	25	67	MHz
MasterClock Period	t_{MCP}	-	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$	-		± 250		± 250	ps
MasterClock Rise Time	t_{MCRise}	-		5		4	ns
MasterClock Fall Time	t_{MCFall}	-		5		4	ns
ModeClock Period	$t_{ModeCKP}$	-		256* t_{MCP}		256* t_{MCP}	ns

NOTES:

5. Operation of he NR4650G is only guaranteed with the Phase Lock Loop enabled.

■ System Interface Parameters (6)

Parameter	Symbol	Test Conditions	NR4650G 100MHz		NR4650G 133MHz		Unit
			Min.	Max.	Min.	Max.	
Data Output(7)	t_{DM}=Min.	$mode_{14..13}$ = 10 (fastest)	1	9	1	9	ns
	t_{DM}=Max.	$mode_{14..13}$ = 01 (slowest)	2	12	2	12	ns
Data Setup	t_{DS}	t_{rise} = 5ns	3.5		3.5		ns
Data hold	t_{DH}	t_{fall} = 5ns	1.5		1.5		ns

6. Timings are measured from 1.5V of the clock to 1.5V of the signal.
7. Capacitive load for all output timings is 50pF.

■ Boot Time Interface Parameters

Parameter	Symbol	Test Conditions	NR4650G 100MHz		NR4650G 133MHz		Unit
			Min.	Max.	Min.	Max.	
Mode Data Setup	t_{DS}	-	3		3		Master Clock Cycle
Mode Data hold	t_{DH}	-	0		0		Master Clock Cycle

■ Package Information

208-PIN PQFP