

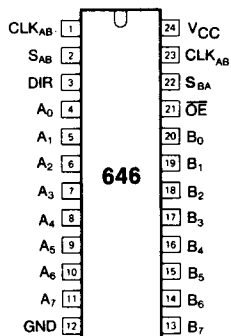
GD54/74HC646, GD54/74HCT646

OCTAL 3-STATE NONINVERTING TRANSCEIVERS AND D-TYPE FLIP-FLOPS

General Description

These devices are identical in pinout to the 54/74LS646. They are bus transceivers with D-type flip-flops designed for high speed multiplexed transmission of data. Depending upon the states of the data source selection inputs, data may be routed to the outputs either from the flip-flops or directly from the inputs. The output enable and the direction pins control the transceiver function. Only one of the two buses, A or B, may be enabled as outputs at any time. However, when either or both of the outputs are in the high impedance state, the pins may be used as inputs to the D-type flip-flops for storage of data. The HC/HCT 648 have similar function with inverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS						DATA I/O*		FUNCTION
OE	DIR	CLK _{AB}	CLK _{BA}	S _{AB}	S _{BA}	A ₀ to A ₇	B ₀ to B ₇	
H	X	H or L	H or L	X	X	input	input	isolation store A and B data
H	X	†	†	X	X			
L	L	X	X	X	L	output	input	real-time B data to A bus stored B data to A bus
L	L	X	X	X	H			
L	H	X	X	L	X	input	output	real-time A data to B bus stored A data to B bus
L	H	H or L	X	H	X			

* The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 † = LOW-to-HIGH level transition

Logic Diagram

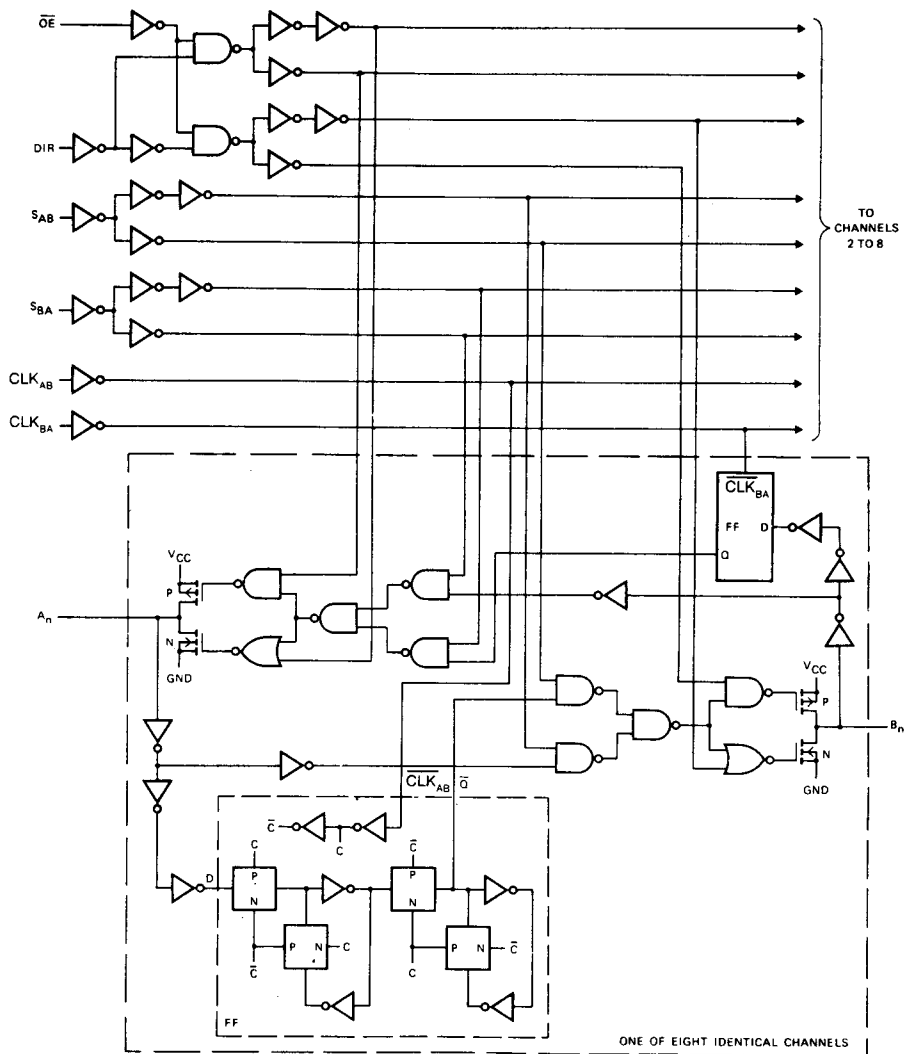


Fig. 1 Logic Diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT646		GD54HCT646		UNIT					
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.						
V _{IH}	HIGH level input Voltage		2.0	1.5			1.5		1.5		V					
			4.5	3.15			3.15		3.15							
			6.0	4.2			4.2		4.2							
V _{IL}	LOW level input voltage		2.0			0.3		0.3		0.3	V					
			4.5			0.9		0.9		0.9						
			6.0			1.2		1.2		1.2						
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0	1.9	2.0		1.9		1.9	V					
				4.5	4.4	4.5		4.4		4.4						
				6.0	5.9	6.0		5.9		5.9						
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0			0.1		0.1		V					
				4.5			0.1		0.1							
				6.0			0.1		0.1							
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		6.0			0.1		1.0		1.0	μA				
			I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL}	V _O =V _{CC} or GND		6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0				8		80		160	μA				

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT646		GD54HCT646		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V	
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V	
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V	
			I _{OH} =-6mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1		0.1		0.1	V
			I _{OL} =6mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA	
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL}	V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA	

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50pF$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC646		GD54HC646		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse with	CLK _{AB} , CLK _{BA}	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t _{su}	Setup time	An, Bn to CLK _{AB} , CLK _{BA}	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t _h	Hold time	An, Bn to CLK _{AB} , CLK _{BA}	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50 pF$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC648		GD54HC648		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum clock pulse frequency		2.0	6	20		5		4		ns
			4.5	30	65		25		20		
			6.0	35	75		30		25		
t _{PLH} / t _{PHL}	Propagation Delay Time An, Bn to Bn, An		2.0		45	140		180		210	ns
			4.5		15	30		36		40	
			6.0		14	26		33		38	
t _{PLH} / t _{PHL}	Propagation Delay Time CLK _{AB} , CLK _{BA} to Bn, An		2.0		40	140		180		210	ns
			4.5		12	25		35		40	
			6.0		10	24		32		38	
t _{PLH} / t _{PHL}	Propagation Delay Time S _{AB} , S _{BA} to Bn, An		2.0		50	150		190		250	ns
			4.5		16	35		50		60	
			6.0		15	22		45		55	
t _{PZH} / t _{PZL}	3-state Output Enable Time OE to A _i , B _n		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
t _{PLZ} / t _{PHZ}	3-state Output Disable Time OE to An, Bn		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
t _{PZH} / t _{PZL}	3-state Output Enable Time DIR to An, Bn		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
t _{PLZ} / t _{PHZ}	3-state Output Disable Time DIR to An, Bn		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
t _{TLH} / t _{THL}	Output Transition Time		2.0		15	60		75		90	ns
			4.5		6	12		15		18	
			6.0		5	10		13		15	

Timing Requirements for HCT: $t_r=t_f=6ns$ $C_L=50pF$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HCT646		GD54HCT646		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	CLK _{AB} , CLK _{BA}	4.5	16	10		20		25		ns
t _{su}	Setup time	An, Bn to CLK _{AB} , CLK _{BA}	4.5	12	10		20		25		ns
t _h	Hold time	An, Bn to CLK _{AB} , CLK _{BA}	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6ns$ $C_L=50 pF$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HCT648		GD54HCT648		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency		4.5	27	54		22		18		ns
t _{PLH} / t _{PHL}	Propagation Delay Time An Bn to Bn, An		4.5		16	30		36		40	ns
t _{PLH} / t _{PHL}	Propagation Delay Time CLK _{AB} , CLK _{BA} to Bn, An		4.5		14	28		35		40	ns
t _{PLH} / t _{PHL}	Propagation Delay Time S _{AB} , S _{BA} to Bn An,		4.5		18	36		50		60	ns
t _{PZH} / t _{PZL}	3-state Output Enable Time OE to An, Bn		4.5		19	38		42		52	ns
t _{PLZ} / t _{PHZ}	3-state Output Disable Time OE to An, Bn		4.5		19	38		42		52	ns
t _{PZH} / t _{PZL}	3-state Output Enable Time DIR to An, Bn		4.5		19	38		42		52	ns
t _{PLZ} / t _{PHZ}	3-state Output Disable Time DIR to An, Bn		4.5		19	38		42		52	ns
t _{TLH} / t _{THL}	Output Transition Time		4.5		6	12		15		18	ns

AC Waveforms

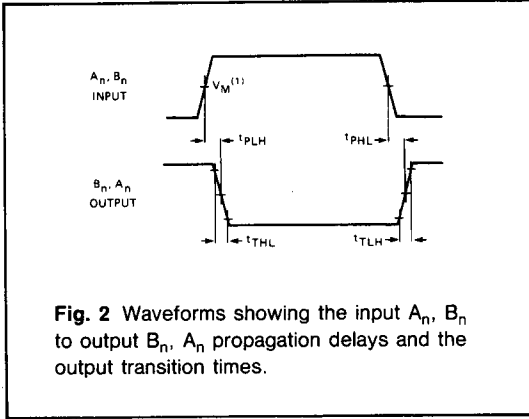


Fig. 2 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

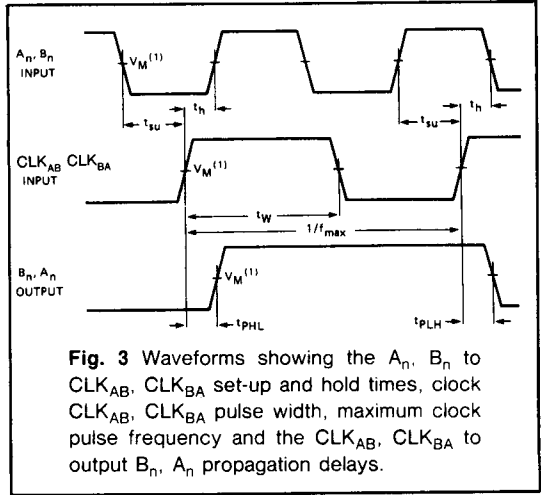


Fig. 3 Waveforms showing the A_n, B_n to CLK_{AB}, CLK_{BA} set-up and hold times, clock CLK_{AB}, CLK_{BA} pulse width, maximum clock pulse frequency and the CLK_{AB}, CLK_{BA} to output B_n, A_n propagation delays.

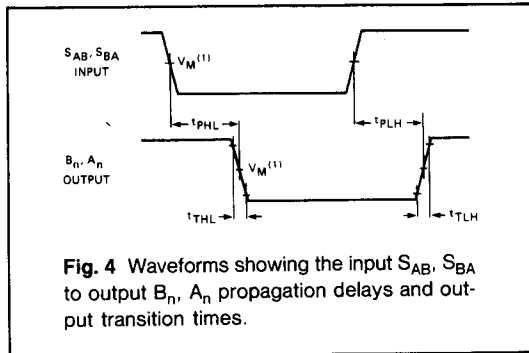


Fig. 4 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delays and output transition times.

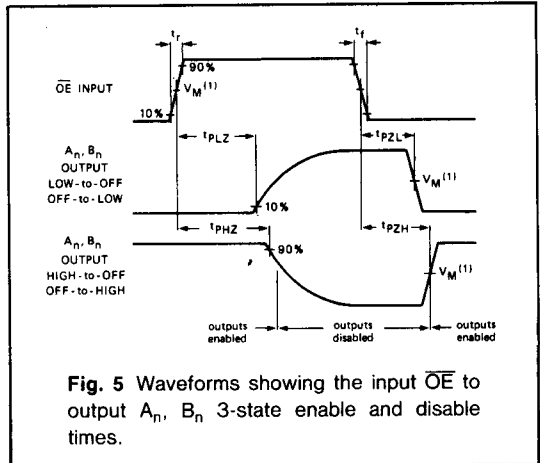


Fig. 5 Waveforms showing the input OE to output A_n, B_n 3-state enable and disable times.

Note to AC waveforms

- (1) HC : V_M=50%; V_I=GND to V_{CC}.
- HCT : V_M=1.3V; V_I=GND to 3V.

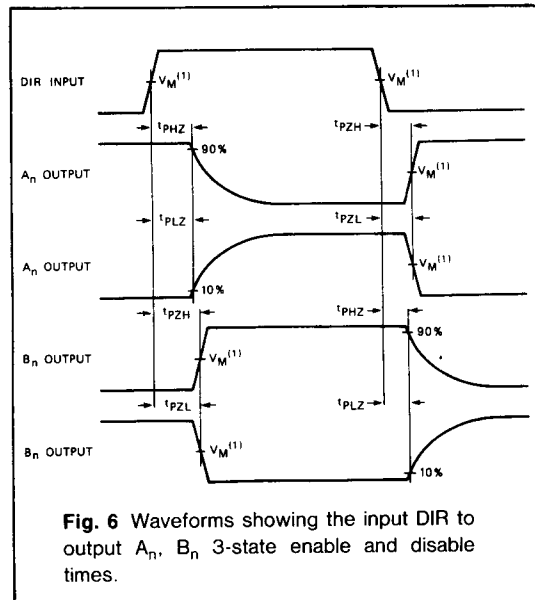


Fig. 6 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.