2GB – 512M x 32/40 DDR3 SDRAM 1.35V – 136/204 PBGA Multi-Chip Package

FEATURES

- DDR3 Data Rate = 800, 1,066, 1333 Mb/s
- Packages:
  - 136 PBGA, 204 PBGA 10 x 14.5mm
  - 0.8mm pitch
- Supply Voltage = 1.35V
- Center terminated push/pull I/O
- Differential bidirectional data strobe
- Differential clock inputs (CK, CK#)
- 8n-bit prefetch architecture
- Eight internal banks
- Fixed Burst length (BL) of 8 and Burst Chop (BC) of 4
- Selectable BC4 or BL8 on-the-fly (OTF)
- Auto Refresh and Self Refresh Modes
- Nominal and dynamic On Die Termination (ODT)
- Programmable CAS read latency (CL)
- Posted CAS additive latency
- Write leveling
- Programmable CAS write latency (CWL) based on t_{CK}
- Commercial, industrial and military** temperature ranges
- Organized as 1 rank of 512M x 32 or 512M x40
- 1.5V option available in same packages.
  Refer to W3J512M32/40G data sheet.
- W3J512M32K-XBX is footprint compatible with Micron® M41K256M32 device.

Micron© is a registered trademark of Micron Technology, Inc.

BENEFITS

- 74% Space savings vs. FBGA
- Reduced part count
- 48% I/O reduction vs. FBGA
- Optional:
  - Address/control terminations
- Differential clock terminations (not populated in XBX package)
- Output drive calibration resistors (RZQ)
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications
- Enhanced thermal management

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

** Contact factory for availability.

TYPICAL APPLICATION

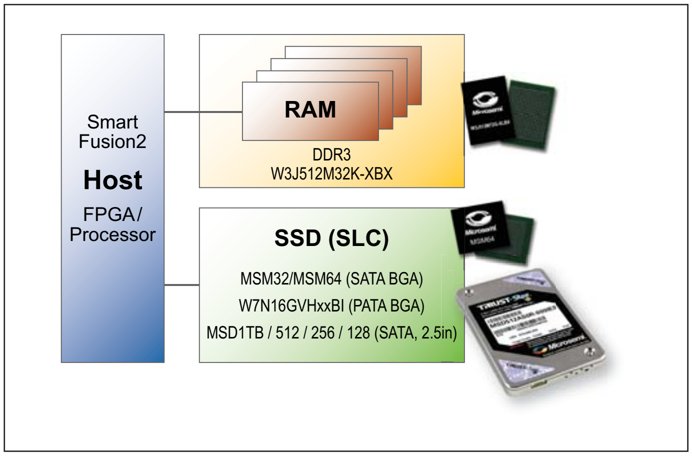
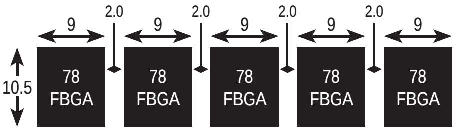
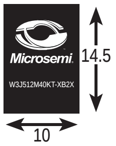
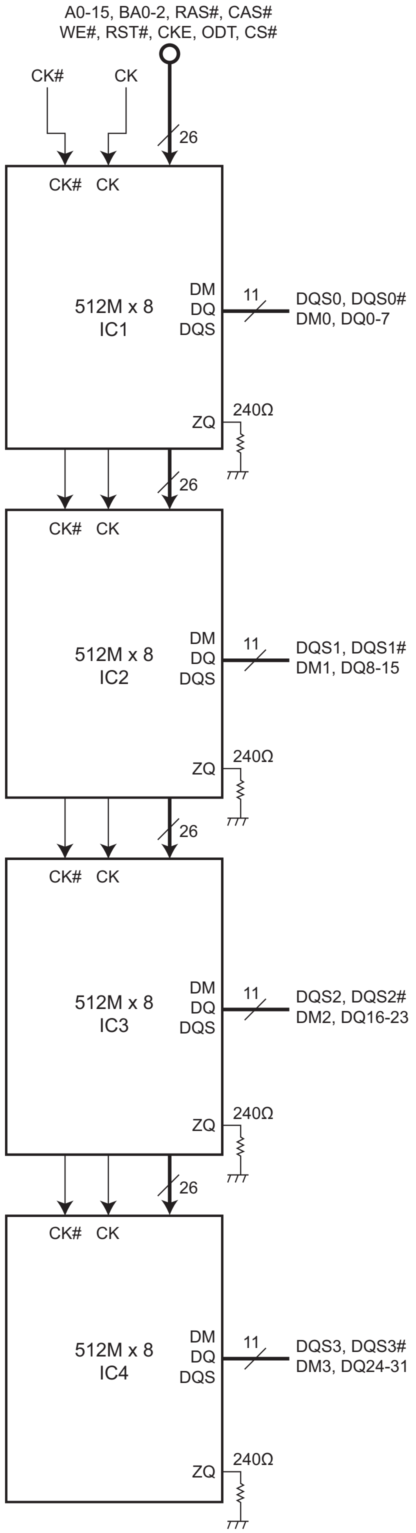


FIGURE 1 – DENSITY COMPARISONS

	CSP Approach (mm)  	W3J512M40KT-XB3X  	SAVINGS
Area	556.5 mm^2	145 mm^2	74%***
I/O Count	5 x 78 balls = 390 balls	204 Balls	48%

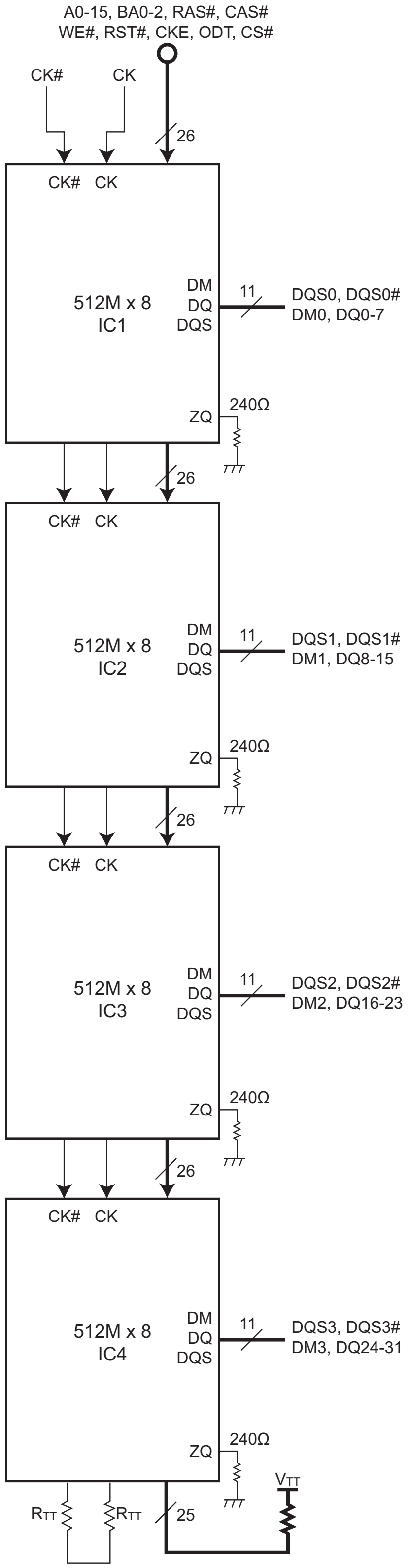
*** not including terminations

FIGURE 2A – FUNCTIONAL BLOCK DIAGRAM FOR W3J512M32K-XBX



NOTES: Block diagram shows actual fly-by order.
Calibration resistors (RZQ) are included.

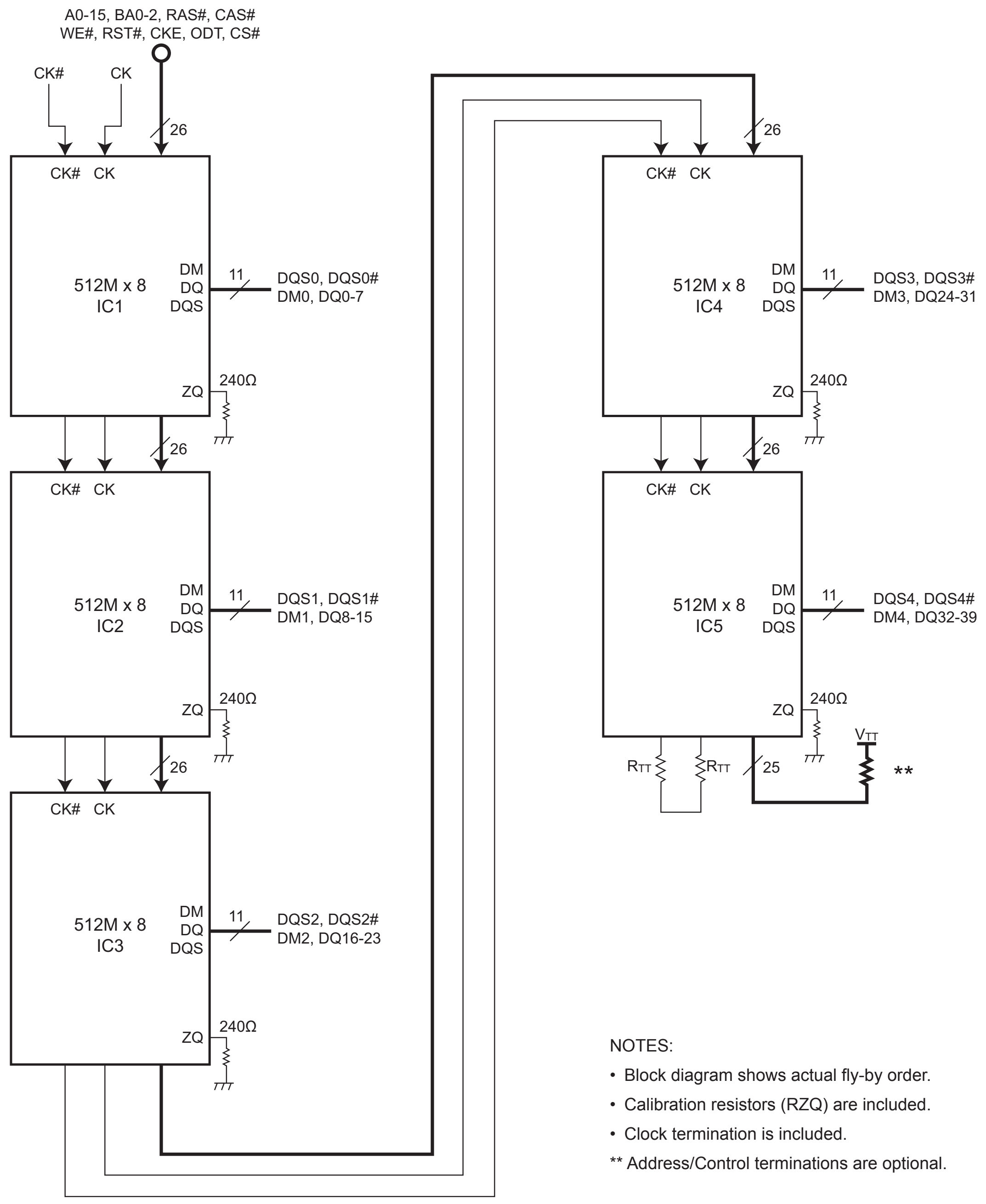
FIGURE 2B – FUNCTIONAL BLOCK DIAGRAM FOR W3J512M32KT-XB2X



NOTES:

- Block diagram shows actual fly-by order.
- Calibration resistors (RZQ) are included.
- Clock termination is included.
- Address/Control terminations are included.

FIGURE 2D – FUNCTIONAL BLOCK DIAGRAM FOR W3J512M40K(T)-XB3X



NOTES:
- Block diagram shows actual fly-by order.
- Calibration resistors (RZQ) are included.
- Clock termination is included.

** Address/Control terminations are optional.

FIGURE 3 – 136 PBGA (XBX) PIN CONFIGURATION

TOP VIEW

	1	2	3	4	9	10	11	12	
A	VCC	GND	GND	DQ1	DQ9	GND	GND	VCC	A
B	VCC	DQ0	GND	DQ3	DQ11	GND	DQ8	VCC	B
C	VCC	DQ2	GND	DM0	DM1	GND	DQ10	VCC	C
D	GND	VCC	DQS0	DQS0#	DQS1#	DQS1	VCC	GND	D
E	GND	DQ4	VCC	DQ5	DQ13	VCC	DQ12	GND	E
F	GND	DQ6	VCC	DQ7	DQ15	VCC	DQ14	GND	F
G	VCC	NC	CAS#	RAS#	CK	CK#	CKE	VCC	G
H	RST#	BA2	ODT	CS#	A10	A14	A15	NC	H
J	VREFDQ	GND	NC	WE#	A1	NC	GND	VREFCA	J
K	BA0	A9	A2	A0	A4	A6	A12	BA1	K
L	VCC	A7	A5	A3	A8	A11	A13	VCC	L
M	GND	DQ24	VCC	DQ25	DQ17	VCC	DQ16	GND	M
N	GND	DQ26	VCC	DQ27	DQ19	VCC	DQ18	GND	N
P	GND	VCC	DQS3	DQS3#	DQS2#	DQS2	VCC	GND	P
R	VCC	DQ28	GND	DM3	DM2	GND	DQ20	VCC	R
T	VCC	DQ30	GND	DQ29	DQ21	GND	DQ22	VCC	T
U	VCC	GND	GND	DQ31	DQ23	GND	GND	VCC	U
	1	2	3	4	9	10	11	12	

NOTE: Calibration resistors (RZQ) are included inside the package.

FIGURE 3A – 204 PBGA PIN CONFIGURATION (XB2X & XB3X)

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	
A	V_{CC}	GND	GND	DQ1	V_{CC}	V_{TT}**	V_{TT}**	V_{CC}	DQ9	GND	GND	V_{CC}	A
B	V_{CC}	DQ0	GND	DQ3	GND	V_{TT}**	V_{TT}**	GND	DQ11	GND	DQ8	V_{CC}	B
C	V_{CC}	DQ2	GND	DM0	GND	V_{TT}**	NC	GND	DM1	GND	DQ10	V_{CC}	C
D	GND	V_{CC}	DQS0	DQS0#	V_{CC}	DQ32*	DQ35*	V_{CC}	DQS1#	DQS1	V_{CC}	GND	D
E	GND	DQ4	V_{CC}	DQ5	V_{CC}	DQ34*	DQ33*	V_{CC}	DQ13	V_{CC}	DQ12	GND	E
F	GND	DQ6	V_{CC}	DQ7	GND	DM4*	NC	GND	DQ15	V_{CC}	DQ14	GND	F
G	V_{CC}	NC	CAS#	RAS#	GND	DQS4*	DQS4#*	GND	CK	CK#	CKE	V_{CC}	G
H	RST#	BA2	ODT	CS#	V_{CC}	DQ37*	DQ38*	V_{CC}	A10	A14	A15	NC	H
J	V_{REFDQ}	GND	NC	WE#	V_{CC}	DQ39*	DQ36*	V_{CC}	A1	NC	GND	V_{REFCA}	J
K	BA0	A9	A2	A0	GND	NC	NC	GND	A4	A6	A12	BA1	K
L	V_{CC}	A7	A5	A3	GND	NC	V_{CC}	GND	A8	A11	A13	V_{CC}	L
M	GND	DQ24	V_{CC}	DQ25	V_{CC}	GND	GND	V_{CC}	DQ17	V_{CC}	DQ16	GND	M
N	GND	DQ26	V_{CC}	DQ27	V_{CC}	GND	GND	V_{CC}	DQ19	V_{CC}	DQ18	GND	N
P	GND	V_{CC}	DQS3	DQS3#	GND	V_{CC}	V_{CC}	GND	DQS2#	DQS2	V_{CC}	GND	P
R	V_{CC}	DQ28	GND	DM3	GND	V_{CC}	V_{CC}	GND	DM2	GND	DQ20	V_{CC}	R
T	V_{CC}	DQ30	GND	DQ29	V_{CC}	GND	GND	V_{CC}	DQ21	GND	DQ22	V_{CC}	T
U	V_{CC}	GND	GND	DQ31	V_{CC}	GND	GND	V_{CC}	DQ23	GND	GND	V_{CC}	U
	1	2	3	4	5	6	7	8	9	10	11	12	

NOTE: Calibration resistors (RZQ) are included inside the package.
* DQ32-39, DM4, DQS4, DQS4# are NC in x32-bit data configuration
** V_{TT} is only used with address/control terminations option

TABLE 1 – BALL DESCRIPTIONS

Symbol	Type	Description
ODT	Input	On-Die termination: ODT (registered HIGH) enables and (registered LOW) disables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQS and DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REF}CA.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# is considered part of the command code. CS# is referenced to V_{REFCA}
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}
DM0-7	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REF}DQ.
BA0–BA2	Input	Bank address inputs: BA0–BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register including (MR, MR0, MR1, MR2, MR3) is loaded during the LOAD MODE command. BA0-2 are referenced to V_{REFCA}
RST#	Input	Reset = RST# or RESET# is an active low CMOS input referenced to V_{SS}. The RST# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 x V_{CCQ} and DC LOW ≤ 0.2 x V_{CCQ}. RST# assertion and desertion are asynchronous
A0-A15	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REF}CA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop).
DQ0-X	I/O	Data input/output: Bidirectional data bus. DQs are referenced to V_{REF}DQ.
DQS0-X, DQS0-X#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
V_{CC}	Supply	Single Power Supply – V_{CC} and V_{CCQ} are internally tied together
V_{TT}	Supply	Termination supply
V_{REF}CA	Supply	Reference voltage for control, command, and address. V_{REF}CA must be maintained at all times (including self refresh) for proper device operation.
V_{REF}DQ	Supply	Reference voltage for data. V_{REF}DQ must be maintained at all times (including self refresh) for proper device operation.
GND	Supply	Ground.
NC	-	No connect: These balls should be left unconnected.
DNU	-	Future use

DESCRIPTION

The 2GB DDR3 SDRAM is a high-speed CMOS, dynamic random-access memory containing 4 or 5 4Gb, (4,294,967,296) bit chips. Each of the 4 or 5 chips in the MCP are internally configured as 8-bank DRAM. The block diagram of the device is shown in Figure 2. Ball assignments and are shown in Figure 3.

The 2GB DDR3 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is a 8*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 2GB DDR3 SDRAM consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is center-aligned with data for writes. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The 2GB DDR3 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered in the first rising edge of "DQS" after the "WRITE" preamble, and output data is referenced on the first rising edge of "DQS" after the "READ" preamble.

Read and write accesses to the DDR3 SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

DDR3 SDRAM use "READ" and "WRITE" BL8 and "BC4" An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR3 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

GENERAL NOTES

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation. (normal operation)
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered illegal, and not supported and can result in unknown operations.

INITIALIZATION

DDR3 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for power up and initialization and is shown in Figure 4.

1. Applying power; RST# is recommended to be below 0.2 x V_{CCQ} during power ramp to ensure the outputs remain disabled. (HIGH-Z) and ODT off (R_{TT} is also HIGH-Z). All other inputs, including ODT, may be undefined.

   During power up, either of the following conditions may exist and must be met:

   Condition A:

   - V_{CC} and V_{CCQ} are driven from a single-power converter output and are ramped with a maximum delta voltage between them of $\Delta V \leq 300mV$. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than V_{CC}, V_{CCQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{CCQ} and V_{CC} on one side, and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
   - Both V_{CC} and V_{CCQ} power supplies ramp to V_{CC} (MIN) and V_{CCQC} (MIN) within t_{VDDPR} = 200ms.
   - V_{REFDQ} tracks V_{CC} × 0.5, V_{REFCA} tracks V_{CC} × 0.5.
   - V_{TT} is limited to 0.875V when the power ramp is complete and is not applied directly to the DRAM components; however, t_{VTD} should be greater than or equal to zero to avoid device latchup.

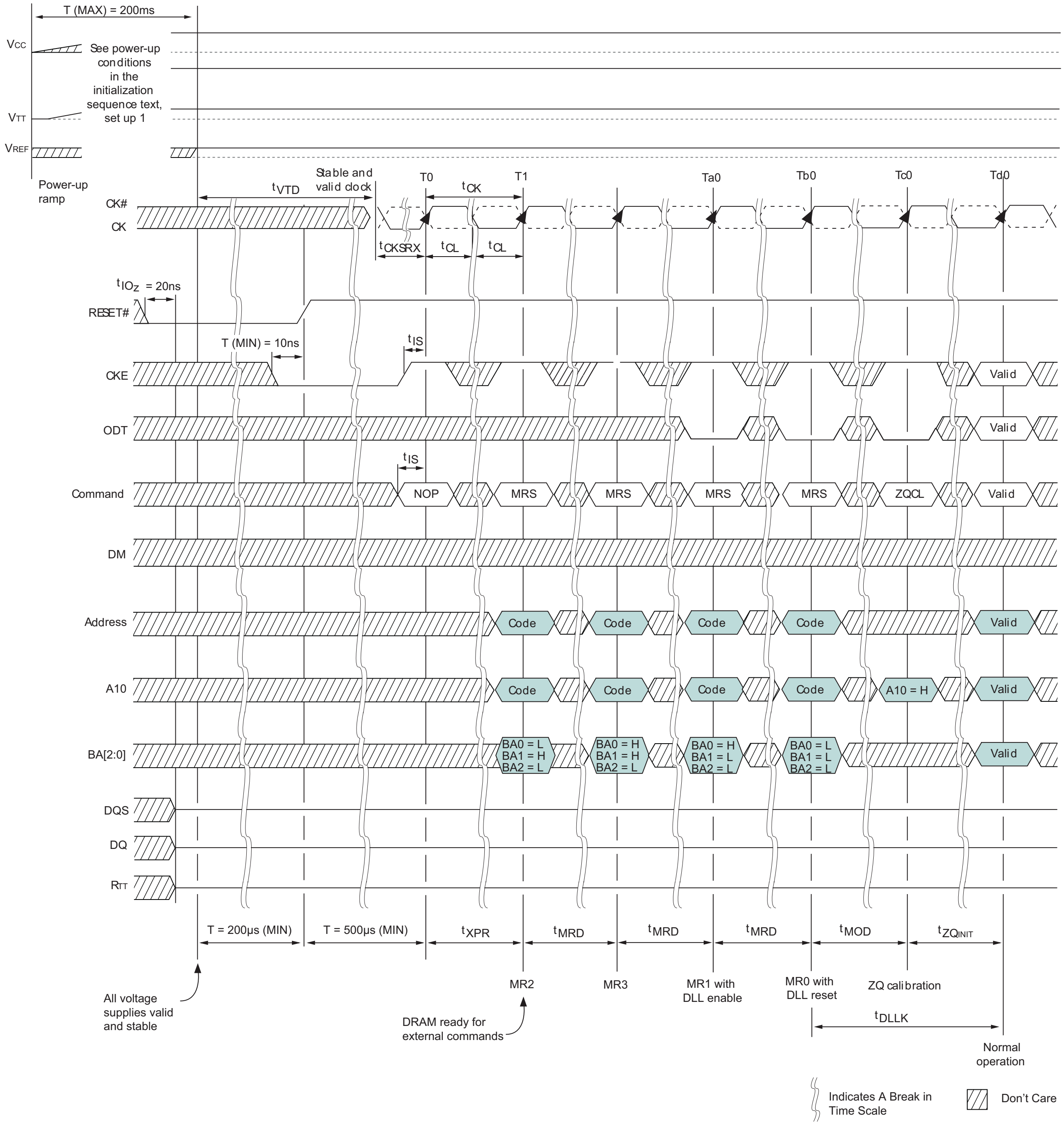
   Condition B:

   - Vcc may be applied before or at the same time as V_{CCQ}.
   - V_{CCQ} may be applied before or at the same time as V_{TT}, V_{REF}DQ, and V_{REF}CA.
   - No slope reversals are allowed in the power supply ramp for this condition.

2. Until stable power, maintain RST# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RST# must be LOW for at least 200µs to begin the initialization process. ODT will remain in the High-Z state while RST# is LOW and until CKE is registered HIGH.
3. CKE must be LOW 10ns prior to RST# transitioning HIGH.
4. After RST# transitions HIGH, wait 500µs (minus one clock) with CKE LOW.
5. After this CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least t_{IS} prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.
6. After CKE is registered HIGH and after t_{XPR} has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).
7. Issue an MRS command to MR3 with the applicable settings.
8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.
9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. t_{DLLK} (512) cycles of clock input are required to lock the DLL.
10. Issue a Z_{QCL} command to calibrate RTT and RON values for the process voltage temperature (PVT). Prior to normal operation, t_{ZQINIT} must be satisfied.
11. When t_{DLLK} and t_{ZQINIT} have been satisfied, the DDR3 SDRAM will be ready for normal operation.

FIGURE 4 – POWER-UP AND INITIALIZATION

Notes appear on page 6



MODE REGISTERS

Mode registers (MR0–MR3) are used to define various modes of programmable operations of the DDR3 SDRAM. A mode register is programmed via the MODE REGISTER SET (MRS) command during initialization, and it retains the stored information (except for MR0[8] which is self-clearing) until it is either reprogrammed, RESET# goes LOW, or until the device loses power. Contents of a mode register can be altered by re-executing the MRS command. If the user chooses to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly. The MRS command can only be issued (or reissued) when all banks are idle and in the precharged state (t_{RP} is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: t_{MRD} and t_{MOD}. The controller must wait t_{MRD} before initiating any subsequent MRS commands The controller must also wait t_{MOD} before initiating any non MRS commands (excluding NOP and DES). The DRAM requires t_{MOD} in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until t_{MOD} has been satisfied, the updated features are to be assumed unavailable.

MODE REGISTER 0 (MR0)

The base register, MR0, is used to define various DDR3 SDRAM modes of operations. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and precharge power-down mode.

BURST LENGTH

Burst length is defined by MR0[1: 0]. (see figure 9) Read and write accesses to the DDR3 SDRAM are burst-oriented, with the burst length being programmable to “4” (chop mode), “8” (fixed), or selectable using A12 during a READ/WRITE command (on-the-fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to “01” during a READ/WRITE command, if A12 = 0, then BC4 (chop) mode is selected. If A12 = 1, then BL8 mode is selected. Specific timing diagrams, and turnaround between READ/WRITE, are shown in the READ/WRITE sections of this document. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[i:2] when the burst length is set to “4” and by A[i:3] when the burst length is set to “8” (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

BURST TYPE

Accesses within a given burst may be programmed to either a sequential or an interleaved order. The burst type is selected via MR0[3], as shown in Figure 6. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 4. DDR3 only supports 4-bit burst chop and 8-bit burst access modes. Full interleave address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word (BL8) boundaries.

DLL RESET

DLL RESET is defined by MR0[8] (see Figure 6). Programming MR0[8] to “1” activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of “0” after the DLL RESET function has been initiated. Anytime the DLL RESET function is initiated, CKE must be HIGH and the clock held stable for 512 (t_{DLLK}) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in invalid output timing specifications, such as t_{DQSCK} timings.

WRITE RECOVERY

WRITE recovery time is defined by MR0[11:9] (see Figure 6). Write recovery values of 5, 6, 7, 8, 10, 12 or 14 may be used by programming MR0[11:9]. The user is required to program the correct value of write recovery and is calculated by dividing t_{WR} (ns) by t_{CK} (ns) and rounding up a non integer value to the next integer: WR (cycles) = roundup (t_{WR} [ns]/t_{CK} [ns]).

PRECHARGE POWER-DOWN (PRECHARGE PD)

The precharge PD bit applies only when precharge power-down mode is being used. When MR0[12] is set to “0,” the DLL is off during precharge power-down providing a lower standby current mode; however, t_{XPDLL} must be satisfied when exiting. When MR0[12] is set to “1,” the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode; however, t_{XP} must be satisfied when exiting.

CAS LATENCY (CL)

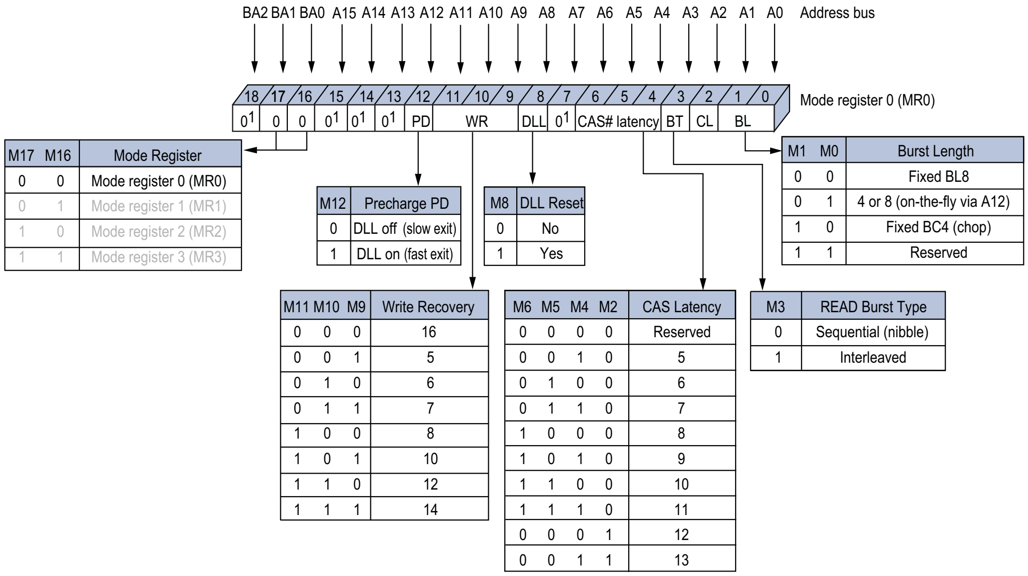
The CAS latency (CL) is defined by MR0[6:4], as shown in Figure 6. CL is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The CL can be set to 5, 6, 7, 8, 9, 10, 11, 12, or 13. DDR3 SDRAM does not support any half-clock latencies.

MODE REGISTER 1 (MR1)

The mode register 1 (MR1) controls additional functions and features not available in the other mode registers: Q OFF (OUTPUT DISABLE), TDQS (for the x8 configuration only, DLL ENABLE/DLL DISABLE, R_{TT_NOM} value (ODT), WRITE LEVELING, POSTED CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. These functions are controlled via the bits shown in Figure 8. The MR1 register is programmed via the MRS command and retains the stored informations until it is reprogrammed, until RESET# goes LOW, or until the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is performed correctly.

continued on page 13

FIGURE 6 – MODE REGISTER 0 (MR0) DEFINITIONS



M17	M16	Mode Register
0	0	Mode register 0 (MR0)
0	1	Mode register 1 (MR1)
1	0	Mode register 2 (MR2)
1	1	Mode register 3 (MR3)

M12	Precharge PD
0	DLL off (slow exit)
1	DLL on (fast exit)

M8	DLL Reset
0	No
1	Yes

M1	M0	Burst Length
0	0	Fixed BL8
0	1	4 or 8 (on-the-fly via A12)
1	0	Fixed BC4 (chop)
1	1	Reserved

M11	M10	M9	Write Recovery
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

M6	M5	M4	M2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13

M3	READ Burst Type
0	Sequential (nibble)
1	Interleaved

NOTE: 1. MR0[18, 15:13, 7] are reserved for future use and must be programmed to 0.

TABLE 4 – BURST ORDER

Burst Length	READ/ WRITE	Starting Column Address			Burst		Notes
					Type = Sequential	Type = Interleaved	
4 CHOP	READ	0	0	0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0	0	1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0	1	0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0	1	1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1	0	0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1	0	1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1	1	0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1	1	1	7, 4, 5, 6, Z, Z, Z, Z	7, 6, 5, 4, Z, Z, Z, Z	1, 2
	WRITE	0	V	V	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, X, X, X, X	1, 3, 4
		1	V	V	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, X, X, X, X	1, 3, 4
8	READ	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1	1	0	5, 6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V	V	V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

NOTES:
1. Internal read and write operations start at the same point in time for BC4 as they do for BL8
2. Z = Data strobe output drives are in tri-state
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins
4. X = "Don't care".

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters. t_{MRD} and t_{MOD} before initiating a subsequent operation

DLL ENABLE/DLL DISABLE

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command, as shown in Figure 11. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering SELF REFRESH operation an is automatically reenabled and reset upon exit of SELF REFRESH operation. IF the DLL is disabled prior to entering self refresh mode, the DLL remains disabled even upon exit of SELF REFRESH operation until it is reenabled and reset.

The DRAM is not tested to check-nor does Microsemi warrant compliance with normal mode timings or functionality when the DLL is disabled. An attempt has been made to have the DRAM operate in the normal mode where reasonably possible when the DLL has been disabled; however, by industry standard, a few known exceptions are defined:

1. ODT is not allowed to be used.
2. The output data is no longer edge-aligned to the clock.
3. CL and CWL can only be six clocks.

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled (see "DLL Disable Mode"). Disabling the DLL also implies the need to change the clock frequency.

OUTPUT DRIVE STRENGTH

The DDR3 SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5, 1]. RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for DDR3 SDRAM devices. To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and V_{SSQ}. The value of the resistor must be 240Ω ±1 percent. The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all data sheet timings and current specifications are met during an update.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by MR1[12], as shown in Figure 8. When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS#) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3 SDRAM outputs (DQ and DQS, DQS#) are tri-stated. The output disable feature is intended to be used during I_{CC} characterization of the READ current and during t_{DQSS} margining (write leveling) only.

ON-DIE TERMINATION (ODT)

ODT resistance RTT_NOM is defined by MR1[9, 6, 2] (see Figure 8). The RTT termination value applies to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls. DDR3 supports multiple RTT termination values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240Ω. Unlike DDR2, DDR3 ODT must be turned off prior to reading data out and must remain off during a READ burst. RTT_NOM termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT enabled (RTT_WR) temporarily replaces RTT_NOM with RTT_WR.

The actual effective termination, RTT_EFF, may be different from the RTT targeted due to nonlinearity of the termination.

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT for any or all devices. The ODT input control pin is used to determine when RTT is turned on (ODTL on) and off (ODTL off), assuming ODT has been enabled via MR1[9, 6, 2].

WRITE LEVELING

The WRITE LEVELING function is enabled by MR1[7], as shown in Figure 8. Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, DDR3 SDRAM memory adopted fly-by topology for the commands, addresses, control signals, and clocks.

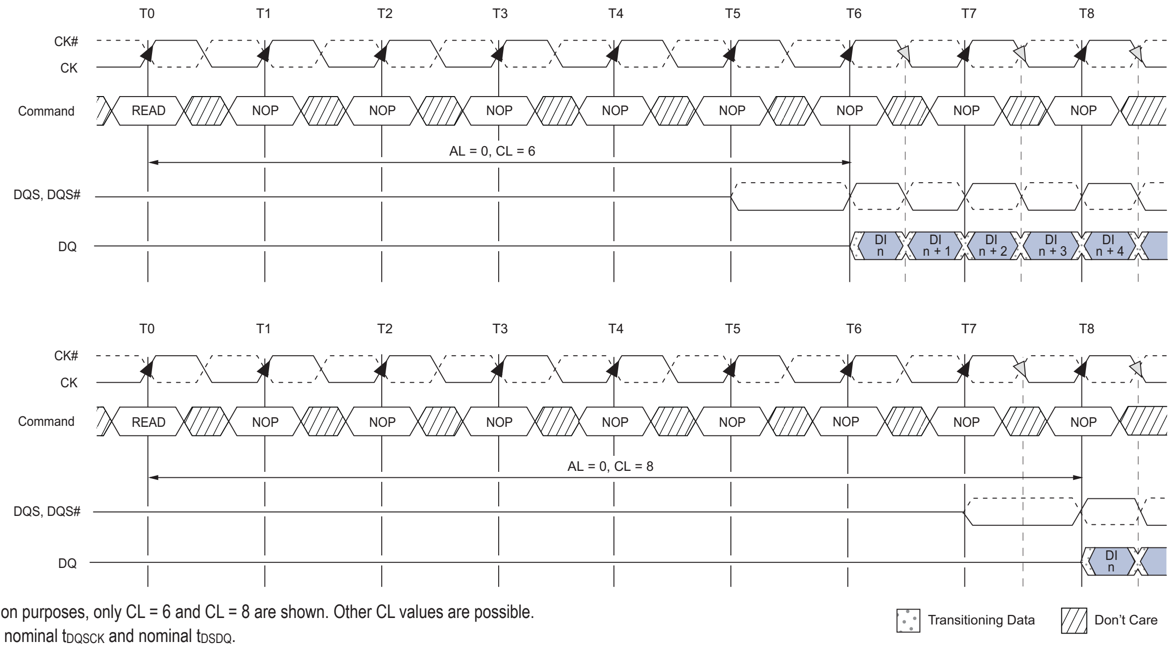
The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM. Controllers will have a difficult time maintaining t_{DQSS}, t_{DSS}, and t_{DSH} specifications without supporting write leveling in systems which use fly-by topology-based designs.

POSTED CAS ADDITIVE LATENCY (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. MR1 [4, 3] define the value of AL, as shown in Figure 8. MR1 [4, 3] enable the user to program the DDR3 SDRAM with an Al = 0, CL-1 or CL -2.

With this feature, the DDR3 SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to t_{RCD} (MIN). The only restriction is ACTIVATE to READ or WRITE + AL ≥ t_{RCD} (MIN) must be satisfied. Assuming t_{RCD} (MIN) = CL, a typical application using this feature sets AL = CL - 1t_{CK} = t_{RCD} (MIN) - 1 t_{CK}. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3 SDRAM device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL), RL = AL + CL. WRITE latency (WL) is the sum of CAS WRITE latency and AL, WL = AL + CWL.

FIGURE 7 – READ LATENCY



NOTES:

1. For illustration purposes, only CL = 6 and CL = 8 are shown. Other CL values are possible.
2. Shown with nominal t_{DQSCK} and nominal t_{DSDQ}.

MODE REGISTER 2 (MR2)

The mode register 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT (R_{TT_WR}). These functions are controlled via the bits shown in Figure 10. The MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is performed correctly. The MR2 register must be loaded when all banks are idle and not data bursts are in progress, and the controller must wait the specified time t_{MRD} and t_{MOD} before initiating a subsequent operation.

CAS WRITE LATENCY (CWL)

CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency (see Figure 10). The overall WRITE latency (WL) is equal to CWL + AL (Figure 11)

AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to disable/enable the ASR function.

When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the maximum temperature of 85°C (sometimes referred to as 1X refresh rate). In the disabled mode, ASR requires the user to ensure the DRAM never exceeds a temperature of 85°C while in self refresh unless the user enables the SRT feature listed below when temperature is between 85°C and 95°C.

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1X to 2X when temperature exceeds 85°C. This enables the user to operate the DRAM beyond the 85°C temperature limit up to 95°C for military grade devices while in self refresh mode.

SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode's refresh rate is assumed to be at the 85°C max temperature (sometimes referred to as 1X refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a temperature of 85°C while in self refresh mode unless the user enables ASR.

When SRT is enabled, the DRAM self refresh is changed internally from 1X to 2X, regardless of the temperature. This enables the user to operate the DRAM beyond 85°C up to 95°C while in self refresh mode. The standard self refresh current test specifies test conditions to 85°C only, meaning if SRT is enabled, the standard self refresh current specifications do not apply.

SRT vs. ASR

If the temperature limit of 85°C is not exceeded then neither SRT nor ASR is required, and both can be disabled throughout operation. However, if the temperature exceeds 85°C (but lower than 95°C), the user is required to provide a 2X refresh rate during (manual) refresh and to enable either the SRT or the ASR to ensure self refresh is performed at the 2X rate. Beyond 95°C , neither SRT or ASR are functional and user is required to provide 4X refresh rate using (manual) refresh commands.

SRT forces the DRAM to switch the internal self refresh rate from 1X to 2X. Self refresh is performed at the 2X refresh rate regardless of the temperature.

ASR automatically switches the DRAM's internal self refresh rate from 1X to 2X. However, while in self refresh mode, ASR enables the refresh rate to automatically adjust between 1X to 2X over the supported temperature range. One other disadvantage with ASR is the DRAM cannot always switch from a 1X to a 2X refresh rate at an exact temperature of 85°C. Although the DRAM will support data integrity when it switches from a 1X to a 2X refresh rate, it may switch at a lower temperature than 85°C. Since only one mode is necessary, SRT and ASR cannot be enabled at the same time.

For military grade devices (max temperature of +125°C), it is recommended to use manual 4X refresh rate.

DYNAMIC ODT

The dynamic ODT (RTT_WR) feature is defined by MR2[10, 9]. Dynamic ODT is enabled when a value is selected. This new DDR3 SDRAM feature enables the ODT termination value to change without issuing an MRS command, essentially changing the ODT termination "on-the-fly."

With dynamic ODT (RTT_WR) enabled, the DRAM switches from normal ODT (RTT_NOM) to dynamic ODT (RTT_WR) when beginning a WRITE burst and subsequently switches back to ODT (RTT_NOM) at the completion of the WRITE burst. If RTT_NOM is disabled, the RTT_NOM value will be High-Z. Special timing parameters must be adhered to when dynamic ODT (RTT_WR) is enabled: ODTLCNW, ODTLCNW4, ODTLCNW8, ODTH4, ODTH8, and t_{ADC}.

Dynamic ODT is only applicable during WRITE cycles. If ODT (RTT_NOM) is disabled, dynamic ODT (RTT_WR) is still permitted. RTT_NOM and RTT_WR can be used independent of one other. Dynamic ODT is not available during write leveling mode, regardless of the state of ODT (RTT_NOM).

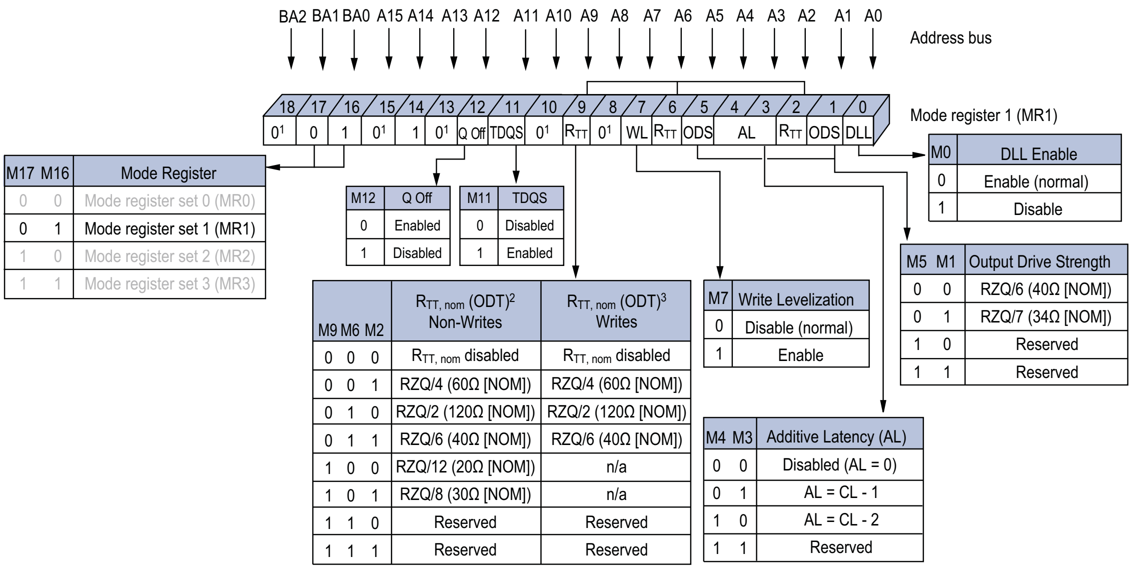
MODE REGISTER 3 (MR3)

The mode register 3 (MR3) controls additional functions and features not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits shown in Figure 12. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time t_{MRD} and t_{MOD} before initiating a subsequent operation.

MULTIPURPOSE REGISTER (MPR)

The MULTIPURPOSE REGISTER function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register, and bits 1 and 0 determine which mode the MPR is placed in. The basic concept of the multipurpose register is shown in Figure 13.

FIGURE 8 – MODE REGISTER 1 (MR1) DEFINITION



M17	M16	Mode Register
0	0	Mode register set 0 (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M12	Q Off
0	Enabled
1	Disabled

M11	TDQS
0	Disabled
1	Enabled

M0	DLL Enable
0	Enable (normal)
1	Disable

M5	M1	Output Drive Strength
0	0	RZQ/6 (40Ω [NOM])
0	1	RZQ/7 (34Ω [NOM])
1	0	Reserved
1	1	Reserved

M9	M6	M2	$R_{TT, nom}$ (ODT)[2] Non-Writes	$R_{TT, nom}$ (ODT)[3] Writes
0	0	0	$R_{TT, nom}$ disabled	$R_{TT, nom}$ disabled
0	0	1	RZQ/4 (60Ω [NOM])	RZQ/4 (60Ω [NOM])
0	1	0	RZQ/2 (120Ω [NOM])	RZQ/2 (120Ω [NOM])
0	1	1	RZQ/6 (40Ω [NOM])	RZQ/6 (40Ω [NOM])
1	0	0	RZQ/12 (20Ω [NOM])	n/a
1	0	1	RZQ/8 (30Ω [NOM])	n/a
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

M7	Write Levelization
0	Disable (normal)
1	Enable

M4	M3	Additive Latency (AL)
0	0	Disabled (AL = 0)
0	1	AL = CL - 1
1	0	AL = CL - 2
1	1	Reserved

NOTES:

1. R1[18, 15:13, 10, 8] are reserved for future use and must be programmed to 0.
2. During write leveling, if MR1[7] and MR1[12] are 1, then all $R_{TT, nom}$ values are available for use.
3. During write leveling, if MR1[7] is a 1, but MR1[12] is a 0, then only $R_{TT, nom}$ write values are available for use.

If MR3[2] is a "0," then the MPR access is disabled, and the DRAM operates in normal mode. However, if MR3[2] is a "1," then the DRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0, 1]. If MR3[0, 1] is equal to "00," then a predefined read pattern for system calibration is selected.

To enable the MPR, the MRS command is issued to MR3, and MR3[2] = 1 (see Table 5). Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged, and t_{RP} is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when either a READ or a RDAP command is issued, is defined by MR3[1:0] when the MPR is enabled (see Table 6). When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2] = 0). Power-down mode, self refresh, and any other nonREAD/RDAP command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

MPR FUNCTIONAL DESCRIPTION

The MPR JEDEC definition enables either a prime DQ (DQ0 on a x4 and a x8; on a x16, DQ0 = lower byte and DQ8 = upper byte) to output the MPR data with the remaining DQs driven LOW, or for all DQs to output the MPR data . The MPR readout supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable, provided the DLL is locked as required.

MPR addressing for a valid MPR read is as follows:

- A[1:0] must be set to "00" as the burst order is fixed per nibble
- A2 selects the burst order:
  - BL8, A2 is set to "0," and the burst order is fixed to 0, 1, 2, 3, 4, 5, 6, 7
- For burst chop 4 cases, the burst order is switched on the nibble base and:
  - A2 = 0; burst order = 0, 1, 2, 3
  - A2 = 1; burst order = 4, 5, 6, 7
- Burst order bit 0 (the first bit) is assigned to LSB, and burst order bit 7 (the last bit) is assigned to MSB
- A[9:3] are a "Don't Care"
- A10 is a "Don't Care"
- A11 is a "Don't Care"
- A12: Selects burst chop mode on-the-fly, if enabled within MR0
- A13 is a "Don't Care"
- BA[2:0] are a "Don't Care"

DESELECT (DES)

The DES command (CS# HIGH) prevents new commands from being executed by the DRAM. Operations already in progress are not affected.

NO OPERATION (NOP)

The NOP command (CS# LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

ZQ CALIBRATION

ZQ CALIBRATION LONG (ZQCL)

The ZQCL command is used to perform the initial calibration during a power-up initialization and reset sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated RON and ODT values.

The DRAM is allowed a timing window defined by either t_{ZQINIT} or t_{ZQOPER} to perform the full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter t_{ZQINIT} must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter t_{ZQOPER} to be satisfied.

ZQ CALIBRATION SHORT (ZQCS)

The ZQCS command is used to perform periodic calibrations to account for small voltage and temperature variations. The shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter t_{ZQCS}. A ZQCS command can effectively correct a minimum of 0.5 percent RON and RTT impedance error within 64 clock cycles, assuming the maximum sensitivities.

ACTIVATE

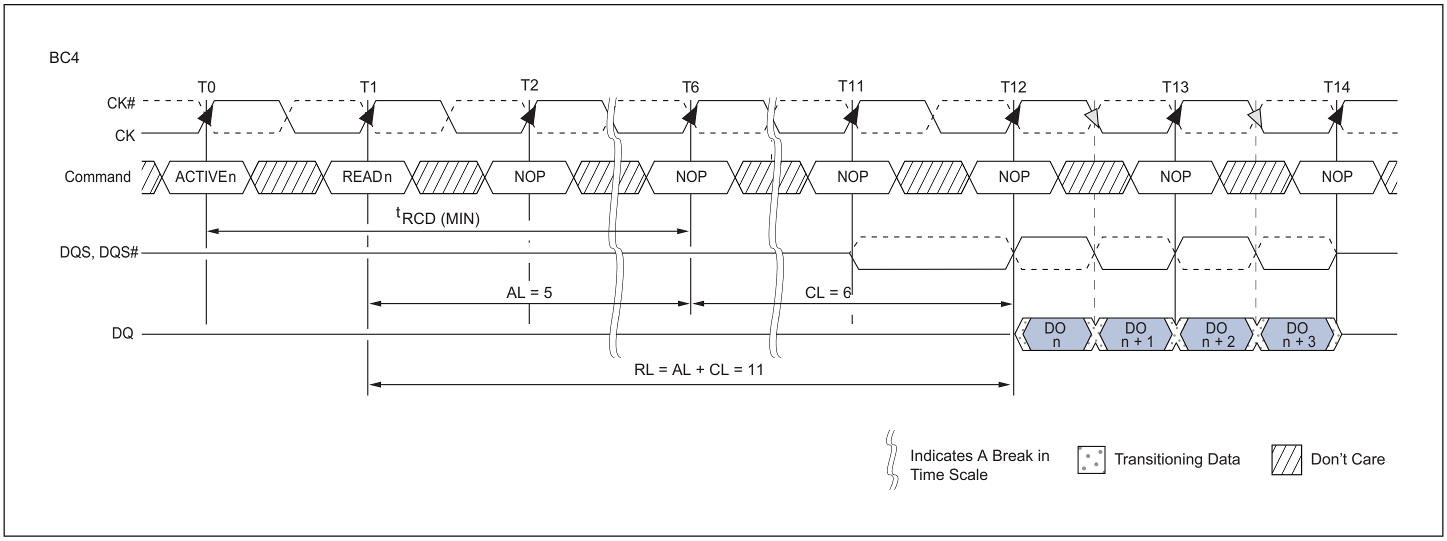
The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[n:0] selects the row. This row remains open (or active) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The address provided on inputs A[2:0] selects the starting column address depending on the burst length and burst type selected. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. The value on input A12 (if enabled in the mode register) when the READ command is issued determines whether BC4 (chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted. A summary of READ commands is shown in Table 9.

FIGURE 9 – READ LATENCY (AL = 5, CL = 6)



WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether or not auto precharge is used. The value on input A12 (if enabled in the MR) when the WRITE command is issued determines whether BC4 (chop) or BL8 is used. The WRITE command summary is shown in Table 10.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or in all banks. The bank(s) are available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued, except in the case of concurrent auto precharge. A READ or WRITE command to a different bank is allowed during concurrent auto precharge as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are precharged. In the case where only one bank is precharged, inputs BA[2:0] select the bank; otherwise, BA[2:0] are treated as “Don’t Care.” After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period is determined by the last PRECHARGE command issued to the bank.

REFRESH

REFRESH is used during normal operation of the DRAM and is analogous to CAS#- before-RAS# (CBR) refresh or auto refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command. The DRAM requires REFRESH cycles at an average interval (t_{REFI}). Refer to “AC Timing Parameters” table for t_{REFI} (MAX) which depends of temperature. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is nine times the maximum average interval refresh rate. The REFRESH period begins when the REFRESH command is registered and ends t_{RFC} (MIN) later.

SELF REFRESH

The SELF REFRESH command is used to retain data in the DRAM, even if the rest of the system is powered down. When in the self refresh mode, the DRAM retains data without external clocking. The self refresh mode is also a convenient method used to enable/disable the DLL (see “DLL Disable Mode”) as well as to change the clock frequency within the allowed synchronous operating range (see “Input Clock Frequency Change”). All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation. For SELF REFRESH limitations see SRT vs ASR on pg. 11.

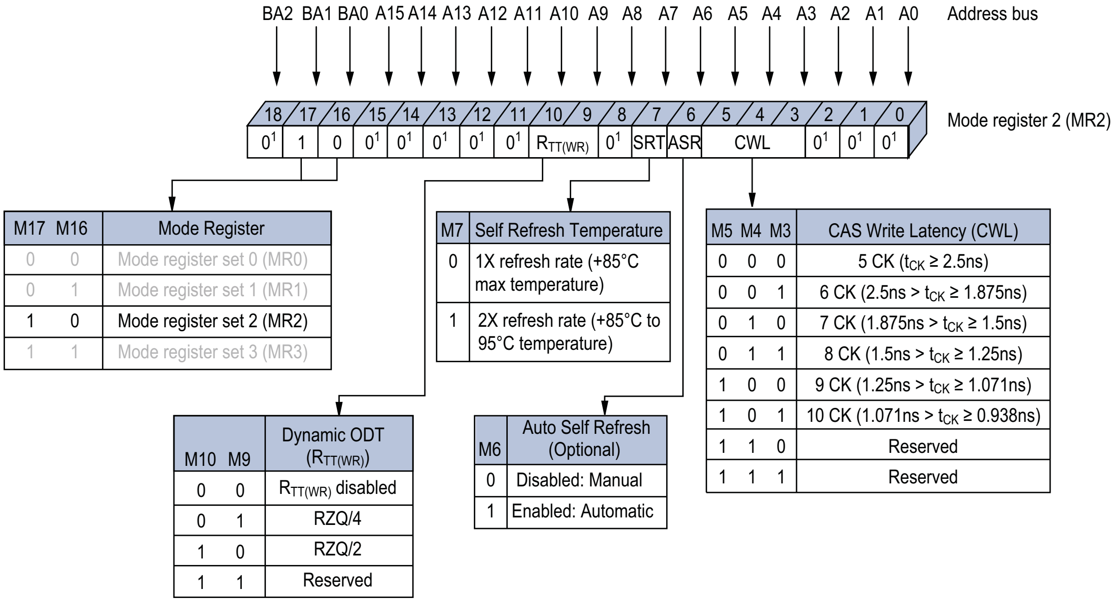
DLL DISABLE MODE

If the DLL is disabled by the mode register (MR1[0] can be switched during initialization or later), the DRAM is targeted, but not guaranteed, to operate similarly to the normal mode with a few notable exceptions:

- The DRAM supports only one value of CAS latency (CL = 6) and one value of CAS WRITE latency (CWL = 6).

continued on page 16

FIGURE 10 – MODE REGISTER 2 (MR2) DEFINITION



M17	M16	Mode Register
0	0	Mode register set 0 (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M7	Self Refresh Temperature
0	1X refresh rate (+85°C max temperature)
1	2X refresh rate (+85°C to 95°C temperature)

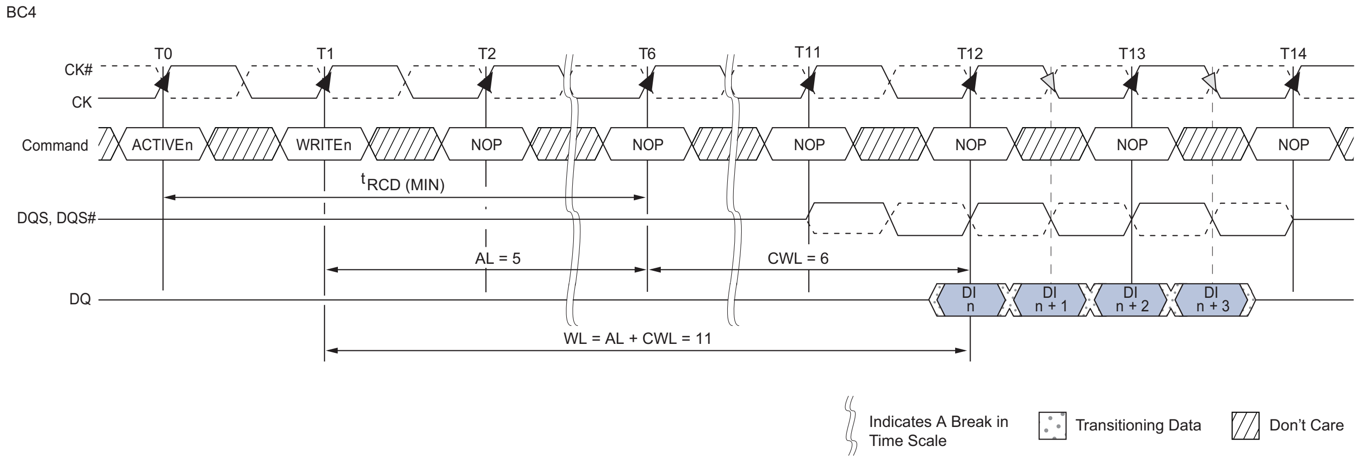
M5	M4	M3	CAS Write Latency (CWL)
0	0	0	5 CK ($t_{CK} \geq 2.5$ns)
0	0	1	6 CK (2.5ns > $t_{CK} \geq 1.875$ns)
0	1	0	7 CK (1.875ns > $t_{CK} \geq 1.5$ns)
0	1	1	8 CK (1.5ns > $t_{CK} \geq 1.25$ns)
1	0	0	9 CK (1.25ns > $t_{CK} \geq 1.071$ns)
1	0	1	10 CK (1.071ns > $t_{CK} \geq 0.938$ns)
1	1	0	Reserved
1	1	1	Reserved

M10	M9	Dynamic ODT ($R_{TT(WR)}$)
0	0	$R_{TT(WR)}$ disabled
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

M6	Auto Self Refresh (Optional)
0	Disabled: Manual
1	Enabled: Automatic

NOTE:
1. MR2[18, 15:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

FIGURE 11 – CAS WRITE LATENCY



- DLL disable mode affects the read data clock-to-data strobe relationship (t_{DQSCK}), but not the read data-to-data strobe relationship (t_{DQSQ}, t_{QH}). Special attention is needed to line the read data up with the controller time domain when the DLL is disabled.
- In normal operation (DLL on), t_{DQSCK} starts from the rising clock edge AL + CL cycles after the READ command. In DLL disable mode, t_{DQSCK} starts AL + CL - 1 cycles after the READ command. Additionally, with the DLL disabled, the value of t_{DQSCK} could be larger than t_{CK}.

The ODT feature is not supported during DLL disable mode (including dynamic ODT). The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming RTT_NOM MR1[9, 6, 2] and RTT_WR MR2[10, 9] to “0” while in the DLL disable mode.

Specific steps must be followed to switch between the DLL enable and DLL disable modes due to a gap in the allowed clock rates between the two modes ($t_{CK\ [AVG]MAX}$ and $t_{CK\ [DLL\ disable]\ MIN}$, respectively). The only time the clock is allowed to cross this clock rate gap is during self refresh mode. Thus, the required procedure for switching from the DLL enable mode to the DLL disable mode is to change frequency during self refresh:

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT_NOM and RTT_WR are High-Z), set MR1[0] to “1” to disable the DLL.
2. Enter self refresh mode after t_{MOD} has been satisfied.
3. After t_{CKSRE} is satisfied, change the frequency to the desired clock rate.
4. Self refresh may be exited when the clock is stable with the new frequency for t_{CKSRX}. After t_{XS} is satisfied, update the mode registers with appropriate values.
5. The DRAM will be ready for its next command in the DLL disable mode after the greater of t_{MRD} or t_{MOD} has been satisfied. A ZQCL command should be issued with appropriate timings met as well.

A similar procedure is required for switching from the DLL disable mode back to the DLL enable mode. This also requires changing the frequency during self refresh mode.

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT_NOM and RTT_WR are High-Z), enter self refresh mode.
2. After t_{CKSRE} is satisfied, change the frequency to the new clock rate.
3. Self refresh may be exited when the clock is stable with the new frequency for t_{CKSRX}. After t_{XS} is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0] to “0” to enable the DLL. Wait t_{MRD}, then set MR0[8] to “1” to enable DLL RESET.
4. After another t_{MRD} delay is satisfied, then update the remaining mode registers with the appropriate values.
5. The DRAM will be ready for its next command in the DLL enable mode after the greater of t_{MRD} or t_{MOD} has been satisfied. However, before applying any command or function requiring a locked DLL, a delay of t_{DLLK} after DLL RESET must be satisfied. A ZQCL command should be issued with the appropriate timings met as well.

The clock frequency range for the DLL disable mode is specified by the parameter t_{CKDLL_DIS}. Due to latency counter and timing restrictions, only CL = 6 and CWL = 6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship (t_{DQSCK}) but not the data strobe to data relationship (t_{DQSQ}, t_{QH}). Special attention is needed to line up read data to the controller time domain.

Compared to the DLL on mode where t_{DQSCK} starts from the rising clock edge AL + CL cycles after the READ command, the DLL disable mode t_{DQSCK} starts AL + CL - 1 cycles after the READ command.

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

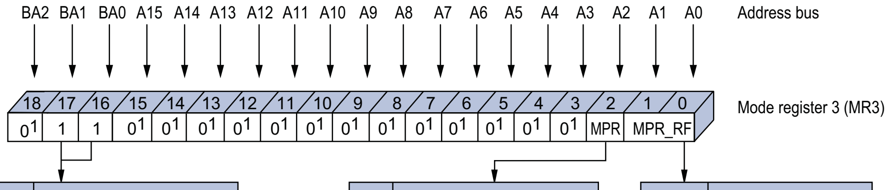
INPUT CLOCK FREQUENCY CHANGE

When the DDR3 SDRAM is initialized, it requires the clock to be stable during most normal states of operation. This means that after the clock frequency has been set to the stable state, the clock period is not allowed to deviate except what is allowed for by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another under two conditions: self refresh mode and precharge power-down mode. Outside of these two modes, it is illegal to change the clock frequency. For the self refresh mode condition, when the DDR3 SDRAM has been successfully placed into self refresh mode and t_{CKSRE} has been satisfied, the state of the clock becomes a “Don’t Care.” When the clock becomes a “Don’t Care,” changing the clock frequency is permissible, provided the new clock frequency is stable prior to t_{CKSRX}. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met.

The precharge power-down mode condition is when the DDR3 SDRAM is in precharge power-down mode (either fast exit mode or slow exit mode). Either ODT must be at a logic LOW or RTT_NOM and RTT_WR must be disabled via MR1 and MR2. This ensures RTT_NOM and RTT_WR are in an off state prior to entering precharge power-down mode, and CKE must be at a logic LOW. A minimum of t_{CKSRE} must occur after CKE goes LOW before the clock frequency can change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade ($t_{CK\ [AVG]MIN}$ to $t_{CK\ [AVG]MAX}$). During the input clock frequency change, CKE must be held at a stable LOW level. When the input clock frequency is changed, a stable clock must be provided to the DRAM t_{CKSRX} before precharge power-down may be exited. After precharge power-down is exited and t_{XP} has been satisfied, the DLL must be reset via the MRS. Depending on the new clock frequency, additional MRS commands may need to be issued. During the DLL lock time, RTT_NOM and RTT_WR must remain in an off state. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

FIGURE 12 – MODE REGISTER 3 (MR3) DEFINITION



M17	M16	Mode Register
0	0	Mode register set (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M2	MPR Enable
0	Normal DRAM operations[2]
1	Dataflow from MPR

M1	M0	MPR READ Function
0	0	Predefined pattern[3]
0	1	Reserved
1	0	Reserved
1	1	Reserved

NOTES:

1. MR3[18 and 15:3] are reserved for future use and must all be programmed to 0.
2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
3. Intended to be used for READ synchronization.

MPR READ PREDEFINED PATTERN

The predetermined read calibration pattern is a fixed pattern of 0, 1, 0, 1, 0, 1, 0, 1. The following is an example of using the read out predetermined read calibration pattern. The example is to perform multiple reads from the multipurpose register in order to do system level read timing calibration based on the predetermined and standardized pattern.

The following protocol outlines the steps used to perform the read calibration:

- Precharge all banks
- After t_{RP} is satisfied, set MRS, MR3[2] = 1 and MR3[1:0] = 00. This redirects all subsequent reads and loads the predefined pattern into the MPR. As soon as t_{MRD} and t_{MOD} are satisfied, the MPR is available
- Data WRITE operations are not allowed until the MPR returns to the normal DRAM state
- Issue a read with burst order information (all other address pins are “Don’t Care”):
  - A[1:0] = 00 (data burst order is fixed starting at nibble)
  - A2 = 0 (for BL8, burst order is fixed as 0, 1, 2, 3, 4, 5, 6, 7)
  - A12 = 1 (use BL8)
- After RL = AL + CL, the DRAM bursts out the predefined read calibration pattern (0, 1, 0, 1, 0, 1, 0, 1)
- The memory controller repeats the calibration reads until read data capture at memory controller is optimized
- After the last MPR READ burst and after t_{MPRR} has been satisfied, issue MRS, MR3[2] = 0, and MR3[1:0] = “Don’t Care” to the normal DRAM state. All subsequent read and write accesses will be regular reads and writes from/to the DRAM array
- When t_{MRD} and t_{MOD} are satisfied from the last MRS, the regular DRAM commands (such as activate a memory bank for regular read or write access) are permitted

MODE REGISTER SET (MRS)

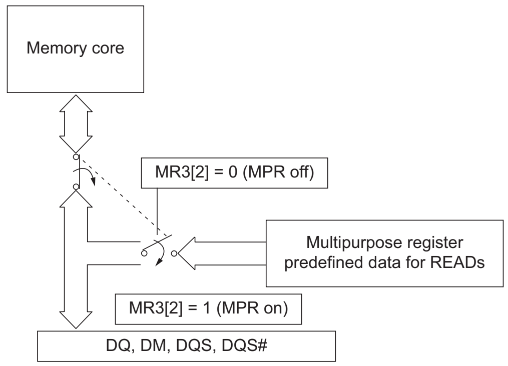
The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determine which mode register is programmed:

- BA2 = 0, BA1 = 0, BA0 = 0 for MR0
- BA2 = 0, BA1 = 0, BA0 = 1 for MR1
- BA2 = 0, BA1 = 1, BA0 = 0 for MR2
- BA2 = 0, BA1 = 1, BA0 = 1 for MR3

The MRS command can only be issued (or reissued) when all banks are idle and in the precharged state (t_{RP} is satisfied and no data bursts are in progress). The controller must wait the specified time t_{MRD} before initiating a subsequent operation such as an ACTIVATE command. There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by t_{MOD}. Violating either of these requirements (t_{MOD}, T_{MRD}) will result in unspecified operation.

(continued on page 19)

FIGURE 13 – MULTIPURPOSE REGISTER (MPR) BLOCK DIAGRAM



NOTES:

1. A predefined data pattern can be read out of the MPR with an external READ command.
2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR contents can be read out continuously with a regular READ or RDAP command.

TABLE 5 – MPR FUNCTIONAL DESCRIPTION OF MR3 BITS

MR3(2)	MR3(1:0)	Function
MPR	MPR Read Function	
0	"Don't Care"	Normal operation, no MPR transaction All subsequent READs come from the DRAM memory array All subsequent WRITEs go to the DRAM memory array
1	A(1:0)	Enable MPR mode, subsequent READ/RDAP commands defined by bits 1 and 2

TABLE 6 – MPR READOUTS AND BURST ORDER BIT MAPPING

MR3(2)	MR3(1:0)	Functions	Burst Length	Read A[2:0]	Function
1	00	Read predefined pattern for system calibration	BL8	000	Burst order: 0 ,1, 2, 3, 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1, 0, 1, 0, 1
			BC4	000	Burst order: 0 ,1, 2, 3 Predefined pattern: 0, 1, 0, 1
			BC4	100	Burst order: 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1
1	01	RFU	n/a	n/a	n/a
1	10	RFU	n/a	n/a	n/a
1	11	RFU	n/a	n/a	n/a

NOTE:

1. Burst order bit 0 is assigned to LSB, and burst order bit 7 is assigned to MSB of the selected MPR agent.

ZQ CALIBRATION OPERATION

The ZQ CALIBRATION command is used to calibrate the DRAM output drivers (RON) and ODT values (RTT) over process, voltage, and temperature, provided a dedicated 240Ω (±1 percent) external resistor is connected from the DRAM's ZQ ball to V_{SSQ}. DDR3 SDRAM need a longer time to calibrate RON and ODT at power-up initialization and self refresh exit and a relatively shorter time to perform periodic calibrations. DDR3 SDRAM defines two ZQ CALIBRATION commands: ZQ CALIBRATION LONG (ZQCL) and ZQ CALIBRATION SHORT (ZQCS).

All banks must be precharged and t_{RP} must be met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than another ZQCL or ZQCS command may be issued to another DRAM) can be performed on the DRAM channel by the controller for the duration of t_{ZQINIT} or t_{ZQOPER} . The quiet time on the DRAM channel helps accurately calibrate RON and ODT. After DRAM calibration is achieved, the DRAM should disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon self refresh exit, an explicit ZQCL is required if ZQ calibration is desired.

ACTIVATE OPERATION

Before any READ or WRITE commands can be issued to a bank within the DRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to t_{RCD} (MIN). In this operation, the DRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank, but prior to t_{RCD} (MIN) with the requirement that (ACTIVATE-to-READ/WRITE) + AL ≥ t_{RCD} (MIN) (see "POSTED CAS ADDITIVE Latency (AL)"). t_{RCD} (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to t_{CCD} (MIN).

A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by t_{RC}.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by t_{RRD}. No more than four bank ACTIVATE commands may be issued in a given t_{FAW} (MIN) period, and the t_{RRD} (MIN) restriction still applies. The t_{FAW} (MIN) parameter applies, regardless of the number of banks already opened or closed.

READ OPERATION

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address is available READ latency (RL) clocks later. RL is defined as the sum of POSTED CAS ADDITIVE latency (AL) and CAS latency (CL) (RL = AL + CL). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK#).

DQS, DQS# is driven by the DRAM along with the output data. The initial low state on DQS and HIGH state on DQS# is known as the READ preamble (t_{RPRE}). The low state on DQS and the HIGH state on DQS#, coincident with the last data-out element, is known as the READ postamble (t_{RPST}). Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued t_{CCD} cycles after the first READ command. If BC4 is enabled, t_{CCD} must still be met which will cause a gap in the data output. DDR3 SDRAM do not allow interrupting or truncating any READ burst.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. To ensure the read data is completed before the write data is on the bus, the minimum READ-to-WRITE timing is RL + t_{CCD} - WL + $2t_{CK}$.

A READ burst may be followed by a PRECHARGE command to the same bank provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank is four clocks and must also satisfy a minimum analog time from the READ command. This time is called t_{RTP} (READ-to-PRECHARGE). t_{RTP} starts AL cycles later than the READ command. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met. The PRECHARGE command followed by another PRECHARGE command to the same bank is allowed. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The DRAM starts an auto precharge operation on the rising edge which is AL + t_{RTP} cycles after the READ command. DRAM support a t_{RAS} lockout feature. If t_{RAS} (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until t_{RAS} (MIN) is satisfied. If t_{RTP} (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until t_{RTP} (MIN) is satisfied.

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TABLE 7 – TRUTH TABLE - DDR3 COMMANDS

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA2 BA1 BA0	An	A12	A10	A11, A9-A0	Notes
			Previous Cycle	Next Cycle										
MODE REGISTER SET		MRS	H	H	L	L	L	L	BA	OP Code				
REFRESH		REF	H	H	L	L	L	H	V	V	V	V	V	
SELF-REFRESH Entry		SRE	H	L	L	L	L	H	V	V	V	V	V	6
SELF-REFRESH Exit		SRX	L	H	H	V	V	V	V	V	V	V	V	6, 7
					L	H	H	H						
Single bank precharge		PRE	H	H	L	L	H	L	BA	V	V	L	V	
All banks PRECHARGE		PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank activate		ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS, BC4MRS	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	8
	BC4OTF	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	8
	BL8OTF	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	8
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA	8
	BC4OTF	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	CA	8
	BL8OTF	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	CA	8
READ	BL8MRS BC4MRS	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	8
	BC4OTF	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	8
	BL8OTF	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	8
READ with auto precharge	BL8MRS BC4MRS	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA	8
	BC4OTF	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	CA	8
	BL8OTF	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	CA	8
NO OPERATION		NOP	H	H	L	H	H	H	V	V	V	V	V	9
Device DESELECT		DES	H	H	H	X	X	X	X	X	X	X	X	10
POWER-DOWN entry		PDE	H	L	L	H	H	H	V	V	V	V	V	6
					H	V	V	V						
POWER-DOWN exit		PDX	L	H	L	H	H	H	V	V	V	V	V	6, 11
					H	V	V	V						
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	L	X	X	X	H	X	12
ZQ QALIBRATION SHORT		ZQCS	H	H	L	H	H	L	X	X	X	L	X	

NOTES: (notes 1-5 apply to the entire table)

1. Commands are defined by states of CAS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device-density and configuration-dependent.
2. RESET# is LOW enabled and used only for asynchronous reset. Thus, RESET# must be held HIGH during any normal operation.
3. The state of ODT doesn not affect the states described in this table.
4. Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.
5. “V” means “H” or “L” (a defined logic level), and “X” means “Don’t Care.”
6. See Table 8 for additional information on CKE transition.
7. Self refresh exit is asynchronous.
8. Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.
9. The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.
10. The DES and NOP commands perform similarly.
11. The power-down mode does not perform any REFRESH operations.
12. ZQ CALIBRATION LONG is used for either ZQINIT (first ZQCL command during initialization) or ZQ oper(ZQCL command after initialization)

TABLE 8 – TRUTH TABLE - CKE [1, 2]

Current State[3]	CKE		Command[5]	Action[5]	Notes
	Previous Cycle[4] (n - 1)	Previous Cycle[4] (n)			
Power-down	L	L	"Don't Care"	Maintain power-down	
	L	H	DES or NOP	Power-down exit	
Self Refresh	L	L	"Don't Care"	Maintain self refresh	
	L	H	DES or NOP	Self refresh exit	
Bank(s) Active	H	L	DES or NOP	Active power-down entry	
Reading	H	L	DES or NOP	Power-down entry	
Writing	H	L	DES or NOP	Power-down entry	
Precharging	H	L	DES or NOP	Power-down entry	
Refreshing	H	L	DES or NOP	Precharge power-down entry	
All banks idle	H	L	DES or NOP	Precharge power-down entry	6
	H	L	REFRESH	Self Refresh	

NOTES:
1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2. t_{CKE} (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + t_{CKE} (MIN) + t_{IH}.
3. Current state = The state of the DRAM immediately prior to clock edge n.
4. CKE (n) is the logic state of CKE at clock edge n; CKE (n - 1) was the state of CKE at the previous clock edge.
5. COMMAND is the command registered at the clock edge (must be a legal command as defined in Table 7). Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.
6. Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied — All self refresh exit and power-down exit parameters are also satisfied.

In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point at which the internal precharge happens (not at the next rising clock edge after this event). The time from READ with auto precharge to the next ACTIVATE command to the same bank is AL + (t_{RTP} + t_{RP})*, where "*" means rounded up to the next integer. In any event, internal precharge does not start earlier than four clocks after the last 8n-bit prefetch.

POWER-DOWN MODE

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while either an MRS, MPR, ZQCAL, READ, or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations (such as ROW ACTIVATION, PRECHARGE, auto precharge, or REFRESH) are in progress. However, the power-down I_{CC} specifications are not applicable until such operations have been completed. Depending on the previous DRAM state and the command issued prior to CKE going LOW, certain timing constraints must be satisfied.

Entering power-down disables the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. NOP or DES commands are required until t_{CPDED} has been satisfied, at which time all specified input/output buffers will be disabled. The DLL should be in a locked state when power-down is entered for the fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation as well as synchronous ODT operation.

During power-down entry, if any bank remains open after all in-progress commands are complete, the DRAM will be in active power-down mode. If all banks are closed after all in-progress commands are complete, the DRAM will be in precharge power-down mode. Precharge power-down mode must be programmed to exit with either a slow exit mode or a fast exit mode. When entering precharge power-down mode, the DLL is turned off in slow exit mode or kept on in fast exit mode.

The DLL remains on when entering active power-down as well. ODT has special timing constraints when slow exit mode precharge power-down is enabled and entered.

While in either power-down state, CKE is held LOW, RESET# is held HIGH, and a stable clock signal must be maintained. ODT must be in a valid state but all other input signals are a "Don't Care." If RESET# goes LOW during power-down, the DRAM will switch out of power-down mode and go into the reset state. After CKE is registered LOW, CKE must remain LOW until t_{PD} (MIN) has been satisfied. The maximum time allowed for powerdown duration is t_{PD} (MAX) (9 × t_{REFI}).

The power-down states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until t_{CKE} has been satisfied. A valid, executable command may be applied after power-down exit latency, t_{XP} t_{XPDLL} have been satisfied.

For certain CKE-intensive operations, for example, repeating a power-down exit to refresh to power-down entry sequence, the number of clock cycles between power-down exit and power-down entry may not be sufficient enough to keep the DLL properly updated. In addition to meeting t_{PD} when the REFRESH command is used in between power-down exit and power-down entry, two other conditions must be met. First, t_{XP} must be satisfied before issuing the REFRESH command. Second, t_{XPDLL} must be satisfied before the next power-down may be entered.

WRITE LEVELING

For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks. Write leveling is a scheme for the memory controller to adjust or deskew the DQS strobe (DQS, DQS#) to CK relationship at the DRAM with a simple feedback feature provided by the DRAM. Write leveling is generally used as part of the initialization process, if required. For normal DRAM operation, this feature must be disabled. This is the only DRAM operation where the DQS functions as an input (to capture the incoming clock) and the DQ function as outputs (to report the state of the clock). Note that nonstandard ODT schemes are required.

The memory controller using the write leveling procedure must have adjustable delay settings on its DQS strobe to align the rising edge of DQS to the clock at the DRAM pins. This is accomplished when the DRAM asynchronously feeds back the CK status via the DQ bus and samples with the rising edge of DQS. The controller repeatedly delays the DQS strobe until a CK transition from “0” to “1” is detected. The DQS delay established through this procedure helps ensure t_{DQSS}, t_{DSS}, and t_{DSH} specifications in systems that use fly-by topology by deskewing the trace length mismatch.

When write leveling is enabled, the rising edge of DQS samples CK, and the prime DQ outputs the sampled CK’s status. The prime DQ for a x8 configuration is DQ0 with all other DQ[7:1] driving low.

The write leveling mode register interacts with other mode registers to correctly configure the write leveling functionality. Besides using MR1[7] to disable/enable write leveling, MR1[12] must be used to enable/disable the output buffers. The ODT value, burst length, and so forth need to be selected as well. It should also be noted that when the outputs are enabled during write leveling mode, the DQS buffers are set as inputs, and the DQ are set as outputs. Additionally, during write leveling mode, only the DQS strobe terminations are activated and deactivated via the ODT ball. The DQ remain disabled and are not affected by the ODT ball.

WRITE LEVELING PROCEDURE

A memory controller initiates the DRAM write leveling mode by setting MR1[7] to a “1,” assuming the other programable features (MR0, MR1, MR2, and MR3) are first set and the DLL is fully reset and locked. The DQ balls enter the write leveling mode going from a High-Z state to an undefined driving state, so the DQ bus should not be driven. During write leveling mode, only the NOP or DES commands are allowed. The memory controller should attempt to level only one rank at a time; thus, the outputs of other ranks should be disabled by setting MR1[12] to a “1” in the other ranks. The memory controller may assert ODT after a t_{MOD} delay as the DRAM will be ready to process the ODT transition. ODT should be turned on prior to DQS being driven LOW by at least ODTL on delay (WL - 2 t_{CK}), provided it does not violate the aforementioned t_{MOD} delay requirement.

The memory controller may drive DQS LOW and DQS# HIGH after $t_{WLDQSEN}$ has been satisfied. The controller may begin to toggle DQS after t_{WLMRD} (one DQS toggle is DQS transitioning from a LOW state to a HIGH state with DQS# transitioning from a HIGH state to a LOW state, then both transition back to their original states). At a minimum, ODTL on and t_{AON} must be satisfied at least one clock prior to DQS toggling.

After t_{WLMRD} and a DQS LOW preamble (t_{WPRE}) have been satisfied, the memory controller may provide either a single DQS toggle or multiple DQS toggles to sample CK for a given DQS-to-CK skew. Each DQS toggle must not violate t_{DQSL} (MIN) and t_{DQSH} (MIN) specifications. t_{DQSL} (MAX) and t_{DQSH} (MAX) specifications are not applicable during write leveling mode. The DQS must be able to distinguish the CK’s rising edge within t_{WLS} and t_{WLH}. The prime DQ will output the CK’s status asynchronously from the associated DQS rising edge CK capture within tWLO. The remaining DQ that always drive LOW when DQS is toggling must be LOW within t_{WLOE} after the first t_{WLO} is satisfied (the prime DQ going LOW). As previously noted, DQS is an input and not an output during this process.

The memory controller will likely sample each applicable prime DQ state and determine whether to increment or decrement its DQS delay setting. After the memory controller performs enough DQS toggles to detect the CK’s “0-to-1” transition, the memory controller should lock the DQS delay setting for that DRAM. After locking the DQS setting, leveling for the rank will have been achieved, and the write leveling mode for the rank should be disabled or reprogrammed (if write leveling of another rank follows).

WRITE LEVELING MODE EXIT PROCEDURE

After the DRAM are leveled, they must exit from write leveling mode before the normal mode can be used. After the last rising DQS (capturing a “1” at T0), the memory controller should stop driving the DQS signals after t_{WLO} (MAX) delay plus enough delay to enable the memory controller to capture the applicable prime DQ state (at ~Tb0). The DQ balls become undefined when DQS no longer remains LOW, and they remain undefined until t_{MOD} after the MRS command (at Te1).

The ODT input should be deasserted LOW such that ODTL off (MIN) expires after the DQS is no longer driving LOW. When ODT LOW satisfies tIS, ODT must be kept LOW (at ~Tb0) until the DRAM is ready for either another rank to be leveled or until the normal mode can be used. After DQS termination is switched off, write level mode should be disabled via the MRS command (at Tc2). After t_{MOD} is satisfied (at Te1), any valid command may be registered by the DRAM. Some MRS commands may be issued after t_{MRD} (at Td1).

TABLE 9 – READ COMMAND SUMMARY

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [3:0]	An	A12	A10	A[11, 9:0]
			Previous Cycle	Next Cycle									
Read	BL8MRS, BC4MRS	RD	H		L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4	H		L	H	L	H	BA	RFU	L	L	CA
	BL8OTF	RDS8	H		L	H	L	H	BA	RFU	H	L	CA
Read with auto precharge	BL8MRS, BC4MRS	RDAP	H		L	H	L	H	BA	RFU	V	H	CA
	BC4OTF	RDAPS4	H		L	H	L	H	BA	RFU	L	H	CA
	BL8OTF	RDAPS8	H		L	H	L	H	BA	RFU	H	H	CA

TABLE 10 – WRITE COMMAND SUMMARY

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [3:0]	An	A12	A10	A[11, 9:0]
			Previous Cycle	Next Cycle									
Write	BL8MRS, BC4MRS	WR	H		L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4	H		L	H	L	L	BA	RFU	L	L	CA
	BL8OTF	WRS8	H		L	H	L	L	BA	RFU	H	L	CA
Write with auto precharge	BL8MRS, BC4MRS	WRAP	H		L	H	L	L	BA	RFU	V	H	CA
	BC4OTF	WRAPS4	H		L	H	L	L	BA	RFU	L	H	CA
	BL8OTF	WRAPS8	H		L	H	L	L	BA	RFU	H	H	CA

TABLE 11 – READ ELECTRICAL CHARACTERISTICS, DLL DISABLE MODE

Parameter	Symbol	Min	Max	Units
Access window of DQS from CK, CK#	t_{DQSCK} (DLL_DIS)	1	10	ns

TABLE 14A – DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V_{CC}	1.283	1.35	1.45	V	1, 2, 3
I/O Supply voltage	V_{CCQ}	1.283	1.35	1.45	V	1, 2, 3
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{CC}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	I_I	-20	-	20	µA	
V_{REF} supply leakage current V_{REFDQ} = V_{CC}/2 or V_{REFCA} = V_{CC}/2 (All other pins not under test = 0V)	I_{VREF}	-10	-	10	µA	4

NOTES:

1. V_{CC} and V_{CCQ} must track one another. V_{CCQ} must be less than or equal to V_{CC}. V_{SS} = V_{SSQ}.
2. V_{CC} and V_{CCQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0Hz to 250 kHz) specifications. V_{CC} and V_{CCQ} must be at same level for valid AC timing parameters.
3. V_{CC} and V_{CCQ} are tied.
4. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.

Table 14B – DC ELECTRICAL CHARACTERISTICS AND INPUT CONDITIONS

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
V_{IN} low; DC/commands/address busses	V_{IL}	V_{SS}	n/a	See table 18	V	
V_{IN} high; DC/commands/address busses	V_{IH}	See table 18	n/a	V_{CC}	V	
Input reference voltage command/address bus	$V_{REFCA(DC)}$	0.49 X V_{CC}	0.5 X V_{CC}	0.51 X V_{CC}	V	1, 2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	0.49 x V_{CC}	0.5 X V_{CC}	0.51 x V_{CC}	V	2, 3
I/O reference voltage DQ bus in SELF REFRESH	$V_{REFDQ(sr)}$	Vss	0.5 X V_{CC}	V_{CC}	V	4
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	–	0.5 x V_{CC}Q	–	V	5

NOTES:

1. $V_{REFCA(DC)}$ is expected to be approximately 0.5 x V_{CC} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1 % x V_{CC} around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of $V_{REFCA(DC)}$.
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces accitional AC noise greater than 20 MHz in frequency.
3. $V_{REFDQ(DC)}$ is expected to be approximately 0.5 x V_{CC} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1 % x V_{CC} around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of $V_{REFDQ(DC)}$.
4. $V_{REFDQ(DC)}$ may transition to $V_{REFDQ(sr)}$ and back to $V_{REFDQ(DC)}$ when in SELF REFRESH, within restrictions outlined in the SELF REFRESH section.
5. V_{TT} is not applied directly to the DRAM component. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

TABLE 15 – ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MIN	MAX	Unit	Notes
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}	-0.4	1.85	V	1
V_{CCQ}	Voltage on V_{CC} pin relative to V_{SS}	-0.4	1.85	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	1.85	V	
T_{STG}	Storage temperature	-55	125	°C	

NOTES:

1. V_{CC} and V_{CCQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{CCQ}. When V_{CC} and V_{CCQ} are less than 500mV, V_{REF} may be ≤300mV.

TABLE 17 – BGA THERMAL RESISTANCE FOR W3J512M32K-XBX

Description	Symbol	Typical	Units	Notes
Junction to Board	Theta JB	TBD	°C/W	1
Junction to Case (Top)	Theta JC	TBD	°C/W	1

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

TABLE 17A – BGA THERMAL RESISTANCE FOR W3J512M32KT-XB2X

Description	Symbol	Typical	Units	Notes
Junction to Board	Theta JB	TBD	°C/W	1
Junction to Case (Top)	Theta JC	TBD	°C/W	1

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

TABLE 17B – BGA THERMAL RESISTANCE FOR W3J512M40K(T)-XB3X

Description	Symbol	Typical	Units	Notes
Junction to Board	Theta JB	TBD	°C/W	1
Junction to Case (Top)	Theta JC	TBD	°C/W	1

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

TABLE 18 – AC INPUT OPERATING CONDITIONS

Parameter	Symbol	DDR3-800 DDR3-1066	**DDR3-1333**	Unit
Command and Address				
Input high AC voltage: Logic 1	V_{IH}(AC160)min	+160	+160	mV
Input high AC voltage: Logic 1	V_{IH}(AC135)min	+135	+135	mV
Input high DC voltage: Logic 1	V_{IH}(DC90)min	+90	+90	mV
Input low DC voltage: Logic 0	V_{IL}(DC90)max	–90	–90	mV
Input low AC voltage: Logic 0	V_{IL}(AC135)max	–135	–135	mV
Input low AC voltage: Logic 0	V_{IL}(AC160)max	–160	–160	mV
DQ and DM				
Input high AC voltage: Logic 1	V_{IH}(AC160)min	+160	+160	mV
Input high AC voltage: Logic 1	V_{IH}(AC135)min	+135	+135	mV
Input high DC voltage: Logic 1	V_{IH}(DC90)min	+90	+90	mV
Input low DC voltage: Logic 0	V_{IL}(DC90)max	–90	–90	mV
Input low AC voltage: Logic 0	V_{IL}(AC135)max	–135	–135	mV
Input low AC voltage: Logic 0	V_{IL}(AC160)max	–160	–160	mV

NOTE

1. All voltages are referenced to V_{REF}, V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.

TABLE 19 – ON-DIE TERMINATION DC ELECTRICAL CHARACTERISICS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
RTT effective impedance	RTT_EFF	See Table 20			Ω	1, 2
Deviation of VM with respect to $V_{CCQ/2}$	ΔVMM	-10		+5	%	1, 2, 3

NOTES

1. 1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{CCQ} = V_{CC}$, $V_{SSQ} = V_{SS}$).
2. Measurement definition for RTT: Apply V_{IH}(AC) to pin under test and measure current I[V_{IH}(AC)], then apply V_{IL}(AC) to pin under test and measure current I[V_{IL}(AC)]:

$$RTT = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

3. Measure voltage (VM) at the tested pin with no load:

$$\Delta VM = \left(\frac{2 \times VM}{V_{CCQ}} - 1\right) \times 100$$

TABLE 20 – AC INPUT OPERATING CONDITIONS

MR1 [9, 6, 2]	R$_{TT}$	Resistor	V$_{OUT}$	Min	Nom	Max	Units
0, 1, 0	120Ω	RTT$_{120PD240}$	0.2 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/1
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/1
			0.8 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/1
		RTT$_{120PU240}$	0.2 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/1
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/1
			0.8 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/1
	120Ω		V$_{IL}$(AC) to V$_{IH}$(AC)	0.8	1.0	1.85	RZQ/2
0, 0, 1	60Ω	RTT$_{60PD120}$	0.2 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/2
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/2
			0.8 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/2
		RTT$_{60PU120}$	0.2 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/2
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/2
			0.8 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/2
	60Ω		V$_{IL}$(AC) to V$_{IH}$(AC)	0.8	1.0	1.85	RZQ/4
0, 1, 1	40Ω	RTT$_{40PD80}$	0.2 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/3
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/3
			0.8 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/3
		RTT$_{40PU80}$	0.2 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/3
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/3
			0.8 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/3
	40Ω		V$_{IL}$(AC) to V$_{IH}$(AC)	0.8	1.0	1.85	RZQ/6
1, 0, 1	30Ω	RTT$_{30PD60}$	0.2 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/4
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/4
			0.8 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/4
		RTT$_{30PU60}$	0.2 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/4
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/4
			0.8 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/4
	30Ω		V$_{IL}$(AC) to V$_{IH}$(AC)	0.8	1.0	1.85	RZQ/8
1, 0, 0	20Ω	RTT$_{20PD40}$	0.2 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/6
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/6
			0.8 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/6
		RTT$_{20PU40}$	0.2 x V$_{CCQ}$	0.9	1.0	1.45	RZQ/6
			0.5 x V$_{CCQ}$	0.9	1.0	1.15	RZQ/6
			0.8 x V$_{CCQ}$	0.6	1.0	1.15	RZQ/6
	20Ω		V$_{IL}$(AC) to V$_{IH}$(AC)	0.8	1.0	1.85	RZQ/12

NOTES

1. Values assume an RZQ of 240Ω (±1 percent).
2. RTT$_{XX}$PU and RTT$_{XX}$PD are for reference only. Only RTT for V$_{OUT}$ from V$_{IL}$(AC) to V$_{IH}$(AC) are tested and guaranteed.

TABLE 21 – DDR3 I_{CC} SPECIFICATIONS AND CONDITIONS – W3J512M32K(T)

Symbol	Proposed Conditions		1,333 CL10	800 CL6 1,066 CL8	Units
I_{CC0}	Operating one bank active-precharge current; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		220	188	mA (1, 2)
I_{CC1}	Operating one bank active-read-precharge current; I_{OUT} = 0mA; BL = 8, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}$ (I_{CC}), $t_{RAS} = t_{RAS}min(I_{CC})$, $t_{RCD} = t_{RCD}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bud inpuyd str plosyinh		264	248	mA (1, 2)
I_{CC2P}	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast	128	112	mA (1, 2)
		Slow	72	72	mA (1, 2)
I_{CC2Q}	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		128	112	mA (1, 2)
I_{CC2N}	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		128	116	mA (1, 2)
I_{CC3P}	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		152	140	mA (1, 2)
I_{CC3N}	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RASMAX}(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		152	140	mA (1, 2)
I_{CC4W}	Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RASMAX}(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		500	440	mA (1, 2)
I_{CC4R}	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 8, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RASMAX}(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DAD6W}		628	560	mA (1, 2)
I_{CC5B}	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		940	912	mA (1, 2)
I_{CC6}	Self refresh current; CK, CK# and CKE are low. Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	80	80	mA (1, 2, 3)
I_{CC6ET}	Self refresh current extended temperature: CK, CK# and CKE are low; other control and address bus inputs are floating; data bus inputs are floating		100	100	mA (2, 4)
I_{CC7}	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 8, CL = CL(I_{CC}), AL = $t_{RC}D(I_{CC})$-1*$t_{CK}(I_{CC})$; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, t_{RCD} = 1*$t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I_{DAD6R}; Refer to the following page for detailed timing conditions		880	760	mA (1, 2)

NOTES:
1. SRT and ASR are disabled.
2. Enabling ASR could increase I_{CCx} by up to an additional 8mA

TABLE 21A – DDR3 I_{CC} SPECIFICATIONS AND CONDITIONS – W3J512M40K(T)

Symbol	Proposed Conditions		1,333 CL10	800 CL6 1,066 CL8	Units
I_{CC0}	Operating one bank active-precharge current; t_{CK} = t_{CK}(I_{CC}), t_{RC} = t_{RC}(I_{CC}), t_{RAS} = t_{RAS}min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		275	235	mA (1, 2)
I_{CC1}	Operating one bank active-read-precharge current; I_{OUT} = 0mA; BL = 8, CL = CL(I_{CC}), AL = 0; t_{CK} = t_{CK}(I_{CC}), t_{RC} = t_{RC} (I_{CC}), t_{RAS} = t_{RAS}min(I_{CC}), t_{RCD} = t_{RCD}(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bud inpuyd str plosyinh		330	310	mA (1, 2)
I_{CC2P}	Precharge power-down current; All banks idle; t_{CK} = t_{CK}(I_{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast	160	140	mA (1, 2)
		Slow	90	90	mA (1, 2)
I_{CC2Q}	Precharge quiet standby current; All banks idle; t_{CK} = t_{CK}(I_{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		160	140	mA (1, 2)
I_{CC2N}	Precharge standby current; All banks idle; t_{CK} = t_{CK}(I_{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		160	145	mA (1, 2)
I_{CC3P}	Active power-down current; All banks open; t_{CK} = t_{CK}(I_{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		190	175	mA (1, 2)
I_{CC3N}	Active standby current; All banks open; t_{CK} = t_{CK}(I_{CC}), t_{RAS} = t_{RASMAX}(I_{CC}), t_{RP} = t_{RP}(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		190	175	mA (1, 2)
I_{CC4W}	Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(I_{CC}), AL = 0; t_{CK} = t_{CK}(I_{CC}), t_{RAS} = t_{RASMAX}(I_{CC}), t_{RP} = t_{RP}(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		625	550	mA (1, 2)
I_{CC4R}	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 8, CL = CL(I_{CC}), AL = 0; t_{CK} = t_{CK}(I_{CC}), t_{RAS} = t_{RASMAX}(I_{CC}), t_{RP} = t_{RP}(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DAD6W}		785	700	mA (1, 2)
I_{CC5B}	Burst auto refresh current; t_{CK} = t_{CK}(I_{CC}); Refresh command at every t_{RFC}(I_{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1,175	1,140	mA (1, 2)
I_{CC6}	Self refresh current; CK, CK# and CKE are low. Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	100	100	mA (1, 2, 3)
I_{CC6ET}	Self refresh current extended temperature: CK, CK# and CKE are low; other control and address bus inputs are floating; data bus inputs are floating		125	125	mA (2, 4)
I_{CC7}	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 8, CL = CL(I_{CC}), AL = t_{RC}D(I_{CC})-1*t_{CK}(I_{CC}); t_{CK} = t_{CK}(I_{CC}), t_{RC} = t_{RC}(I_{CC}), t_{RRD} = t_{RRD}(I_{CC}), t_{RCD} = 1*t_{CK}(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I_{DAD6R}; Refer to the following page for detailed timing conditions		1,100	950	mA (1, 2)

NOTES:
1. SRT and ASR are disabled.
2. Enabling ASR could increase I_{CCx} by up to an additional 10mA

TABLE 22 – DDR3-800 SPEED BINS

CL-t_{RCD}-t_{RP}			6-6-6		Units	Notes
Parameter		Symbol	Min	Max		
ACTIVATE to internal READ or WRITE delay time		t_{RCD}	15	–	ns	
PRECHARGE command period		t_{RP}	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		t_{RC}	52.5	–	ns	
ACTIVATE-to-PRECHARGE command period		t_{RAS}	37.5	9 x t_{REFI}	ns	1
CL = 6	CWL = 5	$t_{CK\ (AVG)}$	2.5	3.3	ns	2
Supported CL settings			6		CK	
Supported CWL setting			5		CK	

NOTES:
1. t_{REFI} depends on T_{OPER}.
2. The CL and CWL settings result in t_{CK} requirements. When making a selection of t_{CK}, both CL and CWL requirement settings need to be fulfilled.

TABLE 23 – DDR3-1,066 SPEED BINS

CL-t_{RCD}-t_{RP}			8-8-8		Units	Notes
Parameter		Symbol	Min	Max		
ACTIVATE to internal READ or WRITE delay time		t_{RCD}	15	–	ns	
PRECHARGE command period		t_{RP}	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		t_{RC}	52.5	–	ns	
ACTIVATE-to-PRECHARGE command period		t_{RAS}	37.5	9 x t_{REFI}	ns	1
CL = 8	CWL = 6	$t_{CK\ (AVG)}$	1.875	<2.5	ns	2
Supported CL settings			5, 6, 8		CK	
Supported CWL setting			5, 6		CK	

NOTES:
1. t_{REFI} depends on T_{OPER}.
2. The CL and CWL settings result in t_{CK} requirements. When making a selection of t_{CK}, both CL and CWL requirement settings need to be fulfilled.

TABLE 24 – DDR3-1,333 SPEED BINS

CL-t_{RCD}-t_{RP}			10-10-10		Units	Notes
Parameter		Symbol	Min	Max		
Internal READ command to fist data		t_{AA}	15	–		
ACTIVATE to internal READ or WRITE delay time		t_{RCD}	15	–	ns	
PRECHARGE command period		t_{RP}	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		t_{RC}	51	-	ns	
ACTIVATE-to-PRECHARGE command period		t_{RAS}	36	9 x t_{REFI}	ns	1
CL = 5	CWL = 5	$t_{CK\ (AVG)}$	3.0	3.3	ns	2
CL = 6	CWL = 5	$t_{CK\ (AVG)}$	2.5	3.3	ns	2
CL = 8	CWL = 6	$t_{CK\ (AVG)}$	1.875	<2.5	ns	2
CL = 10	CWL = 7	$t_{CK\ (AVG)}$	1.5	<1.875	ns	2
Supported CL settings			5, 6, 8, 10		CK	
Supported CWL setting			5, 6, 7		CK	

NOTES:
1. t_{REFI} depends on T_{OPER}.
2. The CL and CWL settings result in t_{CK} requirements. When making a selection of t_{CK}, both CL and CWL requirement settings need to be fulfilled.

TABLE 26 – AC TIMING PARAMETERS

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
			Min	Max	Min	Max	Min	Max		
Clock Timing										
Clock period average: DLL disable mode	Commercial and Industrial	t_{CKDLL_DIS}	8	7,800	8	7,800	8	7,800	ns	9, 42
	Military		8	3,900	8	3,900	8	3,900	ns	42
Clock period average: DLL enable mode		$t_{CK\ (AVG)}$	See "Speed Bin Tables" on page 35 for t_{CK} range allowed						ns	10, 11
High pulse width average		$t_{CH\ (AVG)}$	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		$t_{CL\ (AVG)}$	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	t_{JITPER}	–100	100	–90	90	–80	80	ps	13
	DLL locking	$t_{JITPER,\ LCK}$	–90	90	–80	80	–70	70	ps	13
Clock absolute period		$t_{CK(ABS)}$	MIN = $t_{CK\ (AVG)}$ MIN + t_{JITPER} MIN; MAX = $t_{CK\ (AVG)}$ MAX + t_{JITPER} MAX						ps	
Clock absolute high pulse width		$t_{CH\ (ABS)}$	0.43	–	0.43	–	0.43	–	$t_{CK\ (AVG)}$	14
Clock absolute low pulse width		$t_{CL\ (ABS)}$	0.43	–	0.43	–	0.43	–	$t_{CK\ (AVG)}$	15
Cycle-to-cycle jitter	DLL locked	t_{JITCC}	200		180		160		ps	16
	DLL locking	$t_{JITCC,\ LCK}$	180		160		140		ps	16
Cumulative error across	2 cycles	$t_{ERR2PER}$	–147	147	–132	132	–118	118	ps	17
	3 cycles	$t_{ERR3PER}$	–175	175	–157	157	–140	140	ps	17
	4 cycles	$t_{ERR4PER}$	–194	194	–175	175	–155	155	ps	17
	5 cycles	$t_{ERR5PER}$	–209	209	–188	188	–168	168	ps	17
	6 cycles	$t_{ERR6PER}$	–222	222	–200	200	–177	177	ps	17
	7 cycles	$t_{ERR7PER}$	–232	232	–209	209	–186	186	ps	17
	8 cycles	$t_{ERR8PER}$	–241	241	–217	217	–193	193	ps	17
	9 cycles	$t_{ERR9PER}$	–249	249	–224	224	–200	200	ps	17
	10 cycles	$t_{ERR10PER}$	–257	257	–231	231	–205	205	ps	17
	11 cycles	$t_{ERR11PER}$	–263	263	–237	237	–210	210	ps	17
	12 cycles	$t_{ERR12PER}$	–269	269	–242	242	–215	215	ps	17
	n = 13, 14 . . . 49, 50 cycles	$t_{ERRnPER}$	$t_{ERRnPER}$ MIN = (1 + 0.68ln[n]) × t_{JITPER} MIN $t_{ERRnPER}$ MAX = (1 + 0.68ln[n]) × t_{JITPER} MAX						ps	17
DQ Input Timing										
Data setup time to DQS, DQS#	Base (specification)	$t_{DS\ AC160}$	90	–	40	–	–	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		250	–	200	–	–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	$t_{DS\ AC135}$	140	–	90	–	45	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		275	–	225	–	180	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	$t_{DH\ DC90}$	160	–	110	–	75	–	ps	18,19
	V_{REF} @ 1 V/ns		250	–	200	–	165	–	ps	19, 20
Minimum data pulse width		t_{DIPW}	600	–	490	–	400	–	ps	41
DQ Output Timing										
DQS, DQS# to DQ skew, per access		t_{DQSQ}	–	200	–	150	–	125	ps	
DQ output hold time from DQS, DQS#		t_{QH}	0.38	–	0.38	–	0.38	–	$t_{CK\ (AVG)}$	21
DQ Low-Z time from CK, CK#		$t_{LZ\ (DQ)}$	–800	400	–600	300	–500	250	ps	22, 23
DQ High-Z time from CK, CK#		$t_{HZ\ (DQ)}$	–	400	–	300	–	250	ps	22, 23

TABLE 26 – AC TIMING PARAMETERS (continued)

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
			Min	Max	Min	Max	Min	Max		
DQ Strobe Input Timing										
DQS, DQS# rising to CK, CK# rising		t_{DQSS}	–0.25	0.25	–0.25	0.25	–0.25	0.25	CK	25
DQS, DQS# differential input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		t_{DSS}	0.2	–	0.2	–	0.2	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		t_{DSH}	0.2	–	0.2	–	0.2	–	CK	25
DQS, DQS# differential WRITE preamble		t_{WPRE}	0.9	–	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		t_{WPST}	0.3	–	0.3	–	0.3	–	CK	
DQ Strobe Output Timing										
DQS, DQS# rising to/from rising CK, CK#		t_{DQSCK}	–400	400	–300	300	–255	255	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		$t_{DQSCK\,DLL\_DIS}$	1	10	1	10	1	10	ns	26
DQS, DQS# differential output high time		t_{QSH}	0.38	–	0.38	–	0.40	–	CK	21
DQS, DQS# differential output low time		t_{QSL}	0.38	–	0.38	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		$t_{LZ\,(DQS)}$	–800	400	–600	300	–500	250	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		$t_{HZ\,(DQS)}$	–	400	–	300	–	250	ps	22, 23
DQS, DQS# differential READ preamble		t_{RPRE}	0.9	Note 24	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		t_{RPST}	0.3	Note 27	0.3	Note 27	0.3	Note 27	CK	23, 27
Command and Address Timing										
DLL locking time		t_{DLLK}	512	–	512	–	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	$t_{IS\,AC160}$	215	–	140	–	80	–	ps	29, 30
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	ps	20, 30
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	$t_{IH\,(AC135)}$	365	–	290	–	205	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		500	–	425	–	340	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	$t_{IH\,DC90}$	285	–	210	–	150	–	ps	29, 30
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		t_{IPW}	900	–	780	–	620	–	ps	41
ACTIVATE to internal READ or WRITE delay		t_{RCD}	See "Speed Bin Tables" on page 28 for t_{RCD}						ns	31
PRECHARGE command period		t_{RP}	See "Speed Bin Tables" on page 28 for t_{RP}						ns	31
ACTIVATE-to-PRECHARGE command period		t_{RAS}	See "Speed Bin Tables" on page 28 for t_{RAS}						ns	31, 32
ACTIVATE-to-ACTIVATE command period		t_{RC}	See "Speed Bin Tables" on page 28 for t_{RC}						ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	t_{RRD}	MIN = greater of 4CK or 10ns		MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6ns		CK	31
	2KB page size		MIN = greater of 4CK or 10ns				MIN = greater of 4CK or 7.5ns		CK	31
Four ACTIVATE windows for 1KB page size		t_{FAW}	40	–	37.5	–	30	–	ns	31
Four ACTIVATE windows for 2KB page size			50	–	50	–	45	–	ns	31
Write recovery time		t_{WR}	MIN = 15ns; MAX = n/a						ns	31, 32, 33, 34
Delay from start of internal WRITE transaction to internal READ command		t_{WTR}	MIN = greater of 4CK or 7.5ns; MAX = n/a						CK	31, 34
READ-to-PRECHARGE time		t_{RTP}	MIN = greater of 4CK or 7.5ns; MAX = n/a						CK	31, 32
CAS#-to-CAS# command delay		t_{CCD}	MIN = 4CK; MAX = n/a						CK	
Auto precharge write recovery + precharge time		t_{DAL}	MIN = WR + t_{RP}/t_{CK} (AVG); MAX = n/a						CK	
MODE REGISTER SET command cycle time		t_{MRD}	MIN = 4CK; MAX = n/a						CK	
MODE REGISTER SET command update delay		t_{MOD}	MIN = greater of 12CK or 15ns; MAX = n/a						CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		t_{MPRR}	MIN = 1CK; MAX = n/a						CK	

continued on next page

TABLE 26 – AC TIMING PARAMETERS (continued)

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
			Min	Max	Min	Max	Min	Max		
Calibration Timing										
ZQCL command: Long calibration time	POWER-UP and RESET operation	t_{ZQINIT}	512	–	512	–	512	–	CK	
	Normal operation	t_{ZQOPER}	256	–	256	–	256	–	CK	
ZQCS command: Short calibration time		t_{ZQCS}	64	–	64	–	64	–	CK	
Initialization and Reset Timing										
Exit reset from CKE HIGH to a valid command		t_{XPR}	MIN = greater of 5CK or t_{RFC} + 10ns; MAX = n/a						CK	
Begin power supply ramp to power supplies stable		t_{VDDPR}	MIN = n/a; MAX = 200						ms	
RESET# LOW to power supplies stable		t_{RPS}	MIN = 0; MAX = 200						ms	
RESET# LOW to I/O and RTT High-Z		t_{IOz}	MIN = n/a; MAX = 20						ns	35
Refresh Timing										
REFRESH-to-ACTIVATE or REFRESH command period		t_{RFC}	MIN = 260; MAX = 70,200						ns	
Maximum average periodic refresh	Com, Ind (1X)	t_{REFI}	7.8 (64ms/8,192)						µs	36
	Military, 85°C to 95°C temperature (2X)		3.9 (32ms/8,192)						µs	36
	Military, 95°C to 125°C temperature (4X)		1.95 (16ms/8,192)						µs	36
Self Refresh Timing										
Exit self refresh to commands not requiring a locked DLL		t_{XS}	MIN = greater of 5CK or t_{RFC} + 10ns; MAX = n/a						CK	
Exit self refresh to commands requiring a locked DLL		t_{XSDLL}	MIN = t_{DLLK} (MIN); MAX = n/a						CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		t_{CKESR}	MIN = t_{CKE} (MIN) + CK; MAX = n/a						CK	
Valid clocks after self refresh entry or powerdown entry		t_{CKSRE}	MIN = greater of 5CK or 10ns; MAX = n/a						CK	
Valid clocks before self refresh exit, powerdown exit, or reset exit		t_{CKSRX}	MIN = greater of 5CK or 10ns; MAX = n/a						CK	
Power-Down Timing										
CKE MIN pulse width		$t_{CKE\ (MIN)}$	Greater of 3CK or 7.5ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5.625ns		CK	
Command pass disable delay		t_{CPDED}	MIN = 1; MAX = n/a						CK	
Power-down entry to power-down exit timing		t_{PD}	MIN = t_{CKE} (MIN); MAX = 9 × t_{REFI}						CK	
Begin power-down period prior to CKE registered HIGH		t_{ANPD}	WL - 1CK						CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of t_{ANPD} or t_{RFC} - REFRESH command to CKE LOW time						CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	t_{ANPD} + t_{XPDLL}						CK	
Power-Down Entry Minimum Timing										
ACTIVATE command to power-down entry		$t_{ACTPDEN}$	MIN = 1						CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		t_{PRPDEN}	MIN = 1						CK	
REFRESH command to power-down entry		$t_{REFPDEN}$	MIN = 1						CK	37
MRS command to power-down entry		$t_{MRSPDEN}$	MIN = t_{MOD} (MIN)						CK	
READ/READ with auto precharge command to power-down entry		t_{RDPDEN}	MIN = RL + 4 + 1						CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	t_{WRPDEN}	MIN = WL + 4 + t_{WR}/t_{CK} (AVG)						CK	
	BC4MRS	t_{WRPDEN}	MIN = WL + 2 + t_{WR}/t_{CK} (AVG)						CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t_{WRAPDEN}$	MIN = WL + 4 + WR + 1						CK	
	BC4MRS	$t_{WRAPDEN}$	MIN = WL + 2 + WR + 1						CK	

continued on next page

TABLE 25 – AC TIMING PARAMETERS (continued)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Power-Down Exit Timing									
DLL on, any valid command, or DLL off to commands not requiring locked DLL	t_{XP}	MIN = greater of 3CK or 7.5ns; MAX = n/a				MIN = greater of 3CK or 6ns; MAX = n/a		CK	
Precharge power-down with DLL off to commands requiring a locked DLL	t_{XPDLL}	MIN = greater of 10CK or 24ns; MAX = n/a						CK	28
ODT Timing									
R_{TT} synchronous turn-on delay	ODTL on	CWL + AL - 2CK						CK	38
R_{TT} synchronous turn-off delay	ODTL off	CWL + AL - 2CK						CK	40
R_{TT} turn-on from ODTL on reference	t_{AON}	–400	400	–300	300	–250	250	ps	23, 38
R_{TT} turn-off from ODTL off reference	t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)	t_{AONPD}	MIN = 2; MAX = 8.5						ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)	t_{AOFPD}	MIN = 2; MAX = 8.5						ns	40
ODT HIGH time with WRITE command and BL8	ODTH8	MIN = 6; MAX = n/a						CK	
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = n/a						CK	
Dynamic ODT Timing									
R_{TT}_NOM-to-R_{TT}_WR change skew	$ODTL_{CNW}$	WL - 2CK						CK	
R_{TT}_WR-to-R_{TT}_NOM change skew - BC4	$ODTL_{CNW4}$	4CK + ODTL off						CK	
R_{TT}_WR-to-R_{TT}_NOM change skew - BL8	$ODTL_{CNW8}$	6CK + ODTL off						CK	
R_{TT} dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing									
First DQS, DQS# rising edge	t_{WLMRD}	40	–	40	–	40	–	CK	
DQS, DQS# delay	$t_{WLDQSEN}$	25	–	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	t_{WLS}	325	–	245	–	195	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	t_{WLH}	325	–	245	–	195	–	ps	
Write leveling output delay	t_{WLO}	0	9	0	9	0	9	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	0	2	ns	

AC Overshoot/Undershoot Specification

Table 26 – Control and Address Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure 14)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 15)	0.4V	0.4V	0.4V
Maximum overshoot area above V_{CC} (see Figure 14)	0.67 Vns	0.5 Vns	0.4 Vns
Maximum undershoot area below V_{SS} (see Figure 15)	0.67 Vns	0.5 Vns	0.4 Vns

Table 27 – Clock, Data, Strobe, and Mask Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure 14)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 15)	0.4V	0.4V	0.4V
Maximum overshoot area above V_{CC}/V_{CCQ} (see Figure 14)	0.25 Vns	0.19 Vns	0.15 Vns
Maximum undershoot area below V_{SS}/V_{SSQ} (see Figure 15)	0.25 Vns	0.19 Vns	0.15 Vns

FIGURE 14 – OVERSHOOT

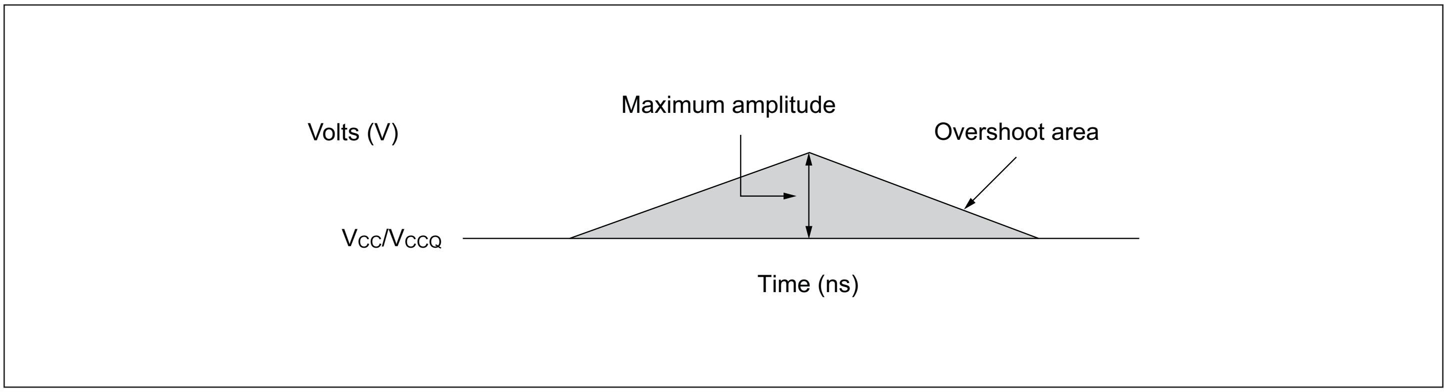
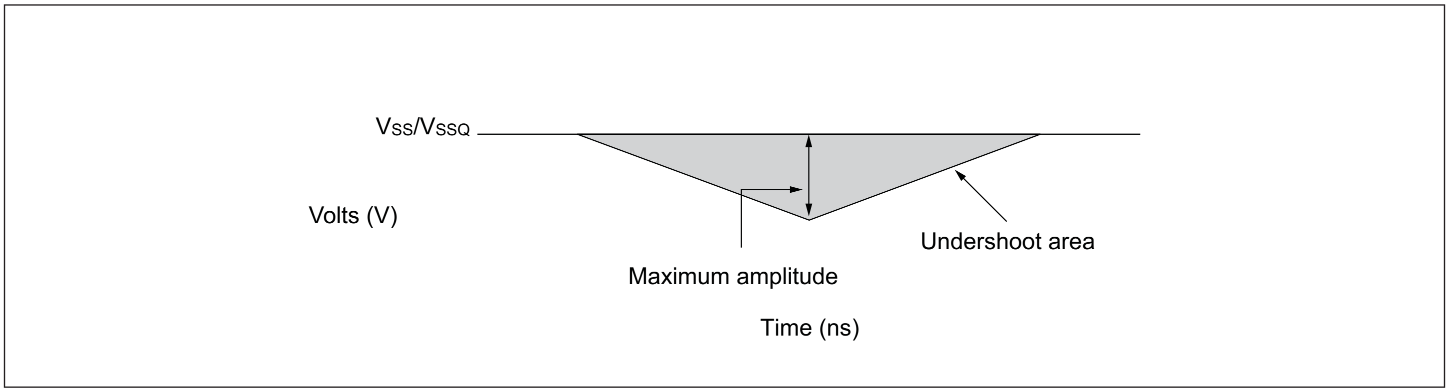


FIGURE 15 – UNDERSHOOT

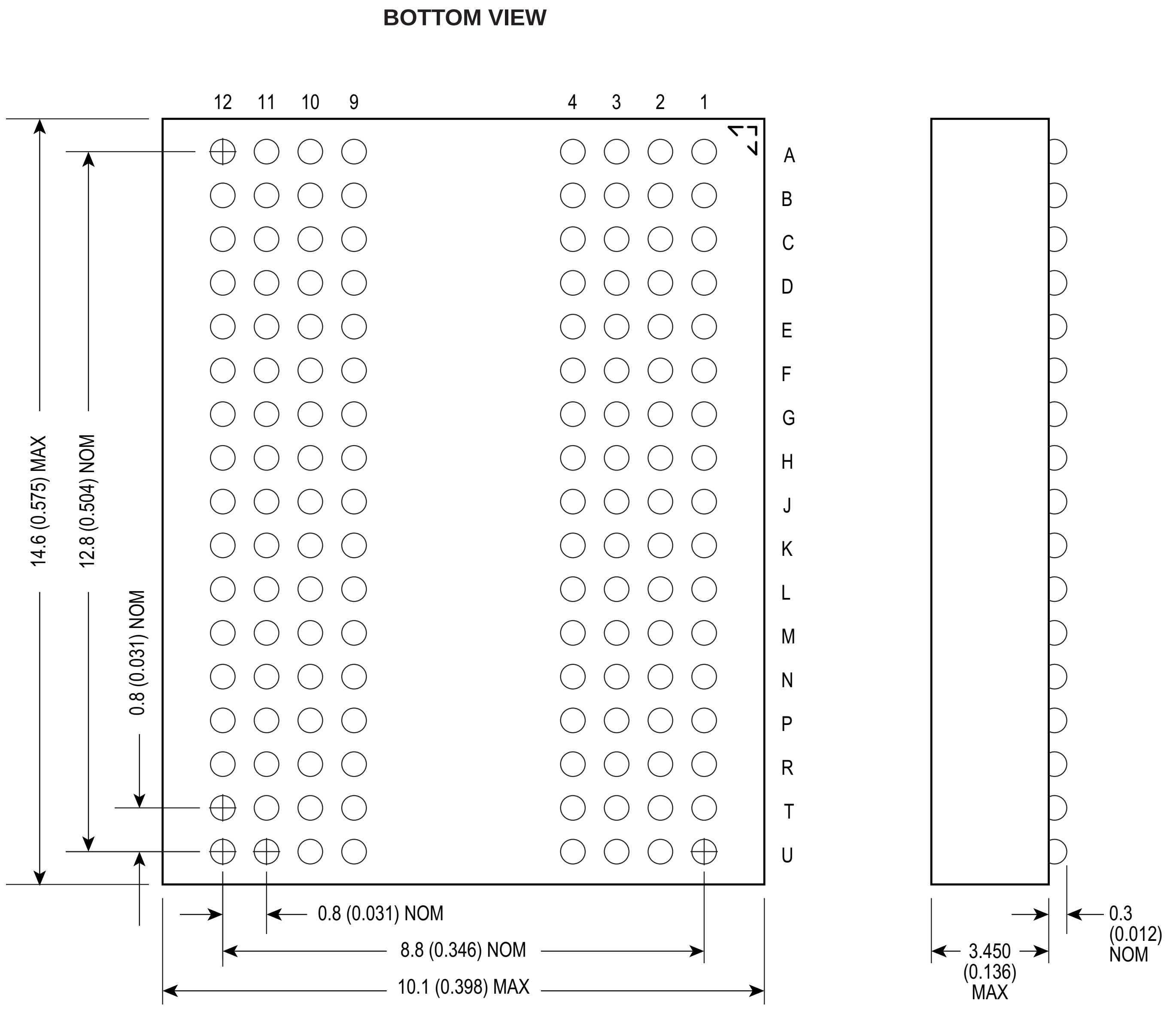


NOTES:

1. Parameters are applicable with V_{CC}/V_{CCQ} = +1.35V ±0.075V.
2. All voltages are referenced to VSS.
3. Output timings are only valid for RON34 output buffer selection.
4. Unit "t_{CK} (AVG)" represents the actual t_{CK} (AVG) of the input clock under operation. Unit "CK" represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{CC} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except t_{IS}, t_{IH}, t_{DS}, and t_{DH} use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
6. All timings that use time-based values (ns, µs, ms) should use t_{CK} (AVG) to determine the correct number of clocks (AC Operation Table). In the case of non integer results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. The use of "strobe" or "DQSDIFF" refers to the DQS and DQS# differential crossing point when DQS is the rising edge. The use of "clock" or "CK" refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{CCQ/2}$ for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, Microsemi does not warrant compliance with normal mode timings or functionality.
10. The clock's $t_{CK\ (AVG)}$ is the average clock over any 200 consecutive clocks and $t_{CK(AVG)}$ MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1 percent of t_{CK} (AVG) as a long-term jitter component; however, the spread-spectrum may not use a clock rate below t_{CK} (AVG) MIN.
12. The clock's $t_{CH\ (AVG)}$ and $t_{CL\ (AVG)}$ are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (t_{JITPER}) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. tCH(ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. tCL(ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter (t_{JITCC}) is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error ($t_{ERRnPER}$), where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
18. t_{DS} (base) and t_{DH} (base) values are for a single-ended 1 V/ns DQ slew rate and 2 V/ns differential DQS, DQS# slew rate.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJITPER of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting $t_{ERR10PER}$ (MAX): t_{DQSCK} (MIN), t_{LZ} (DQS)MIN, t_{LZ} (DQ) MIN, and t_{AON} (MIN). The following parameters are required to be derated by subtracting $t_{ERR10PER}$ (MIN): t_{DQSCK} (MAX), t_{HZ} (MAX), t_{LZ} (DQS)MAX, t_{LZ} (DQ) MAX, and t_{AON} (MAX). The parameter t_{RPRE} (MIN) is derated by subtracting t_{JITPER} (MAX), while t_{RPRE} (MAX) is derated by subtracting t_{JITPER} (MIN).
24. The maximum preamble is bound by t_{LZDQS} (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The t_{DQSCK} (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by t_{HZDQS} (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency t_{XPDLL}, timing must be met.
29. t_{IS} (base) and tIH (base) values are for a single-ended 1 V/ns control/command/ address slew rate and 2 V/ns CK, CK# differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports $t_{nPARAM\ (nCK)} = RU(t_{PARAM\ [ns]}/t_{CK[AVG]\ [ns]})$, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP\ (nCK)} = RU(t_{RP}/t_{CK[AVG]})$ if all input clock jitter specifications are met. This means for DDR3-800 6-6-6, of which t_{RP} = 15ns, the device will support $t_{nRP} = RU(t_{RP}/t_{CK[AVG]})$ = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until t_{RAS} (MIN) has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for t_{WR}.
34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS and OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms up to +85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands must be asserted at least once every 70.3µs.
37. Although CKE is allowed to be registered LOW after a REFRESH command when $t_{REFPDEN}$ (MIN) is satisfied, there are cases where additional time such as t_{XPDLL} (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on.
39. Half-clock output parameters must be derated by the actual $t_{ERR10PER}$ and t_{JITDTY} when input clock jitter is present. This results in each parameter becoming larger. The parameters t_{ADC} (MIN) and t_{AOF} (MIN) are each required to be derated by subtracting both $t_{ERR10PER}$ (MAX) and t_{JITDTY} (MAX). The parameters t_{ADC} (MAX) and t_{AOF} (MAX) are required to be derated by subtracting both $t_{ERR10PER}$ (MAX) and t_{JITDTY} (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. This output load is used for ODT timings.
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than t_{RFC} (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

    For example, for DDR3-800, two input AC levels are defined: $VIH_{(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with $t_{IS(AC175)}$ of 200ps or $V_{IH(AC150),min}$ with $t_{IS(AC150)}$ of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with $t_{DS(AC175)}$ of 75ps or $V_{IH(AC150),min}$ with $t_{DS(AC150)}$ of 125ps.

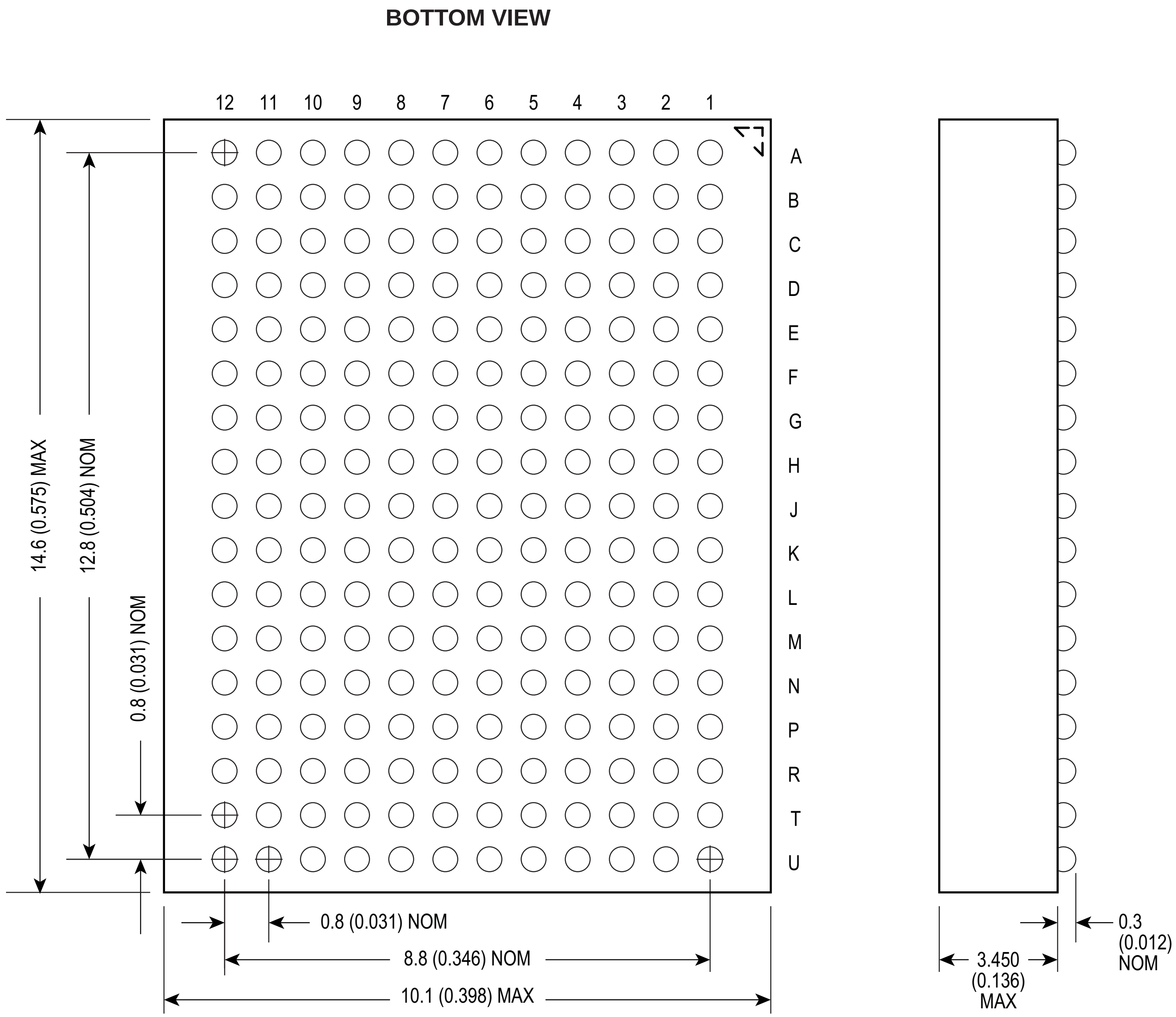
FIGURE 16 – PACKAGE DIMENSION: 136 PLASTIC BALL GRID ARRAY (PBGA) for W3J512M32KT-XBX



- Pads are Solder Mask Defined (SMD), pads openings: 0.4mm

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

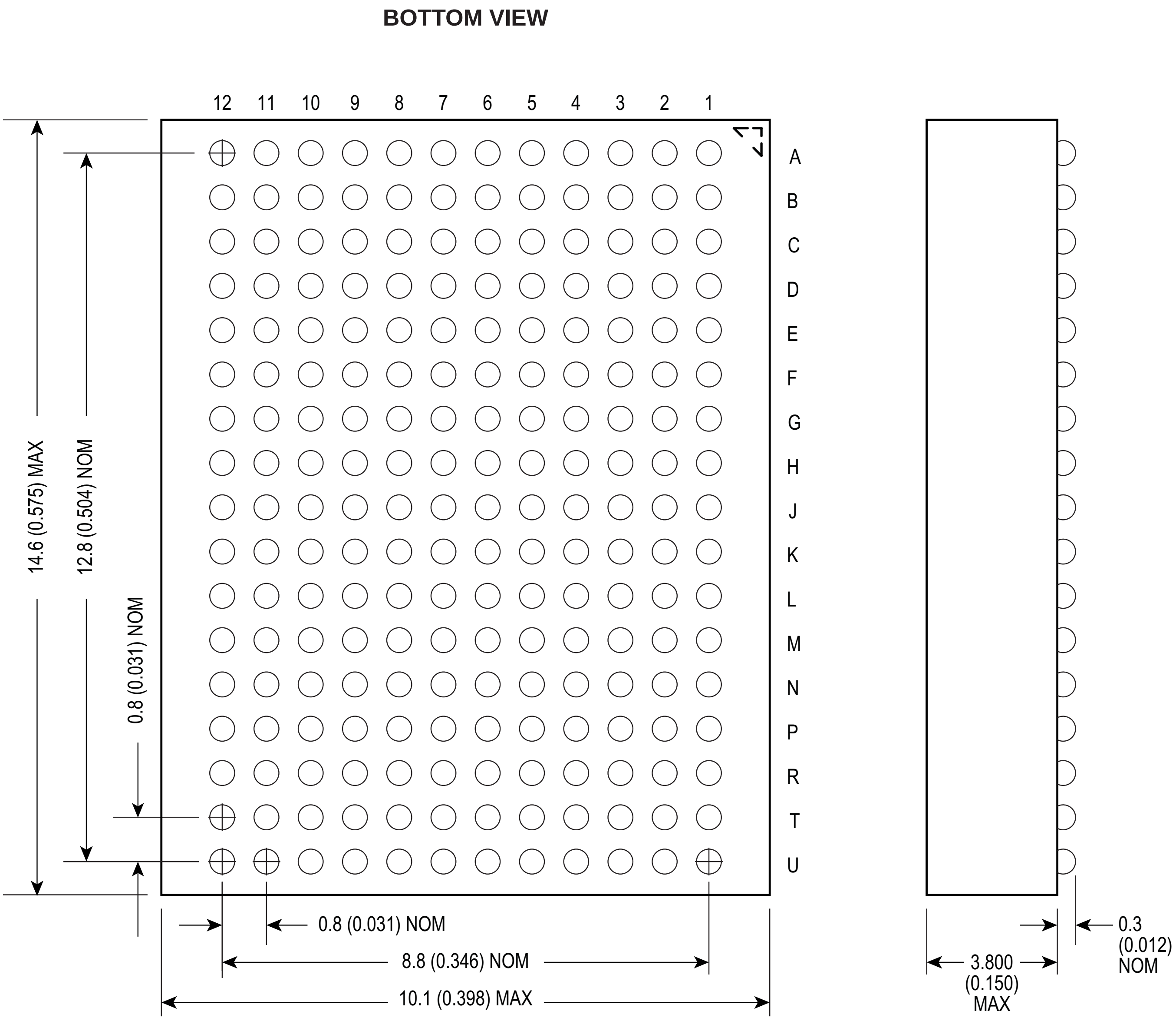
FIGURE 16A – PACKAGE DIMENSION: 204 PBGA, for W3J512M32T-XB2X



- Pads are Solder Mask Defined (SMD), pads openings: 0.4mm

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIGURE 16B – PACKAGE DIMENSION: 204 PBGA, for W3J512M40K(T)-XB3X



- Pads are Solder Mask Defined (SMD), pads openings: 0.4mm

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W 3J 512M XX K T - XXXX XX X

MICROSEMI CORPORATION:

DDR3 SDRAM:

CONFIGURATION, 512M x32 or x40:

1.35V POWER SUPPLY:

OPTIONAL:
T = Address/Control Termination resistors included

DATA RATE (Mb/s):
800 = 800Mb/s
1066 = 1,066Mb/s
1333 = 1,333Mb/s

PACKAGE:
B = 136 Plastic Ball Grid Array (PBGA) – only x32 with no address/control termination, no clock termination, with calibration resistors.
B2 = 204 PBGA, x32 with clock termination, with calibration resistors with address/control termination. Only option available is 512M32KT.
B3 = 204 PBGA, x40 configuration with clock termination, with calibration resistors, with optional address/control termination.

DEVICE GRADE:

M	=	Military**	-55°C to +125°C
I	=	Industrial	-40°C to +85°C
C	=	Commercial	0°C to +70°C

** Contact factory for availability

Document Title

2GB – 512M x 32/40 DDR3 SDRAM 1.35V – 136/204 PBGA Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	April 2014	Preliminary
Rev 1	Change (Pg. 1) 1.1 Change W3J512M36K(T)-XB2X to W3J512M32K(T)-XB2X "B2" package is for X32 with termination.	June 2014	Preliminary
Rev 2	Changes (Pg. 1, 3, 4, 40, 41, 42, 43) 2.1 Remove all reference to x36 package 2.2 Remove functional block diagram for x36 configuration 2.3 "B2" package only available in x32 bit data configuration with address/control terminations	September 2014	Preliminary
Rev 3	Changes (Pg. 23) 3.1 Correct Table 7 "Bank Activate" values for RAS#, CAS# and WE#	December 2014	Preliminary