TRW | LSI MULTIPLIERS HJ SERIES

N X N BIT PARALLEL MULTIPLIERS, N =8, 12, 16, or 24
COMMERCIAL/MILITARY TEMPERATURE RANGES
PRELIMINARY

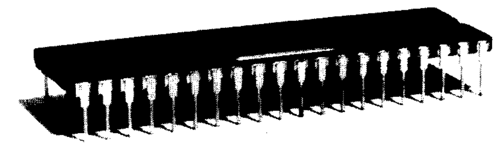
004333

The MPY LSI multipliers are high speed, TTL LSI devices. They are n-by-n parallel array multipliers with double precision outputs. Their low power and high performance characteristics are the result of a proven method developed and patented by TRW (U.S. Patent No. 3,900,724). Fundamental TTL devices used to produce the MPY-LSI were also developed and patented by TRW (U.S. Patent No. 3,283,170). The major multiplier array logic achieves speed-power performance of less than 1 picojoule per equivalent gate.

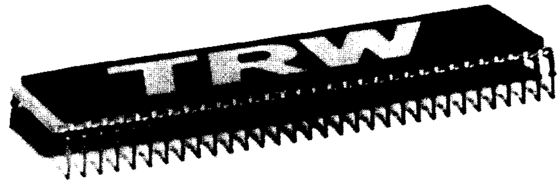
Four input/output registers are used in the MPY LSI multipliers. These registers are D-type flip-flops with a single phase TTL clock.

Applications for MPY LSI multipliers include digital processing and high speed multiplication for fast Fourier transforms. They are ideal for extending the capabilities of mini/microcomputers, permitting hardware multiplication for increased computational speed.

They have a better than 2-to-1 speed-power improvement over the MPY AJ series multipliers.



MPY–8HJ



MPY–12HJ, MPY–16HJ, and MPY–24HJ

FEATURES

- n-by-n parallel array multiplier, n = 8, 12, 16, or 24
- Double precision product
- 45 to 200 nsec typical multiply time
- Much lower power/less space than MSI equivalent multipliers
- Includes input/output registers
- Single chip, bipolar TTL technology
- Single bus or multiport operation
- Radiation hard
- Three-state outputs
- Single power supply, +5V

NEW FEATURES OF HJ SERIES

- Higher speed/lower power
- Zero-nanosecond register hold time
- Two's complement, unsigned magnitude, or mixed-mode multipliers (all except MPY-8HJ)
- Easily expandable for larger array multiplication
- Worst case specs across full voltage and temperature ranges
- Controllable, transparent product registers (all except MPY-8HJ)
- Shift/normalize product capability (MPY-24HJ)
- Pin-compatible with AJ series multipliers

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GENERAL INFORMATION

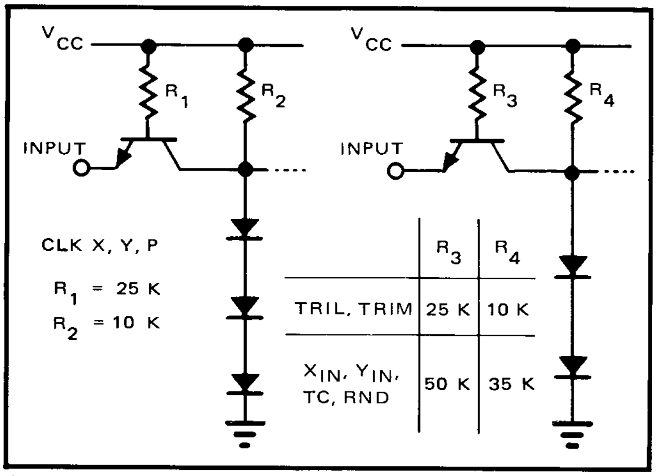


Figure 1. Equivalent Input Schematics

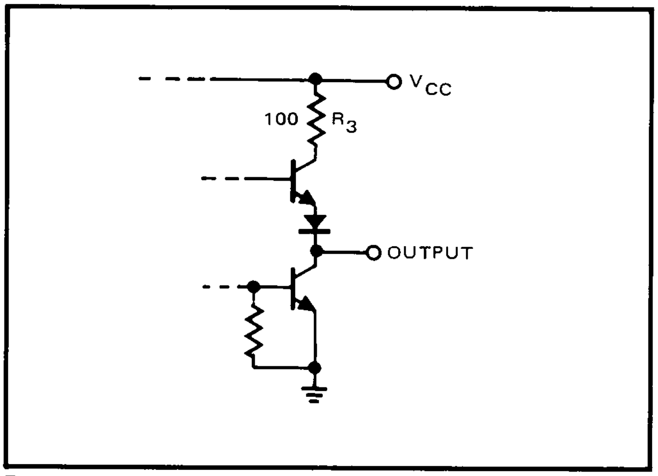


Figure 2. Output Schematic

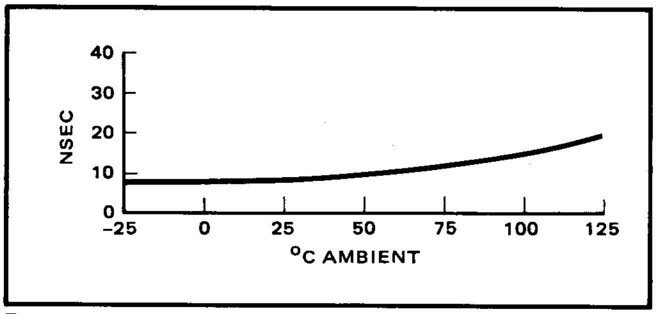


Figure 3. Typical Setup Time

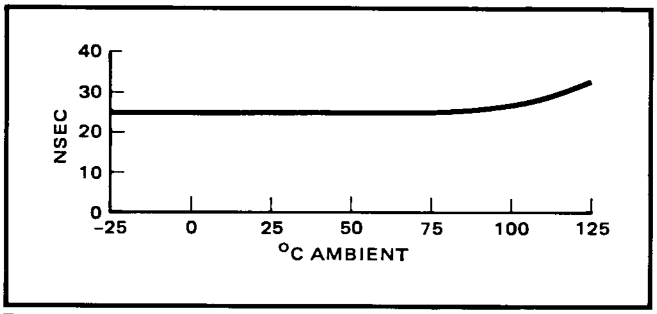


Figure 4. Typical Three-State Delay, Output Delay

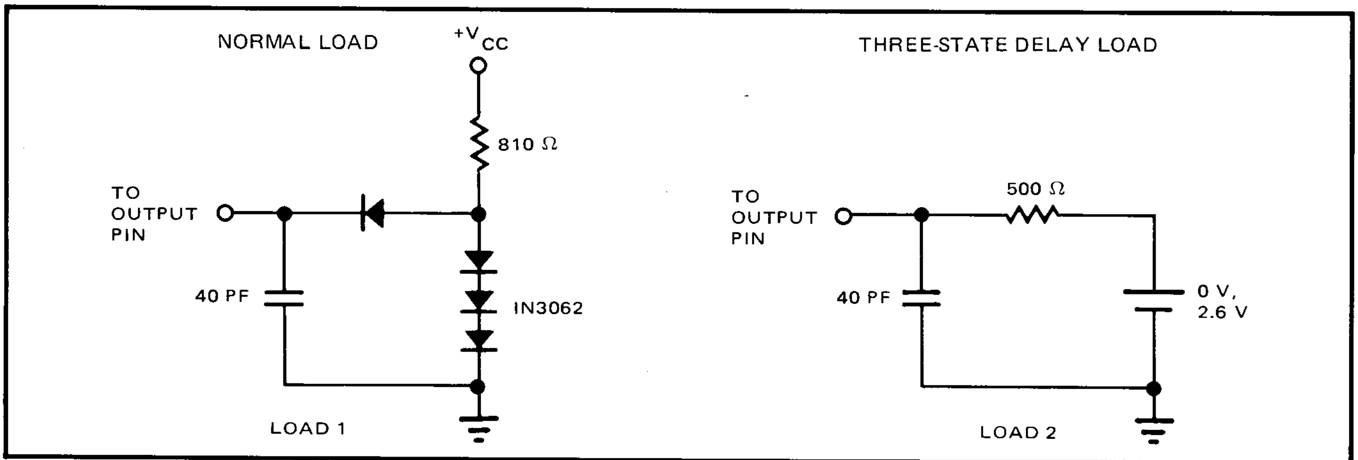


Figure 5. Test Loads for Delay Measurements

SOCKET INFORMATION

TYPE	40 PIN	64 PIN
Wire wrap	Excel 800B-003-40	Excel 800B-003-64
Solder tail-tin plate	Cambion 703-4040-01-04-12	Cambion 703-4064-01-04-12
Solder tail-gold plate	Robinson Nugent ICN-406-S5-G	Robinson Nugent ICN-649-S5-G
Zero insertion force	Textool 240-3346-00-0605	Textool 232-2601-00-0605 (2 Required)

GENERAL SPECIFICATIONS

Absolute maximum ratings (above which the useful life may be impaired)

Supply voltage . . . . -0.5 to 7.0 V
Input voltage . . . . 0 to 5.5 V
Output voltage . . . . 0 to 5.5 V
Operating temperature range (Tcase). . . . . -55°C to 125°C
Storage temperature range. . . . . -65°C to 150°C
Lead temperature (10 seconds) . . . . 300°C
Junction temperature. . . . . 175°C

Part Numbers

Commercial	Military
MPY-8HJ	MPY-8HJM
MPY-8HJ-1	—
MPY-12HJ	MPY-12HJM
MPY-16HJ	MPY-16HJM
MPY-24HJ	MPY-24HJM

Recommended operating conditions

	COMMERCIAL			MILITARY			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
High-level output current, I_{OH}			-0.4			-0.4	mA
Low-level output current, I_{OL}			4.0			4.0	mA
Clock pulse width, t_{PW} (measured at 1.5 V level)	25			30			nsec
Input register setup time, t_S (see Figure 6)	25			30			nsec
Input register hold time, t_H (see Figure 6)	0			0			nsec
Operating temperature ($T_{ambient}$ for commercial, T_{case} for military)	0		70	-55		125	°C

Electrical characteristics over recommended temperature range (except as otherwise noted)

PARAMETER		TEST CONDITIONS		COMMERCIAL			MILITARY			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2.0			2.0			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -0.4 mA	2.4	2.7		2.4	2.7		V
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 4.0 mA		0.3	0.5		0.3	0.5	V
I_{IH}	High-level input current	V_{CC} = MAX	V_{IH} = 2.4			75			75	μA
I_{IL}	Low-level input current	V_{CC} = MAX	V_{IL} = 0.4			-0.4			-0.4	mA
I_{IH}	Clocks*, three-states— high level input current	V_{CC} = MAX	V_{IL} = 2.4			75			75	μA
I_{IL}	Clocks*, three-states— low level input current	V_{CC} = MAX	V_{IL} = 0.4			-1.0			-1.0	mA

*NOTE: Clock P is two equivalent clock loads.

Switching characteristics across V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS	TYP**	MAX		UNIT
			COMMERCIAL	MILITARY	
Output delay t_D	Load 1 (see Figure 5)	25	35	40	nsec
Three state output delay Output enable, t_{ENA}, Output disable, t_{DIS}	Load 2 (see Figure 5)	25	35	40	nsec

**NOTE: At V_{CC} = 5.0 V, T_A = 25°C.

MPY-8HJ
8 X 8 BIT PARALLEL MULTIPLIER

The MPY-8HJ multiplier is a high speed, TTL LSI device. It is a parallel two's complement multiplier with double precision output. It can be plugged into an MPY-8AJ socket, and be functionally equivalent. However, this newer multiplier has positive setup and zero hold times, which reduces system clocking complexity in many applications. Also, the RND control is now a registered input, making its timing and usage more convenient.

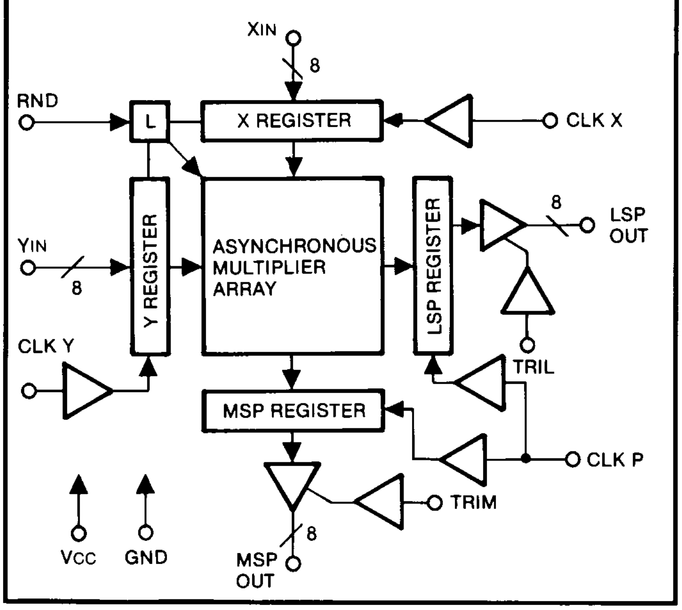
Four input/output registers are used in the MPY-8HJ multipliers. These registers are D-type flip-flops with a single phase TTL clock.

Applications for the MPY-8HJ multipliers include digital processing and high speed multiplication for fast, nonrecursive filters. They are ideal for extending the capabilities of mini/microcomputers, permitting hardware multiplication for increased computational speed, and are particularly useful for video processing.

FEATURES

- 8-by-8 parallel, two's complement multiplier
- Double precision product
- 65 nsec typical multiply time (MPY-8HJ)
- 45 nsec typical multiply time (MPY-8HJ-1)
- Much lower power than MSI equivalent multipliers
- Includes input/output positive edge-triggered registers
- Single chip, bipolar technology
- Single bus or multiport operation
- Radiation hard
- TTL input and output
- Three state outputs
- Single power supply, +5V
- 40 pin dual in-line package
- Pin compatible with MPY-8AJ
- Zero hold time on input registers

MPY–8HJ LOGICAL BLOCK DIAGRAM



CONTROLS
(Positive logic unless otherwise noted)

CLK X – X_{IN} Register Clock

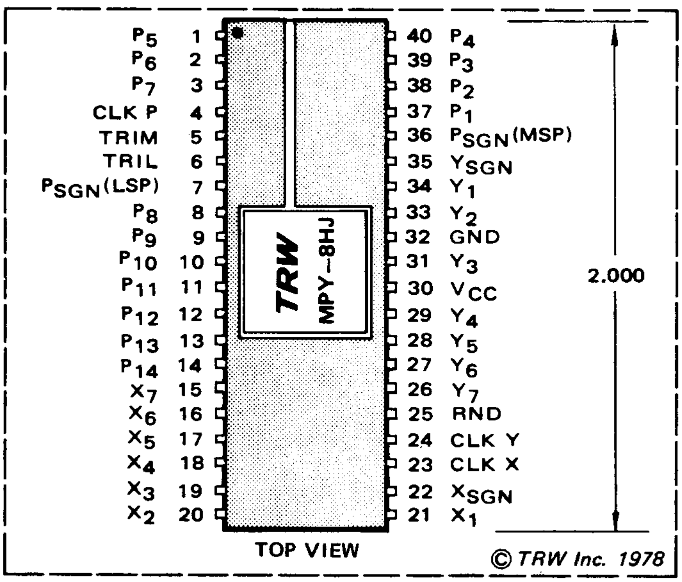
CLK Y – Y_{IN} Register Clock

CLK P – Product Registers Clock

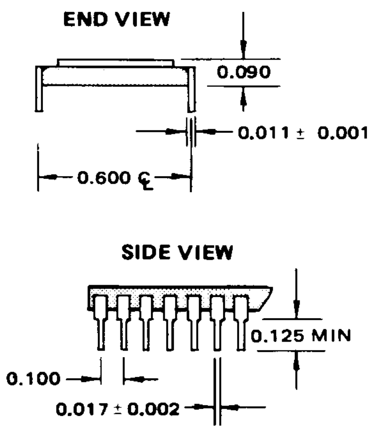
TRIL – LSP Three-State Control,
TRIM – MSP Three-State Control,
LOGIC 0 = Enable, LOGIC 1 = Disable

RND (LOGIC 1) – Adds 2^{-8} to product (fractional two's complement field – See Page 5 for I/O Format)

RND Latch is strobed by (CLK X or CLK Y)



PACKAGE INFORMATION



NOTE
DIMENSIONS IN INCHES

THERMAL CHARACTERISTICS

θ_{CA}(Still air) = 25°C/W

θ_{CA}(300 cfm) = 15°C/W

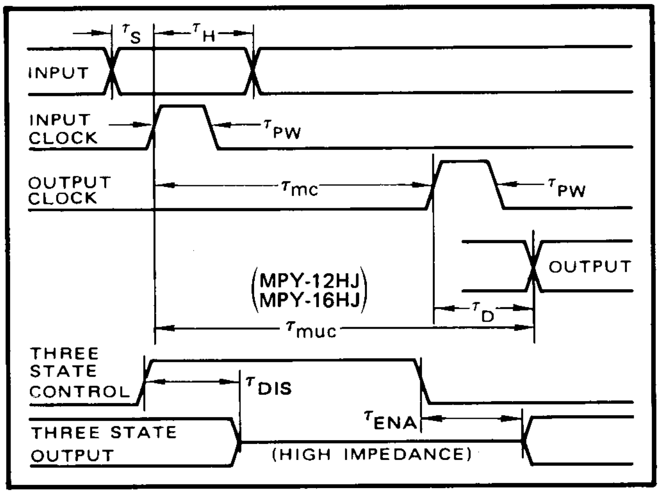


Figure 6. Timing Diagram

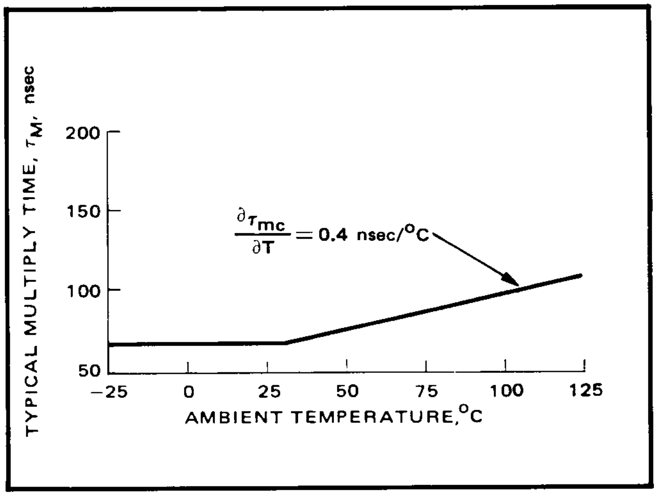


Figure 7. Multiply Time Versus Temperature

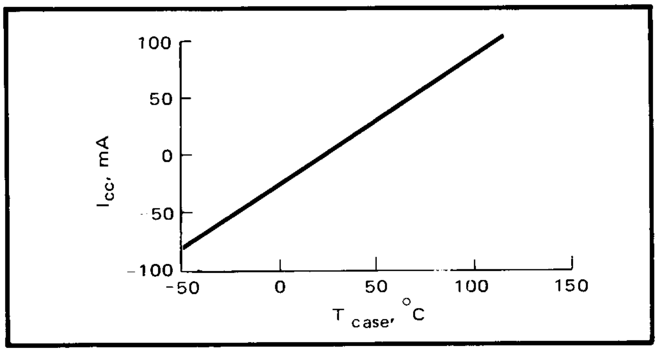


Figure 8. $T_{ambient}$ Versus T_{case}

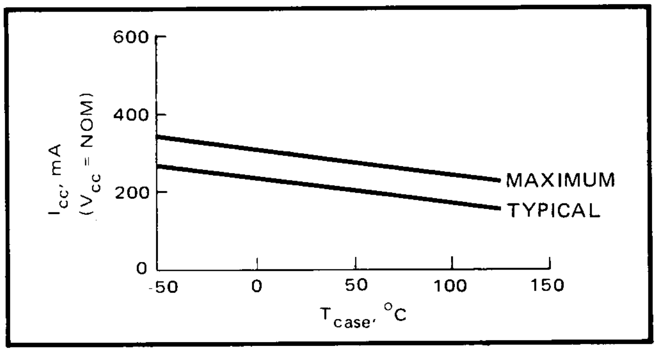


Figure 9. I_{CC} Versus T_{case}

Electrical and switching characteristics over recommended V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS		TYP*	MAX		UNIT
				COMMERCIAL	MILITARY	
MPY–8HJ Multiply time, τ_{mc}	See Figures 6, 7		65	90	115	nsec
MPY–8HJ–1 τ_{mc}	See Figure 6	T_A = 60°C	45	60	–	nsec
		T_A = 70°C	45	65	–	nsec
Supply current I_{CC}	See Figure 9		200	270	330	mA

* NOTE: At V_{CC} = 5.0 V, T_A = 25°C

INPUT/OUTPUT FORMAT FOR FRACTIONAL TWO'S COMPLEMENT FIELD

X_{IN}								Y_{IN}							
X SGN	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y SGN	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}
								-2^0	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}
P SGN	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P SGN	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}
MSP								LSP							

An overflow occurs in the attempted multiplication of the two's complement number 1.000 . . . . (–1 base 10) with itself, yielding a result of the same number, i.e., $(-1)_{10} * (-1)_{10} = (-1)_{10}$

MPY-12HJ and MPY-16HJ

12 X 12 and 16 X 16 BIT PARALLEL MULTIPLIERS

The MPY-12HJ and MPY-16HJ multipliers are high speed TTL compatible LSI devices. They are N-by-N parallel array multipliers with double precision or single precision (uniform rounded or truncated) outputs.

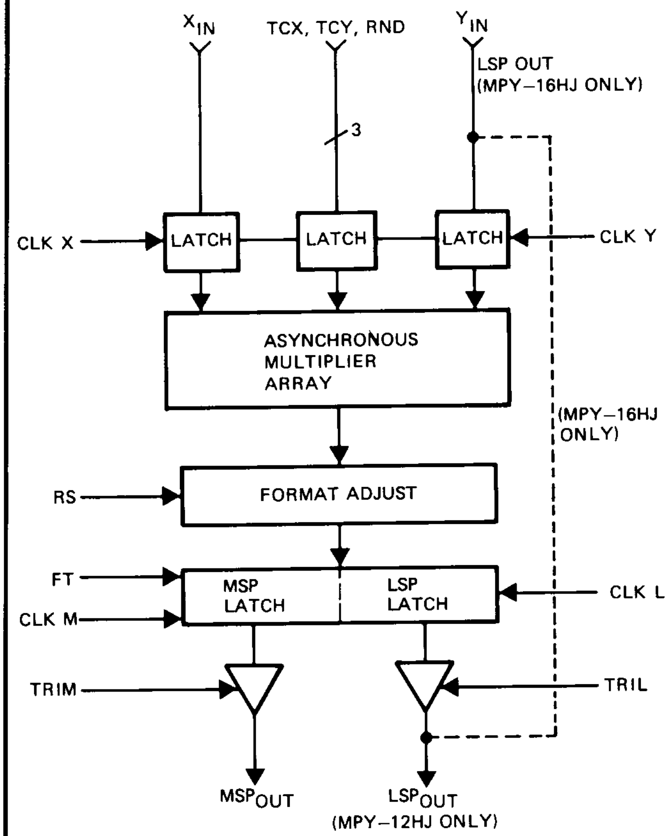
The input registers are positive edge-triggered latches. The output latches are similarly positive edge-triggered latches, with a feedthrough control line, which allows the user to bypass the registers completely, making them asynchronous. If the output clocks are disabled, then the feedthrough control can be used to convert the output registers to level latches.

Applications for these multipliers include high speed digital signal processing, such as Fourier transforms, FIR and IIR filters, and linear predictive algorithms. They are ideal for upgrading the capabilities of mini and microcomputers, permitting hardware multiplication for increased computational speed at low cost. They can also be added on a retrofit basis to older signal processors, decreasing system power and size, while increasing reliability and (in many cases) system throughput.

These multipliers can be plugged into MPY-12AJ and MPY-16AJ sockets, and be functionally equivalent. However, these newer multipliers have positive setup and zero hold times, which reduces system clocking complexity in many applications. The RND control is now a registered input, making its timing and usage more convenient.

The multipliers can operate with two's complement, unsigned magnitude, and mixed mode input formats. As such, they are ideal for expansion into larger multipliers, such as 32 by 32 bits, or 36 by 36 bits.

MPY–12HJ and MPY–16HJ
LOGIC BLOCK DIAGRAM



FEATURES

- 12 x 12 (MPY-12HJ) or 16 x 16 (MPY-16HJ) parallel array multiplier
- Double precision output
- 80 nsec (MPY-12HJ), 100 nsec (MPY-16HJ) multiply time
- Two's complement, unsigned magnitude, or mixed mode multiplies
- Positive edge-triggered input latches
- Output latches positive edge-triggered or transparent
- Three-state outputs
- Pin compatible with MPY-12AJ or MPY-16AJ
- Two output formats

CONTROLS

(Positive logic unless otherwise noted)

CLK X – X_{IN} Register Clock

CLK Y – Y_{IN} Register Clock

CLK L – LSP Register Clock

CLK M – MSP Register Clock

TRIL – LSP Three-State Control,
TRIM – MSP Three-State Control,
RS – Right Shift MSP word down 1 bit, removes LSP SIGN bit.
FT (Feedthrough) – Makes output latch transparent

TCX, TCY – Denotes respective input words as two's complement (logic 1) or magnitude (logic 0) data format (registered control inputs strobed by respective clocks)

ROUND – ADDS 1 to MSB bit of LSP word, regardless of shift position (registered control input strobed by [CLK X or CLK Y]).

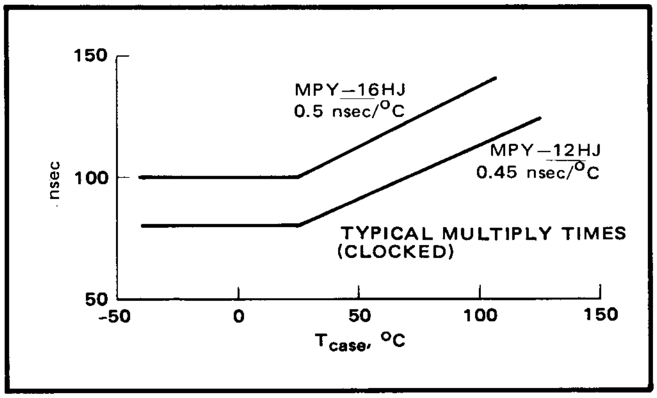


Figure 10. Multiply Time Versus Temperature

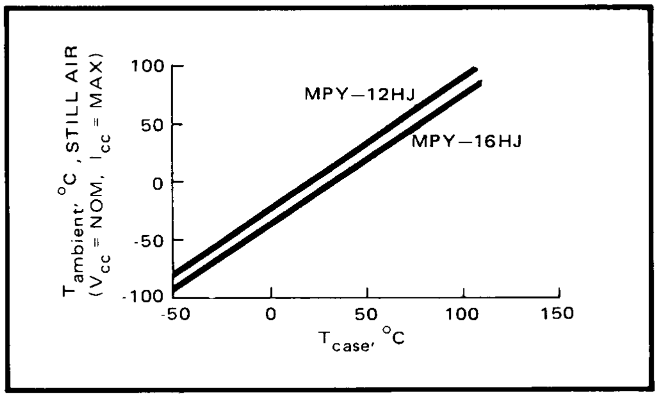


Figure 11. $T_{ambient}$ Versus T_{case}

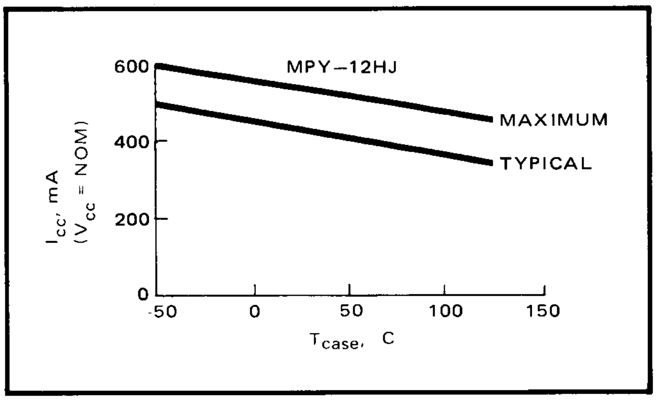


Figure 12. I_{CC} Versus T_{case}

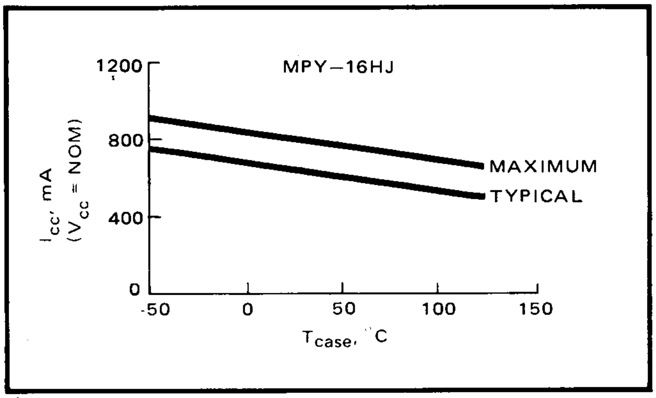


Figure 13. I_{CC} Versus T_{case}

Electrical and switching characteristics over V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS	DEVICE	TYP*	COMMERCIAL	MILITARY	UNIT
Clocked multiply time τ_{mc}	See Figure 6	MPY-12	80	110	140	nsec
		MPY-16	100	140	185	nsec
Unclocked multiply time, τ_{muc}	See Figure 6	MPY-12	105	145	180	nsec
		MPY-16	125	175	225	nsec
I_{CC} supply current		MPY-12 see Figure 12	400	540	600	mA
		MPY-16 see Figure 13	600	800	900	mA

*NOTE: At $V_{CC} = 5.0$ V, $T_A = 25°C$

INPUT/OUTPUT FORMATS

FRACTIONAL TWO'S COMPLEMENT

X_{IN} — TCX = 1

X_{11}	X_{10}	X_9	…	X_2	X_1	X_0
X SGN	2^{-1}	2^{-2}		2^{-9}	2^{-10}	2^{-11}

TCY = 1 — Y_{IN}

Y_{11}	Y_{10}	Y_9	…	Y_2	Y_1	Y_0
Y SGN	2^{-1}	2^{-2}		2^{-9}	2^{-10}	2^{-11}

MSP

	P_{23}	P_{22}	P_{21}	…	P_{14}	P_{13}	P_{12}
RS = 0	-2^0 SGN	2^{-1}	2^{-2}		2^{-9}	2^{-10}	2^{-11}
RS = 1	-2^1 SGN	2^0	2^{-1}		2^{-8}	2^{-9}	2^{-10}

LSP

	P_{11}	P_{10}	P_9	…	P_2	P_1	P_0
RS = 0	-2^0 SGN	2^{-12}	2^{-13}		2^{-20}	2^{-21}	2^{-22}
RS = 1	2^{-11}	2^{-12}	2^{-13}		2^{-20}	2^{-21}	2^{-22}

$$X = -1 * X_{SIGN} + \sum_{n=1}^{11} X_n 2^{-n} \qquad P = -1 * P_{SIGN} + \sum_{n=1}^{22} P_n 2^{-n}$$

The resulting values for X and P given in the above evaluations (Y is expressed in the same manner as X) are in fractional two's complement format. The value for the sign variable is 0 for positive or zero numbers and 1 for negative numbers.

RS = 0 An overflow occurs in the attempted multiplication of the two's complement number 1.0000 . . . (−1 base 10) with itself, yielding a result of the same number, i.e.,

$$(-1)_{10} * (-1)_{10} = (-1)_{10}$$

The product sign bit is available redundantly as the MSB of both the MSP and LSP words.

RS = 1 No overflow occurs when multiplying $-1_{(10)}$ times $-1_{(10)}$. The product is a true $+1.0_{(10)}$; i.e., product bit P_{22} is a 1, all other bits are 0.

INTEGER MAGNITUDE

X_{IN} — TCX = 0

X_{11}	X_{10}	X_9	…	X_2	X_1	X_0
2^{11}	2^{10}	2^9		2^2	2^1	2^0

TCY = 0 — Y_{IN}

Y_{11}	Y_{10}	Y_9	…	Y_2	Y_1	Y_0
2^{11}	2^{10}	2^9		2^2	2^1	2^0

MSP

P_{23}	P_{22}	P_{21}	…	P_{14}	P_{13}	P_{12}
2^{23}	2^{22}	2^{21}		2^{14}	2^{13}	2^{12}

RS = 1

LSP

P_{11}	P_{10}	P_9	…	P_2	P_1	P_0
2^{11}	2^{10}	2^9		2^2	2^1	2^0

Note: (1) When doing unsigned magnitude or mixed mode multiplications, RS must be a 1 to get a valid product.

(2) When doing mixed mode (two's complement times unsigned magnitude) multiplies, P_{23} is the product sign bit.

INPUT/OUTPUT FORMATS

FRACTIONAL TWO'S COMPLEMENT

X_{IN} TCX = 1

X_{15}	X_{14}	X_{13}	…	X_2	X_1	X_0
X SGN	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}

TCY = 1 Y_{IN}

Y_{15}	Y_{14}	Y_{13}	…	Y_2	Y_1	Y_0
Y SGN	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}

MSP / LSP

	P_{31}	P_{30}	P_{29}	…	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	…	P_2	P_1	P_0
RS = 0	-2^0 SGN	2^{-1}	2^{-2}		2^{-13}	2^{-14}	2^{-15}	-2^0 SGN	2^{-16}	2^{-17}		2^{-28}	2^{-29}	2^{-30}
RS = 1	-2^1 SGN	2^0	2^{-1}		2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}		2^{-28}	2^{-29}	2^{-30}

$$X = -1 * X_{SIGN} + \sum_{n=1}^{15} X_n 2^{-n} \qquad P = -1 * P_{SIGN} + \sum_{n=1}^{30} P_n 2^{-n}$$

The resulting values for X and P given in the above evaluations (Y is expressed in the same manner as X) are in fractional two's complement format. The value for the sign variable is 0 for the positive or zero numbers and 1 for negative numbers.

RS = 0 An overflow occurs in the attempted multiplication of the two's complement number 1.0000 . . . (−1 base 10) with itself, yielding a result of the same number, i.e.,

$$(-1)_{10} * (-1)_{10} = (-1)_{10}$$

The product sign bit is available redundantly as the MSB of both the MSP and LSP words.

RS = 1 No overflow occurs when multiplying $-1_{(10)}$ times $-1_{(10)}$. The product is a true $+1.0_{(10)}$; i.e., product bit P_{30} is a 1, all other bits are 0.

INTEGER MAGNITUDE

X_{IN} TCX = 0

X_{15}	X_{14}	X_{13}	…	X_2	X_1	X_0
2^{15}	2^{14}	2^{13}		2^2	2^1	2^0

TCY = 0 Y_{IN}

Y_{15}	Y_{14}	Y_{13}	…	Y_2	Y_1	Y_0
2^{15}	2^{14}	2^{13}		2^2	2^1	2^0

MSP / LSP

	P_{31}	P_{30}	P_{29}	…	P_{18}	P_{17}	P_{16}	P_{15}	P_{14}	P_{13}	…	P_2	P_1	P_0
RS = 1	2^{31}	2^{30}	2^{29}		2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}		2^2	2^1	2^0

Note: (1) When doing unsigned magnitude or mixed mode multiplications, RS must be a 1 to get a valid product.

(2) When doing mixed mode (two's complement times unsigned magnitude) multiplies, P_{31} is the product sign bit.

MPY-24HJ
24 X 24 BIT PARALLEL MULTIPLIER

The MPY-24HJ is a high-speed TTL LSI device. It is a 24 x 24-bit parallel two's complement or magnitude multiplier with a double precision output. Its low power and high performance are the result of circuits developed and patented by TRW. The multiplier array logic achieves a speed-power performance of less than 1 picojoule per gate.

Three registers are used in the MPY-24HJ multiplier. The two 24 bit input registers are positive edge triggered, and have independent clocks. The 48 bit output register is a level-dependent latch. As such, the outputs can be used either synchronously or asynchronously (transparent).

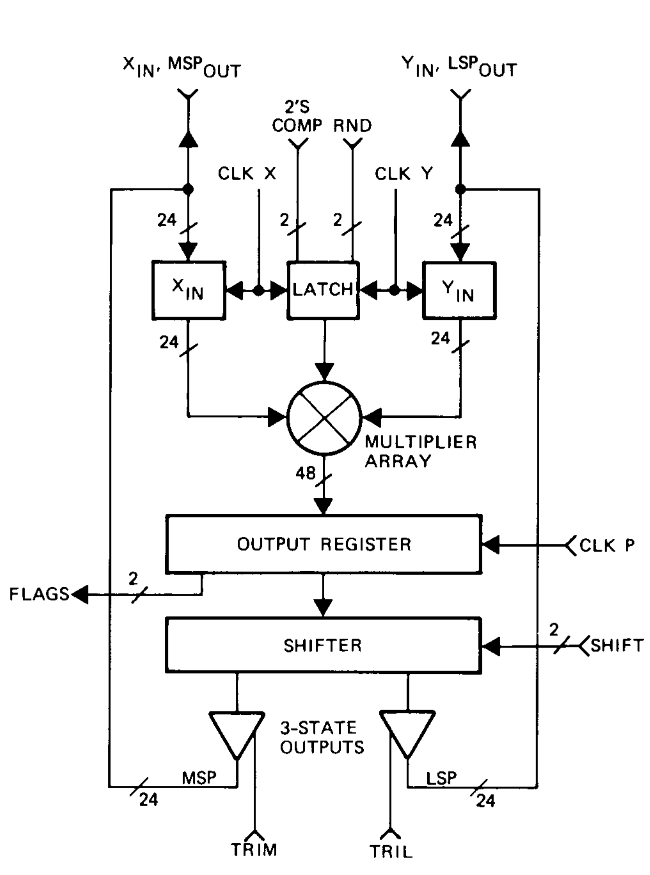
Applications for the MPY-24HJ include high speed, high accuracy digital signal processing, digital filters, and the fast Fourier transform. It is particularly suited to doing the mantissa multiply in floating point multiplication.

The modular architecture of the MPY-24HJ allows straightforward implementation of larger array multipliers such as 48 x 48 bits.

FEATURES

- 24 x 24 bit parallel multiply
- Single chip bipolar technology
- Two's complement or magnitude (can be mixed)
- 200 nsec synchronous multiply
- 225 nsec asynchronous multiply (output register transparent)
- Includes input and output registers
- Much lower power than MSI equivalent multipliers
- Radiation-hard
- Three-state outputs
- Uniform rounding available
- Overflow and normal flags for floating point multiply
- Built-in shifter for floating point normalization or scaling
- TTL inputs and outputs
- Single power supply, +5V

MPY–24HJ LOGIC BLOCK DIAGRAM



CONTROLS
(Positive logic unless otherwise noted)

CLK X – X_{IN} Register Clock

CLK Y – Y_{IN} Register Clock

CLK P – Output Register Clock

TRIL – LSP Three-State Control

TRIM – MSP Three-State Control

SH A, SH B – Shifts the output product zero, one or two bits upward, adds trailing zeros

OVF – Flags the two's complement output as overflowed (see figure 18)

NORM – Flags the two's complement output as already normalized (see figure 18)

RND A, RND B – Adds 1 to one of 3 places

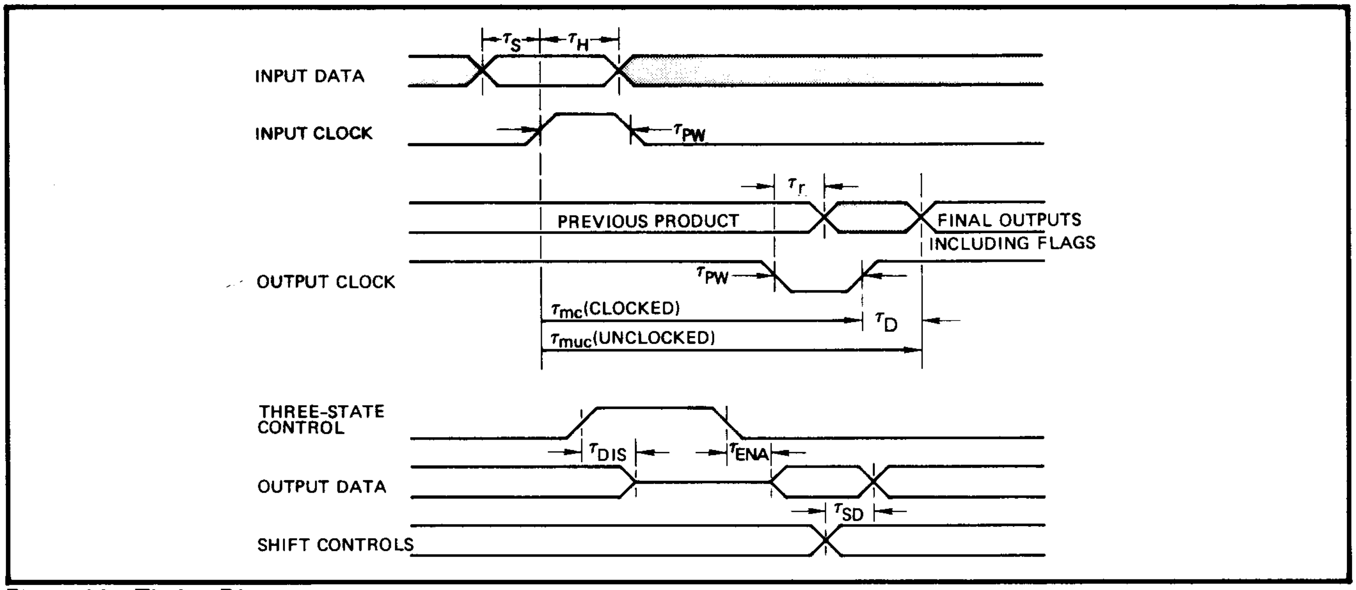


Figure 14. Timing Diagram

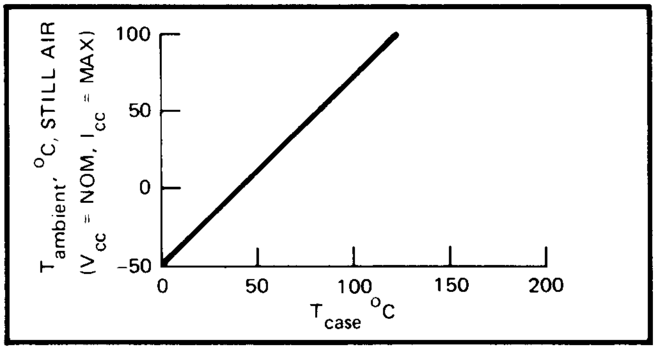


Figure 15. $T_{ambient}$ Versus T_{case}

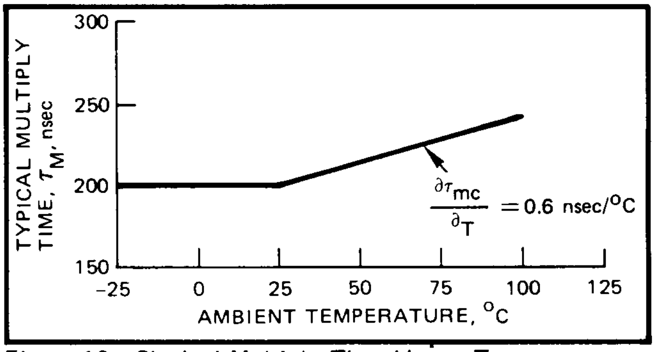


Figure 16. Clocked Multiply Time Versus Temperature

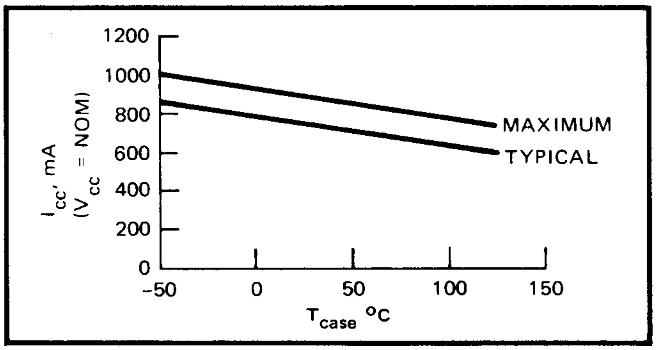


Figure 17. I_{CC} Versus T_{case}

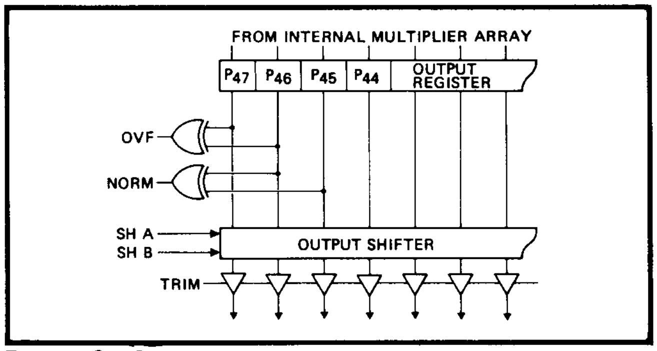


Figure 18. Output Detail

Electrical and switching characteristics over V_{CC} and temperature ranges(except as otherwise noted)

PARAMETER	TEST CONDITIONS	TYP*	MAX COMMERCIAL	MAX MILITARY	UNIT
Clocked multiply time, τ_{mc}	See Figure 14	200	285	320	nsec
Unclocked multiply time, τ_{muc}	See Figure 14	225	325	365	nsec
Shift delay, τ_{SD}	See Figure 14	25	35	40	nsec
CLK P release time, τ_r	See Figure 14	25	35	40	nsec
Supply current, I_{CC}	See Figure 17	700	850	1000	mA

*Note: at V_{CC} = 5.0 V, τ_A = 25°C

CONTROL AND CLOCK TRUTH TABLE AND LOGIC DESCRIPTION

All inputs, outputs, and controls are TTL compatible; positive logic

CONTROL MNEMONIC		LOGIC STATE	FUNCTION	
Data Input/Output			Positive logic, Logic 1 = 1 * 2^n	
CLK X, CLK Y			Loads internal X_{IN}, Y_{IN} register on 0 to 1 transition. Holds data until next 0 to 1 transition. D type register.	
CLK P		↑	Freezes internal output latches on 0 to 1 transition.	
		1	Holds last latched state.	
		↓	Releases latched state to follow mode on 1 to 0 transition.	
		0	Unclocked mode. Output register continuously follows the array product.	
TCX (Mode Control, X input) TCY (Mode Control, Y input)			Registered controls clocked by (CLK X or CLK Y).	
		1	Two's complement number system.	
		0	Unsigned magnitude number system (for expandable case, see text and diagrams)	
OVF		0	Signals P_{47} and P_{46} are of the same state.	
		1	Signals P_{47} and P_{46} are opposite states.	
NORM		0,1	Same as flag overflow for P_{46} and P_{45}.	
SH B	SH A		Direct nonregistered inputs, no effect on flag outputs.	
0	0		No shift, MSP bit has weight of 1 * 2^{47} magnitude notation.	
0	1		Shift up one bit, MSP has weight of 1 * 2^{46}, $P_0 = 0$.	
1	X		Shift up two bits, MSP has weight of 1 * 2^{45}, P_0, $P_1 = 0$.	
RND B	RND A		Registered controls clocked by (CLK X or CLK Y).	
			Two's Complement	Magnitude
0	0		No round.	No round.
0	1		Adds 1 * 2^{-25} to product.	Adds 1 * 2^{21} to product.
1	0		Adds 1 * 2^{-24} to product.	Adds 1 * 2^{22} to product.
1	1		Adds 1 * 2^{-23} to product.	Adds 1 * 2^{23} to product.
TRIL, TRIM			Three-state controls on putputs. TRIL operates on LSP, TRIM on MSP.	
		0	Output enabled, output is low impedance.	
		1	Output disabled, output is high impedance.	

TYPICAL OPERATING SEQUENCE (TWO PORT) FOR REPEATED SETS OF MULTIPLICATIONS

1) Load 24 bit multiplier (N_0) and 24 bit multiplicand (M_0) into X and Y input registers. Simultaneously load output registers with the product of two previous operands, N_{-1} and M_{-1}. Three-state controls are in high state.
2) During the multiplication period of $N_0 * M_0$, the previous product $N_{-1} * M_{-1}$ is read to the I/O bus by placing the three-state controls in the low state. Following the product read period, the three-state controls are again returned to the high state and new operands N_1 and M_1 are sourced to the bus. The procedure is repeated by returning to item 1 above. In this way, a continual pipelined multiplication set is performed each τ_m period. Timing diagrams are shown below.

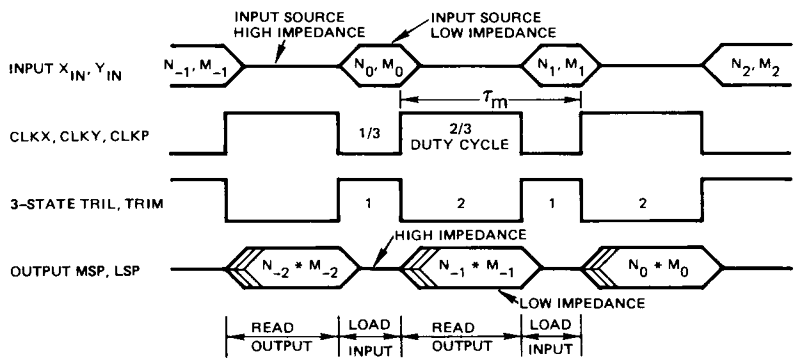


Figure 19. Multiplexed I/O Timing Diagram

DATA FORMAT EXAMPLES

FRACTIONAL TWO'S COMPLEMENT

X_{IN} TCX = 1

X_{23}	X_{22}	X_{21}	⟩⟩	X_2	X_1	X_0
X SGN	2^{-1}	2^{-2}		2^{-21}	2^{-22}	2^{-23}

TCY = 1 Y_{IN}

Y_{23}	Y_{22}	Y_{21}	⟩⟩	Y_2	Y_1	Y_0
Y SGN	2^{-1}	2^{-2}		2^{-21}	2^{-22}	2^{-23}

MSP_{OUT} / LSP_{OUT}

P_{47}	P_{46}	P_{45}	⟩⟩	P_{26}	P_{25}	P_{24}		P_{23}	P_{22}	P_{21}	⟩⟩	P_2	P_1	P_0
-2^1 P SGN	2^0	2^{-1}		2^{-20}	2^{-21}	2^{-22}	SH A = SH B = 0	2^{-23}	2^{-24}	2^{-25}		2^{-44}	2^{-45}	2^{-46}
2^0	2^{-1}	2^{-2}		2^{-21}	2^{-22}	2^{-23}	SH A = 1 SH B = 0	2^{-24}	2^{-25}	2^{-26}		2^{-45}	2^{-46}	0
2^{-1}	2^{-2}	2^{-3}		2^{-22}	2^{-23}	2^{-24}	SH A = X SH B = 1	2^{-25}	2^{-26}	2^{-27}		2^{-46}	0	0

Note: In all multiply cases except $-1.0_{(10)} \times -1.0_{(10)}$, the two MSB bits ($-2^1$ and 2^0) are the same. In that one multiply case, -2^1 will be a 0 and 2^0 will be a 1, all other bits will be 0. The OVF flag ($-2^1 \oplus 2^0$) will be a 1, and the NORM flag ($2^0 \oplus 2^{-1}$) will also be a 1. Since these flags are generated before the output shifter, the shift position will have no effect on the states of the flags. See figure 18.

Fractional 2's complement

$$X = -1 * SGN + \sum_{n=1}^{23} X_n 2^{-n} \qquad P = -1 * PSGN + \sum_{n=0}^{46} P_n 2^{-n}$$

Magnitude

$$X = \sum_{n=0}^{23} X_n 2^n \qquad P = \sum_{n=0}^{47} P_n 2^n$$

INTEGER MAGNITUDE

X_{IN} TCX = 0

X_{23}	X_{22}	X_{21}	⟩⟩	X_2	X_1	X_0
2^{23}	2^{22}	2^{21}		2^2	2^1	2^0

TCY = 0 Y_{IN}

Y_{23}	Y_{22}	Y_{21}	⟩⟩	Y_2	Y_1	Y_0
2^{23}	2^{22}	2^{21}		2^2	2^1	2^0

MSP_{OUT} / LSP_{OUT}

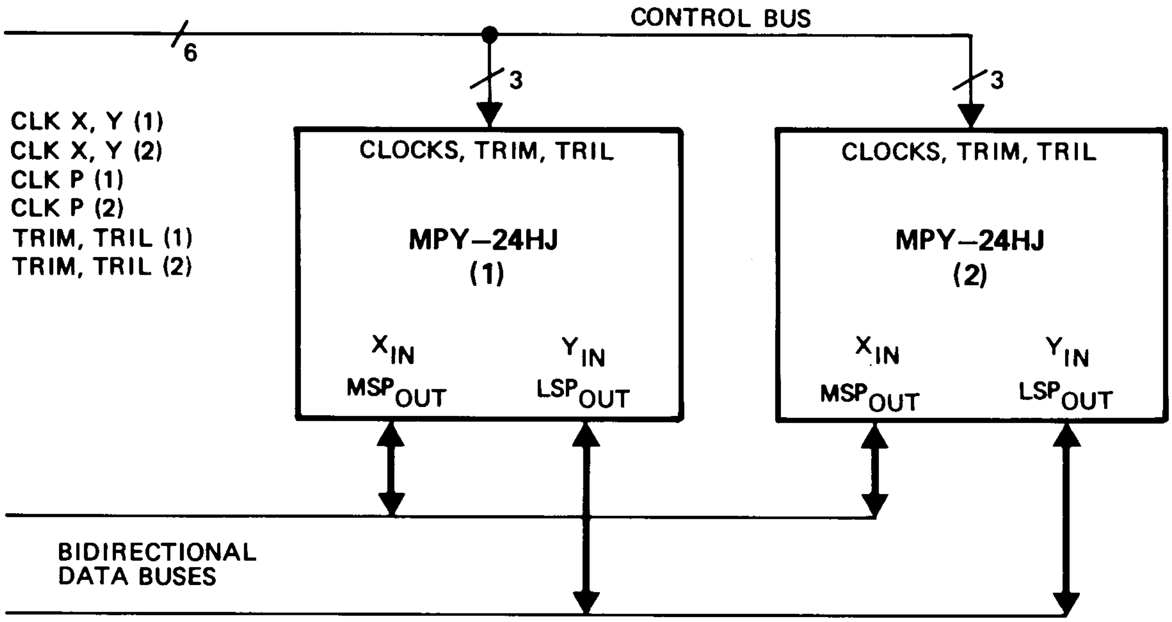
P_{47}	P_{46}	P_{45}	⟩⟩	P_{26}	P_{25}	P_{24}		P_{23}	P_{22}	P_{21}	⟩⟩	P_2	P_1	P_0
2^{47}	2^{46}	2^{45}		2^{26}	2^{25}	2^{24}	SH A = SH B = 0	2^{23}	2^{22}	2^{21}		2^2	2^1	2^0
2^{46}	2^{45}	2^{44}		2^{25}	2^{24}	2^{23}	SH A = 1 SH B = 0	2^{22}	2^{21}	2^{20}		2^1	2^0	0
2^{45}	2^{44}	2^{43}		2^{24}	2^{23}	2^{22}	SH A = X SH B = 1	2^{21}	2^{20}	2^{19}		2^0	0	0

When mixed mode signals are used, the flag signals, FLAG OVFLO and FLAG NORM will not have the same general utility as described under FLAG outputs.

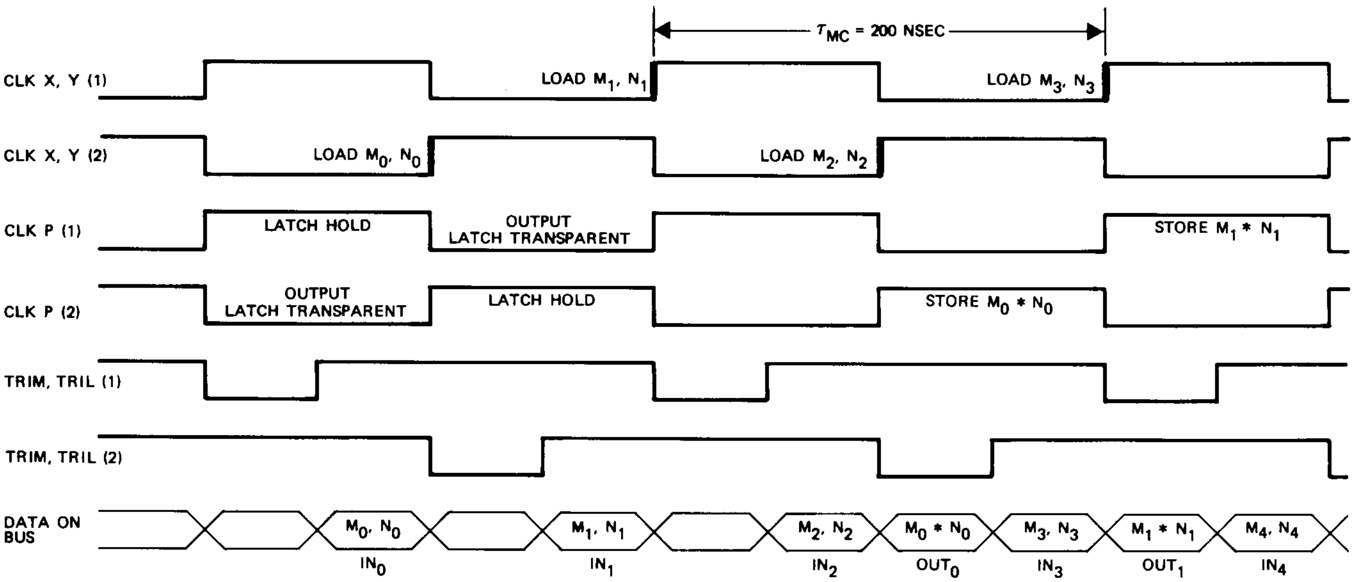
APPLICATION NOTES

100 NSEC 24 X 24 BIT MULTIPLIER

The multipliers can be interfaced easily on a data bus (or buses) to achieve greater multiply throughput rates. The MPY-24HJ was picked for the example below because it has the highest number of multiplexed I/O ports. The MPY-12HJ and MPY-16HJ (single precision mode), with their individual inputs and outputs, are easier to interface because the buses do not have to be multiplexed for a given throughput rate. The timing for the clocks and three-state controls of this circuit are given below.



Block Diagram



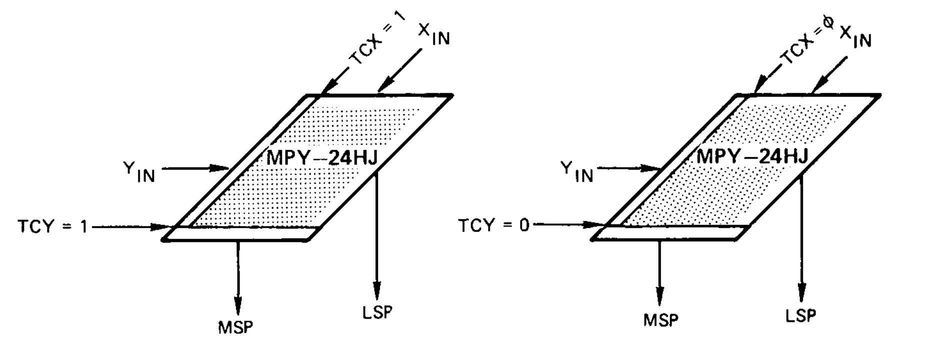
Timing Diagram

APPLICATION NOTES

48 X 48 TWO'S COMPLEMENT MULTIPLIER

The expanded two's complement diagram shows the connections to external adders required to complete the partial product summation. The diagram simplified for illustrative purposes is accurate, but for speed optimization additional registers can be used to pipeline the additions. Each adder shown is a 24 bit wide two input adder or equivalent. Carry-in and carry-out are also required.

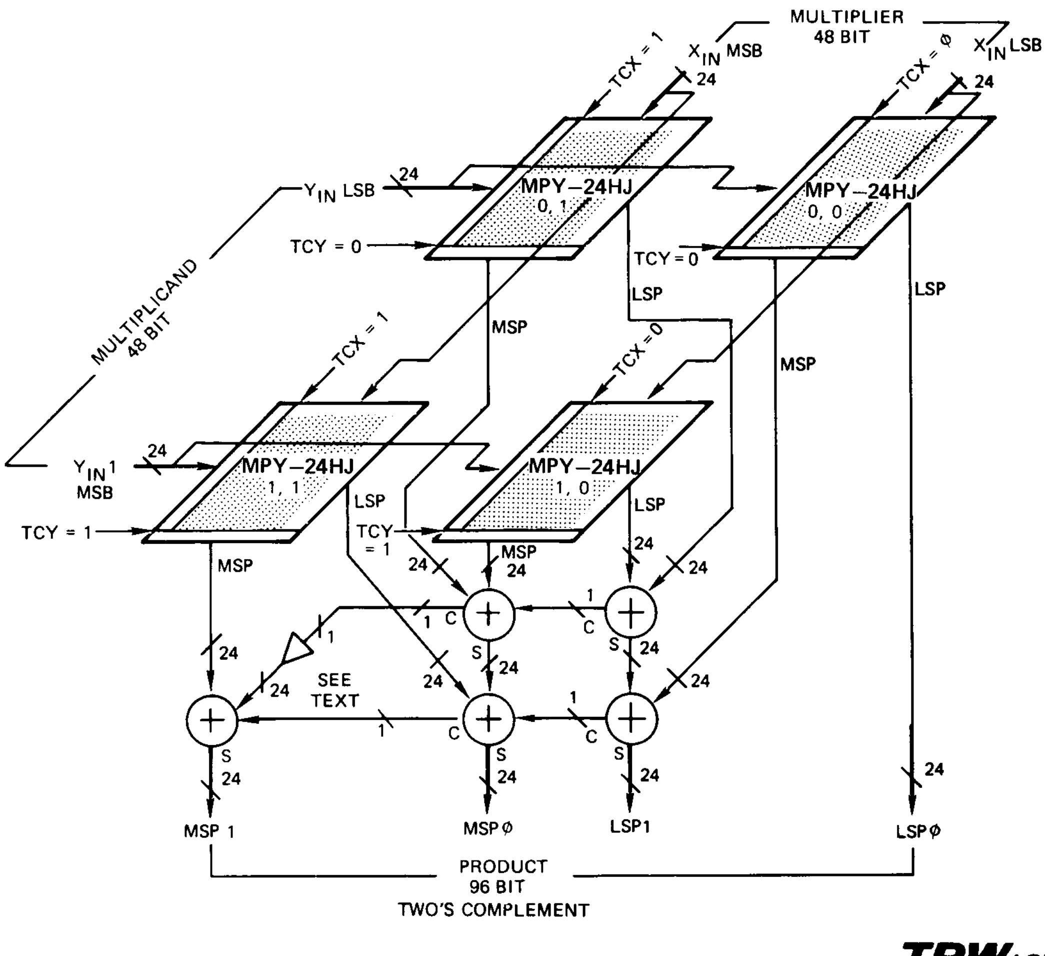
The expanded magnitude case is similar except all TC controls are set low, logic 0, and the upper carry into the last most significant adder connects only to the least significant bit of the adder. The remaining 23 inputs to the adder are then terminated to logic zero, ground.



TWO'S COMPLEMENT CASE

MAGNITUDE CASE

TWO'S COMPLEMENT
MULTIPLIER, MULTIPLICAND



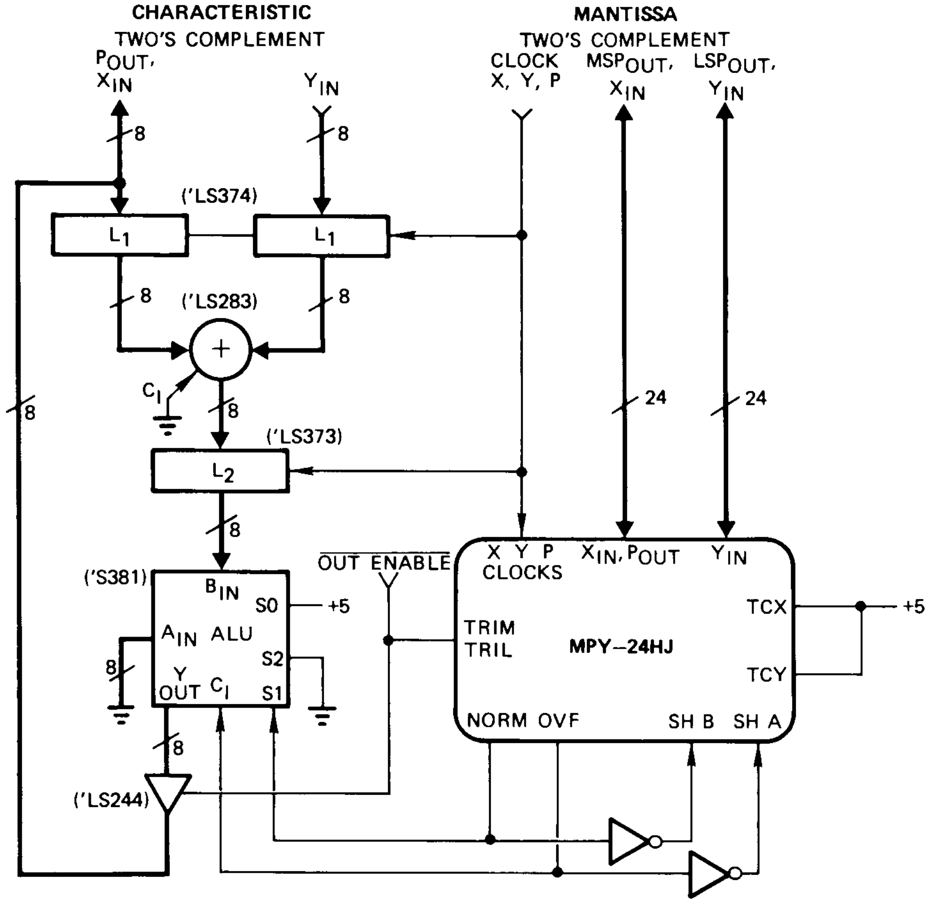
APPLICATION NOTES

32 BIT FLOATING POINT MULTIPLICATION—TWO'S COMPLEMENT

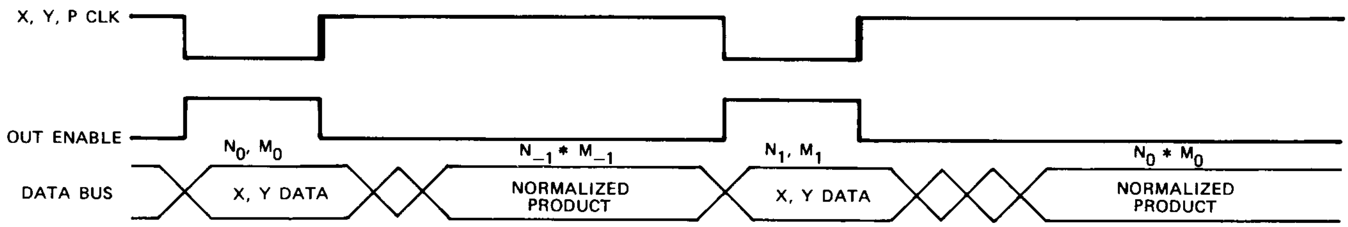
The MPY-24HJ, with its shifter, is ideally suited for floating point multiplication applications. The most complex part of the function, the mantissa multiply plus normalize, can now be done with 1 chip. The cost, power, and size of the floating point multiply function can be greatly reduced. The latches and adders shown are chosen to closely match the setup, hold, and output delay times of the MPY-24HJ. Split timing is used to read the products and load new operands via common buses.

The multiply time is divided into two phases defined by the clock. At the rising edge of the X, Y, P clock, a new multiplier and multiplicand are stored in the input latches of the MPY-24HJ and L_1 latches. While the internal multiplier array of the MPY-24HJ is generating a product, the two characteristics are added. When the clock goes low and then high again, the product is stored in the output latch of the MPY-24HJ, and L_2 (new operands could also be read in again). The flag outputs of the multiplier chip are then used to normalize the characteristics and mantissa of the product. Although not shown here, many floating point users test for an overflow of the characteristic after final normalization, setting a flag or hard limiting if it does.

When the output shifter and ALU have settled, the normalized product is put onto the bus and read back.



Two's Complement Block Diagram

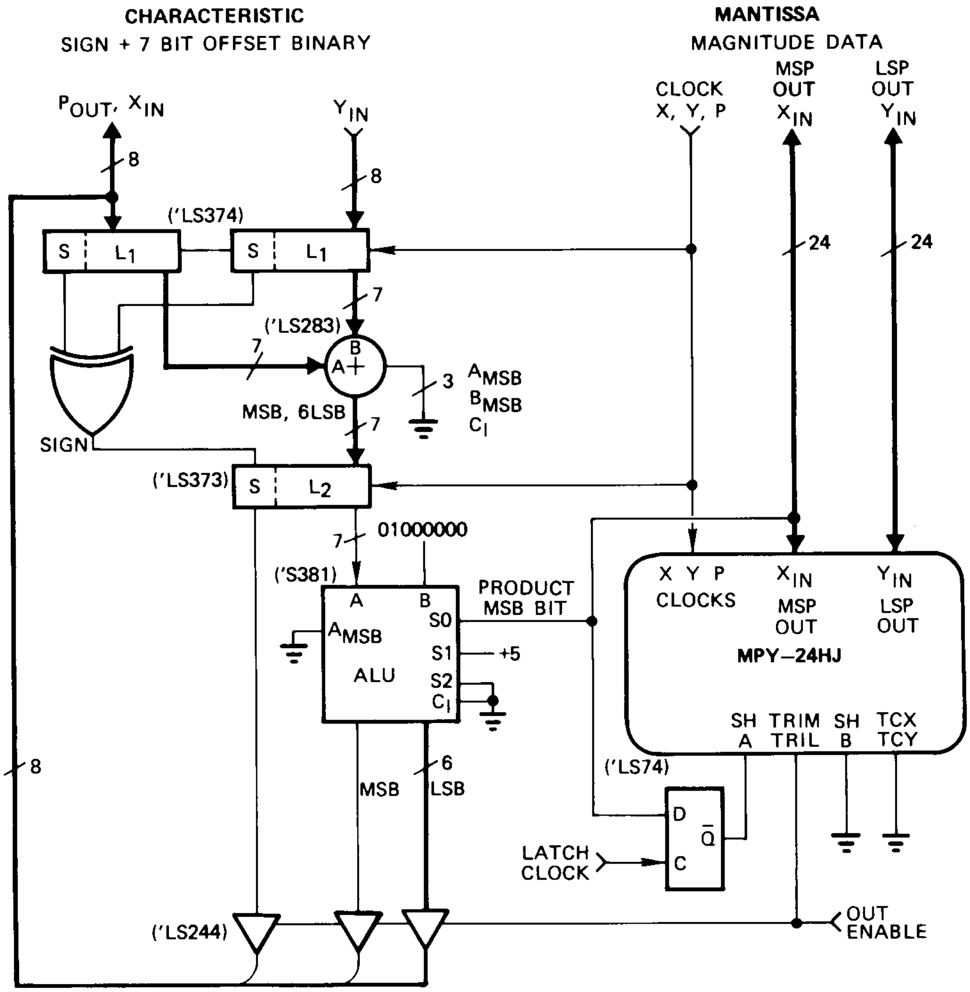


Two's Complement I/O Timing Diagram

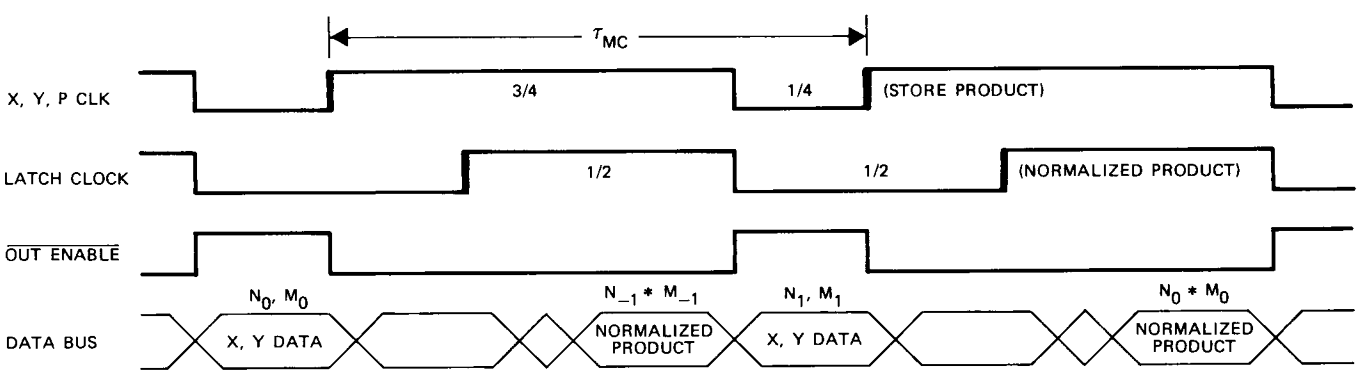
APPLICATION NOTES

32 BIT FLOATING POINT MULTIPLICATION–MAGNITUDE

The basic multiply time is partitioned into three phases defined by the clocks. At the rising edge of the X, Y, P clock, new X and Y operands are loaded into the input latches. Simultaneously, the previous product is stored in the output registers of the MPY-24HJ and 'LS373. The MSB of the mantissa is read into the ALU to adjust the exponent, and also into the 'LS74 latch where it is stored on the rising edge of the latch clock. Shortly after that edge, the MPY-24HJ output will be normalized and may be read, along with the output of the ALU. When the output enable goes high, the output buffers are turned off. New X and Y operands can now be brought in prior to the next X, Y, P clock.



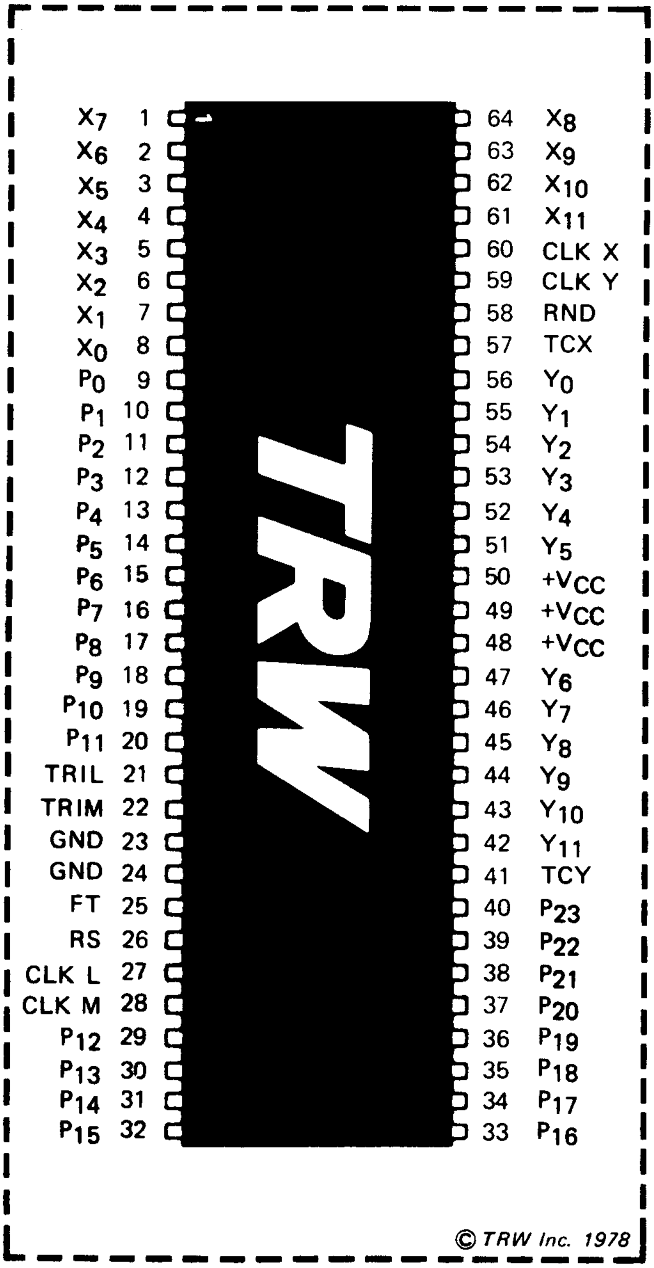
32 Bit Floating Point Multiplier Block Diagram



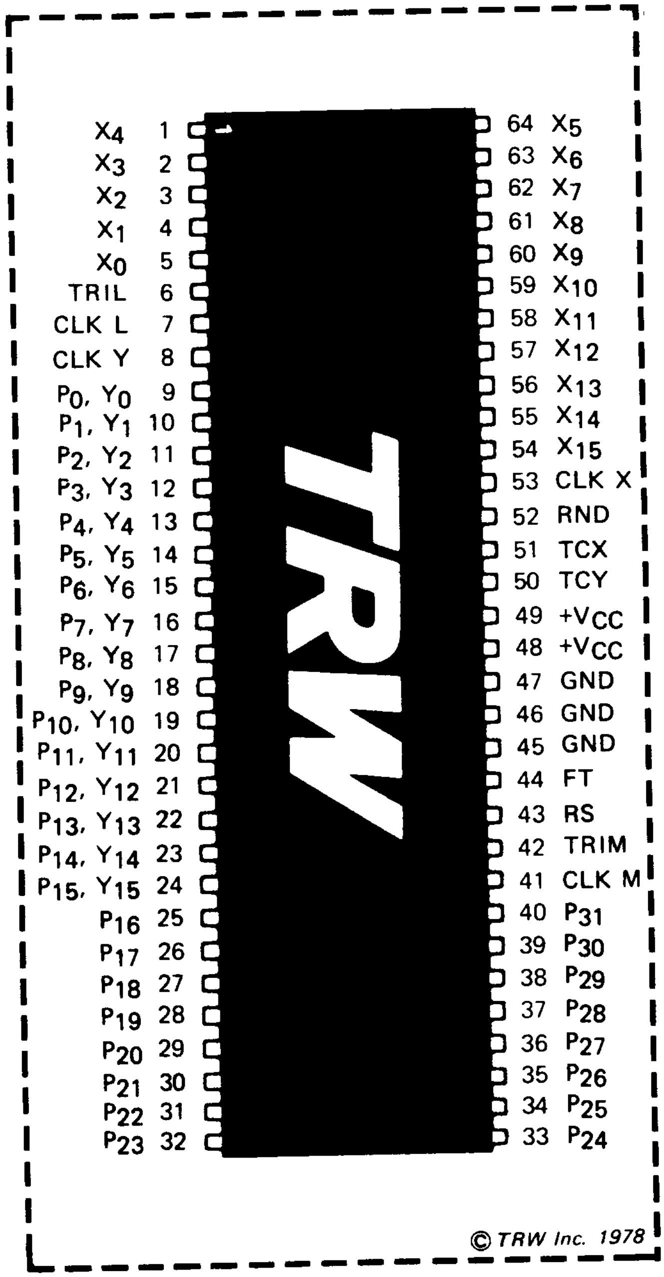
Magnitude I/O Timing Diagram

PACKAGE INFORMATION

MPY-12HJ



MPY-16HJ

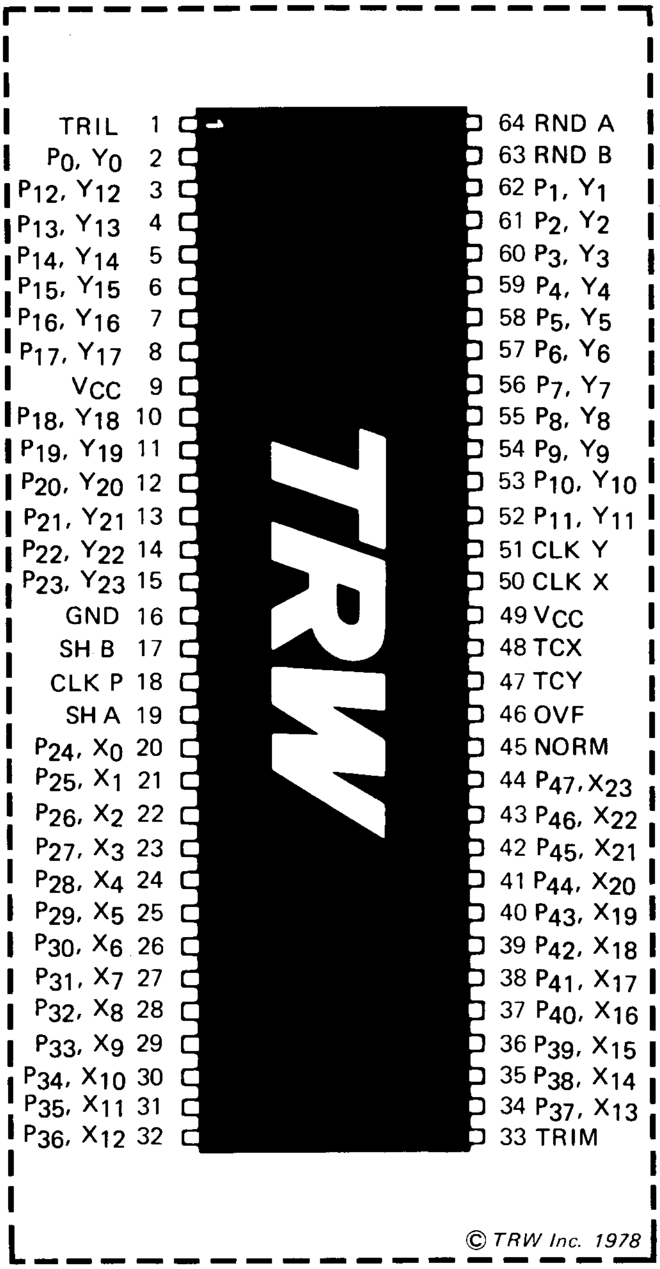


FRACTIONAL/INTEGER MULTIPLICATION

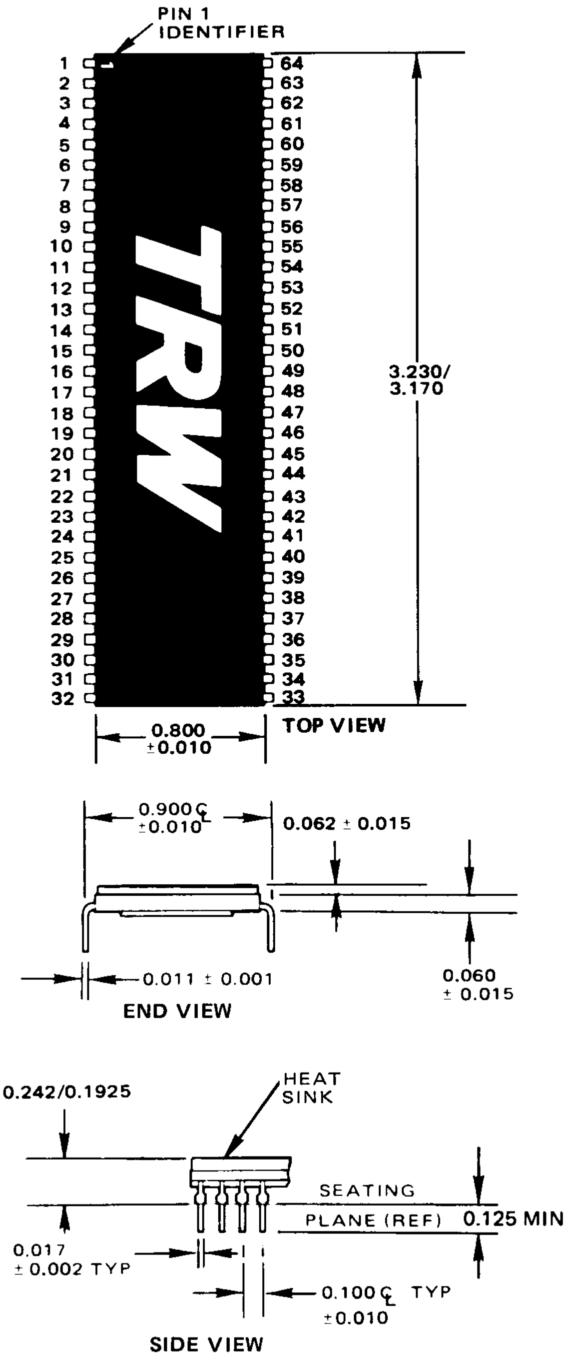
The MPY-series multipliers may be used in either a fractional or integer mode – the difference is conceptual. For example, using a 4-bit case, the multiplier does not know (or care) whether it is performing the multiplication $6 \times (-2) = -12$ or $(6/8) \times (-2/8) = -12/64$; the input and output binary fields will be the same. Fractional multiplication (using fields as defined in the previous specifications) offers the advantage of more convenient single precision usage. The MSB is closest to the binary point in fractional representation (the LSB for integer representation). The fractional notation is frequently the most convenient when implementing a floating point multiplication system.

PACKAGE INFORMATION

MPY-24HJ



64-PIN DIP



THERMAL RESISTANCE DATA

Junction to case	$\theta_{JC} \approx 4^{o}C/W$
Case to ambient	θ_{CA} (Still air) $\approx 10^{o}C/W$
Case to ambient	θ_{CA} (300 cfm airflow) $\approx 4^{o}C/W$

NOTES

- DIMENSIONS IN INCHES
- ALL POWER AND GROUND PINS MUST BE CONNECTED

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