SIEMENS

Video-Pulse Generator

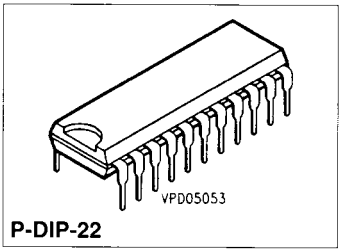
TBB 278 B

Preliminary Data

CMOS

Features

- Free-running or external synchronization
- External synchronization optionally with S signal and PLL or with basic timing signal t_0 and frame reset signal
- Parallel or serial programming
- Line interlacing can be disabled
- Parallel programming:
  - 16 systems with firmly assigned line numbers and pulse widths (CCIR 624-3, EIA RS 343 A, CCIR AZ 11, HDTV and others)
- Serial programming:
  - Line number per field selectable between 1 and 4095
  - Pulse widths selectable in steps
  - Identification signals for PAL, PAL-M, SECAM and NTSC color systems
  - Equalizing signals and V_{sync}-interruptors can be disabled
  - TLL-compatible serial interface
  - Power-on reset on PAL system



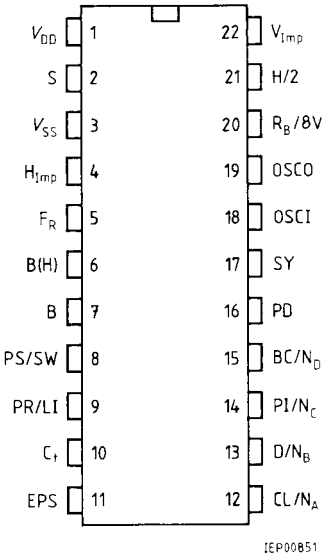
P-DIP-22

Type	Ordering Code	Package
S▼ TBB 278 B	Q67100-H8759	P-DIP-22

▼ New type

The TBB 278 B video-pulse generator is an LSI circuit generating the sync, control and color-subcarrier-window signals that are necessary for controlling cameras, monitors, mixing consoles and similar items of equipment. Up to 4095 lines and the pulse widths of output signals can be serially programmed. Alternatively to serial programming, 16 standards or systems based on standards can be selected on a parallel interface or by switches or hardwiring.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{DD}	Supply voltage
3	V_{SS}	Ground
19	OSCO	Crystal connection/ext. clock
18	OSCI	Crystal connection
16	PD	PLL output
12	CL/N_A	Clock/parallel programm. input
13	D/N_B	Data/parallel programm. input
11	EPS	Parallel/serial programming switchover, transfer to serial latch
17	SY	Ext. sync signal input
4	H_{Imp}	Horizontal pulse (line freq.)
21	H/2	Double line frequency
6	B(H)	Horizontal blanking pulse
10	C_t	Clamping pulse
7	B	Blanking signal
20	R_B/8 V	Vidicon blanking signal output/ output for color-subcarrier-phase identification signal
2	S	Sync signal
5	F_R	Frame reset signal
22	V_{Imp}	Vertical pulse
14	PI/N_C	Output for PAL identification pulse or SECAM identification/ parallel programming input
15	BC/N_D	Burst window output (PAL, PAL-M, NTSC), color-subcarrier blanking-window output (SECAM)/ parallel programming input
8	PS/SW	PAL squarewave output/input for external sync selection
9	PR/LI	Reset input for PAL square on 1st field, set input for S9, S10 on 4th field/ disactivate line interlacing

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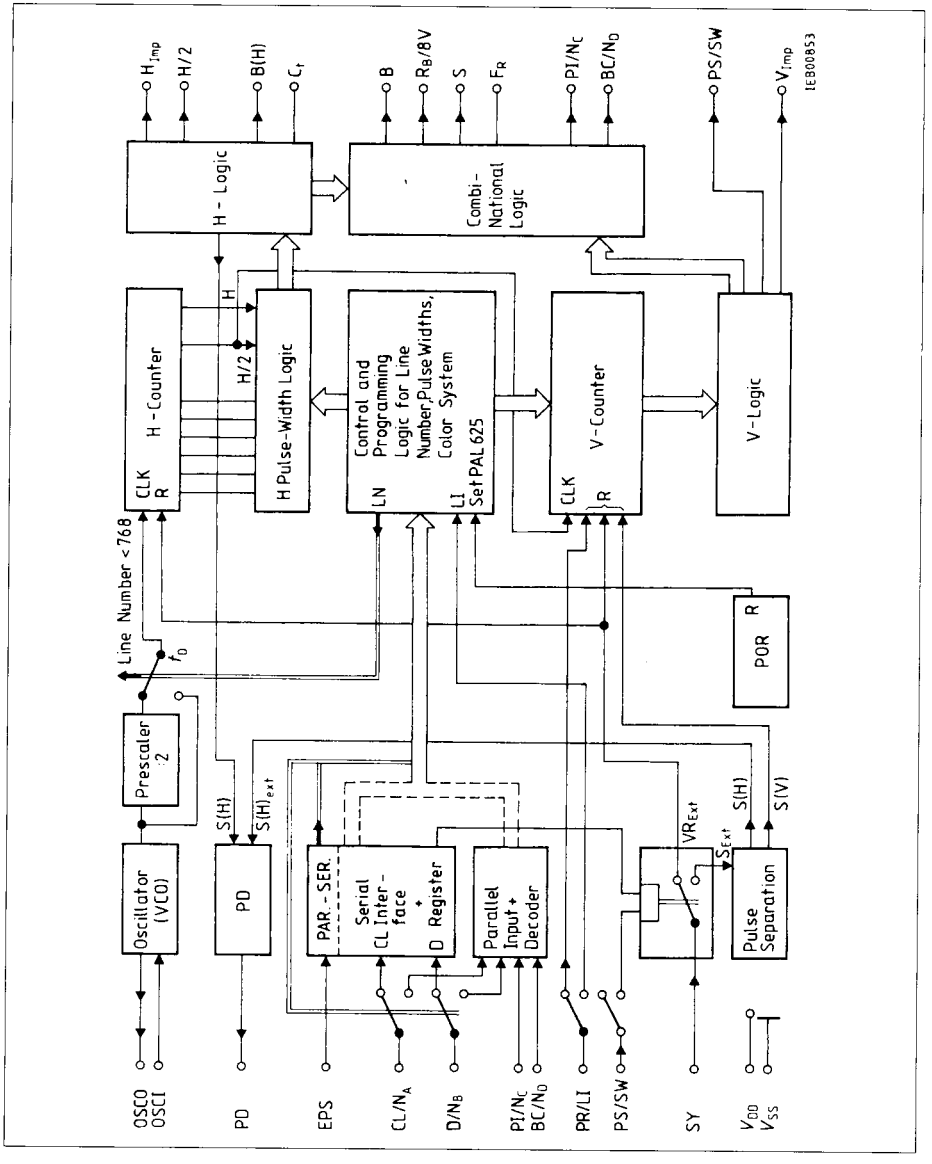

Block Diagram

Functional Description

The block diagram illustrates the basic design of the circuit.

The TBB 278 B is parallelly or serially programmed according to the level on pin EPS. Pins with names separated by a slash have a different function for parallel and serial programming.

Parallel Programming (EPS = High)

16 systems can be selected with firmly assigned numbers of lines and pulse widths (**see tables 1 and 2**).

Pins CL/N_A, D/N_B, PI/N_C, BC/N_D, PS/SW and PR/LI are activated as parallel programming inputs. In addition to the PS/SW selection of the sync mode, the line interlacing PR/LI can also be freely selected for all 16 programs (**see table 1**). In systems S9 and S10 four fields have the standard line numbers 1023 and 1249, respectively. (Because of the odd number of lines the fourth field has a different number of lines to the preceeding three fields.)

Apart from the input signal PS/SW, which is effective immediately, parallel systems newly programmed with PR/LI, CL/N_A, etc are not adopted until the following (internal) F_R pulse occurs, i.e. the TBB 278 B does not start to operate according to the new system until the beginning of the next frame.

The sync input signals SY and PR/LI (PR only for S9, S10) are effective immediately (**see figure 1**).

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Serial Programming (EPS = Low)

It is possible to design systems with any line numbers and pulse widths (**see table 3**). Pins CL/N_A and D/N_B are activated as serial programming inputs, PI/N_C, BC/N_D, PS/SW and R_B/8V as color-identification signal outputs and PR/LI as a PAL square reset input.

The power-on reset automatically programs the serial register to the PAL-system with 625 lines/frame. Another system can be written in with shift clock CL/N_A and data D/N_B, and transfer by the following (internal) F_R pulse can be activated with a short high-pulse on pin EPS. (A high pulse that is substantially longer than 5 µs will switch the TBB 278 B to "parallel", but the information in the shift register will not be lost.) As in the parallel mode, the TBB 278 B does not start to operate according to the new system until the beginning of the next frame.

Only the sync selection bit # 1 is effective immediately with the EPS high edge, and likewise of course the sync input signals SY and PR/LI (**see figure 3**).

Serial Coding Comprises a Total of 71 Bits:

12 bits	2^0 thru 2^{11}	for line number per field, 1-4095
3 bits		for selecting color system
47 bits		for flexible setting of pulse widths and delays of horizontal and vertical output signals as multiples of oscillator basic timing t_o or of line period H.
6 bits		number of equalizing pulses and V_{sync}-interrupt pulses
1 bit		with or without equalizing pulses and V_{sync}-interrupt pulses
1 bit		with or without line interlacing
1 bit		for selecting synchronization mode N_B : for external timing = master timing, intern. osc. is disabled.

Functional Description

Systems Selectable on Parallel Interface

System	Lines/Frame	Field/Frame Freq.	Standard
S1	625	50/25	CCIR report 624-3
S2	525	60/30	CCIR report 624-3
S3	735	60/30	Based on EIA RS 343 A
S4	875	50/25	Based on CCIR
S5	1125	60/30	HDTV Japan
S6	1023	60/30	EIA RS 343 A
S7	1249	50/25	Based on EIA RS 343 A
S8	1249	80/40	Flickerfree monitors
S9	3 × 256 1 × 255	120	Progressive scanning
S10	3 × 312 1 × 313	100	Progressive scanning
S11	1023	30	Progressive scanning
S12	1249	25	Progressive scanning
S13	2046	3	High-definition progressive scanning
S14	2498	2.5	High-definition progressive scanning
S15	1251	50/25	Based on EIA RS 343 A
S16	1125	60/30	CCIR report AZ 11

Absolute Maximum Ratings

T_A = – 25 to 75 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input voltage	V_I	– 0.3	V_{DD} + 0.3	V
Supply voltage	V_{DD}	– 0.3	6	V
Storage temperature	T_{stg}	– 50	125	°C
Total power dissipation	P_{tot}		500	mW
Power dissipation per output	P_Q		50	mW

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (without output load)	I_{DD}			5	mA
Operating frequency	f_{OSC}			15	MHz
Ambient temperature	T_A	– 25		75	°C

DC Characteristics
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Inputs						
PI/N_C, BC/N_D SY, PS/SW, OSCI, OSCO						(OSCO for ext. clock)
H-input voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
L-input voltage	V_{IL}	0		0.3 V_{DD}	V	
Input capacitance	C_I			10	pF	
Input current	I_I			1	µA	
Inputs (TTL-compatible)						
EPS, CL/N_A, D/N_B						
H-input signal	V_{IH}	2		V_{DD}	V	
L-input signal	V_{IL}	V_{SS}		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_I			1	µA	
Outputs						
H/2, B(H), C_t, B PI/N_C, BC/N_D, PS/SW, R_B/8V						
H-output voltage	V_{QH}	4.5		V_{DD}	V	I_{QH} = 2.5 mA
L-output voltage	V_{QL}	0		0.5	V	I_{QL} = 2.5 mA
PD						
H-output voltage	V_{QH}	4		V_{DD}	V	I_{QH} = 100 µA
L-output voltage	V_{QL}	0		1	V	I_{QL} = 100 µA
OSCO						
H-output voltage	V_{QH}	4		V_{DD}	V	I_{QH} = 200 µA
L-output voltage	V_{QL}	0		1	V	I_{QL} = 200 µA
H_{Imp}, S, F_R; V_{Imp}						
H-output voltage	V_{QH}	4.5		V_{DD}	V	I_{QH} = 5 mA
L-output voltage	V_{QL}	0		0.5	V	I_{QL} = 5 mA

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AC Characteristics

T_A = 25 °C

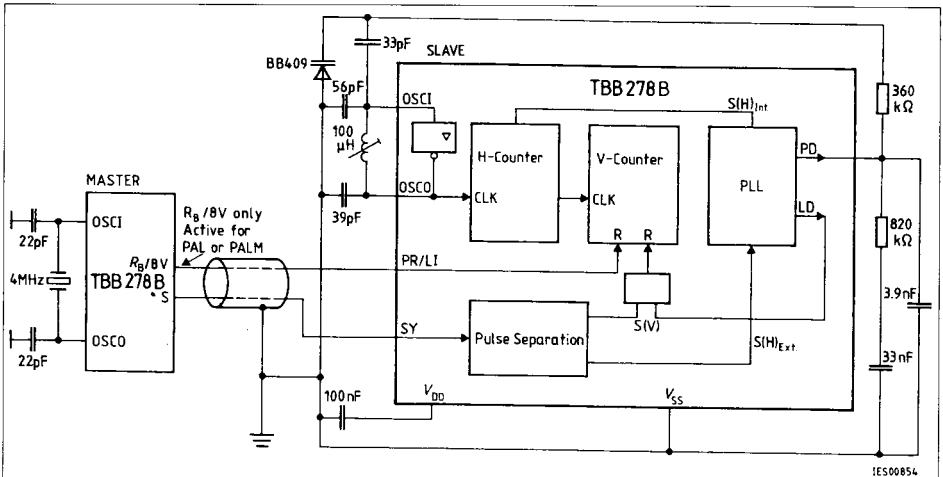
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Inputs						
CL/N_A						
Clock period	t_{CL}	1			µs	
D/N_B						
Data setup	t_{SD}	50			ns	
Data hold	t_{HD}	50			ns	
EPS						
Transfer pulse, duration	t_L			2	µs	
Propagation time	t_P			50	ns	OSCO clock edge to signal o/p
PR/LI						
PAL square reset, duration	t_{PR}	100			ns	
Outputs						
H_{Imp}, S, F_R						
Rise time	t_{LH}			15	ns	C_L = 20 pF
Fall time	t_{HL}			5	ns	C_L = 20 pF
H/2, B(H), C_t, B, V_{Imp}						
PI/N_C, BC/N_D, PS/SW, R_B/8V						
Rise time	t_{LH}			50	ns	C_L = 20 pF
Fall time	t_{HL}			20	ns	C_L = 20 pF

Synchronization

(applies to parallel and serial programming)

Synchronization of Slave with Combined S Signal

A PLL compares the phase of the internal and external S (H) pulses and adjusts the oscillator frequency accordingly. The S (V) signal resets the V counter to the beginning of the field if the phase difference between the external and internal S (H) pulse is smaller than ± 8 t_0 (see Lock Detect LD). Master and slave must be programmed for the same system (same number of lines and equalizing signals). V_{Imp}, S(V), B(V) and F_R will appear on the slaves' outputs if the line number of the master is smaller than that of the slave. The V_{Imp}, S(V), B(V) signals will be shortened by one half line.



Example: master with 4-MHz crystal oscillator for PAL 625. slave with LC oscillator and PD filter.

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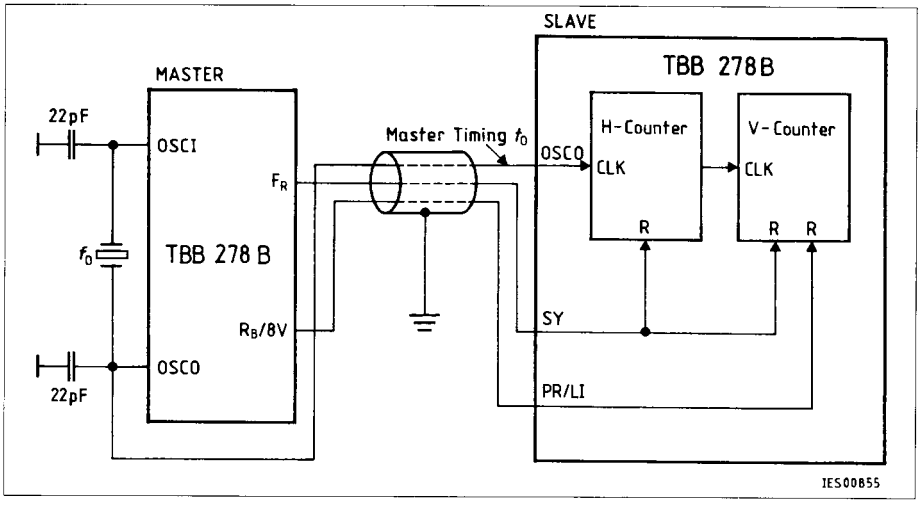
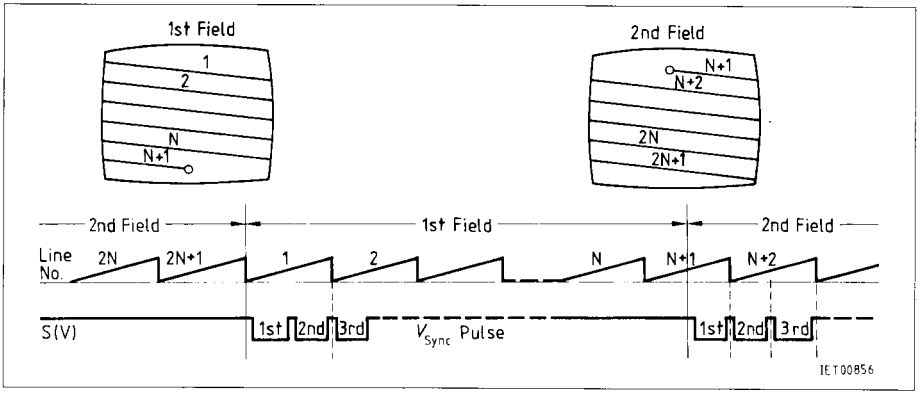
Synchronization with Master Timing and F_R Reset

Same timing: master and slave are synchronous. After any disturbance the next falling edge of F_R resets the V counter to the beginning of the frame and the H counter to the beginning of the line. The supply to the oscillator inverter is disabled and thus OSCI too.



This kind of synchronization is advisable for high-definition systems because less jitter is produced than with the PLL.

Line Interlacing
(applies to even and odd numbers of equalizing pulses)



Systems with Line Interlacing

The 1st field begins with a whole line and ends after a half.

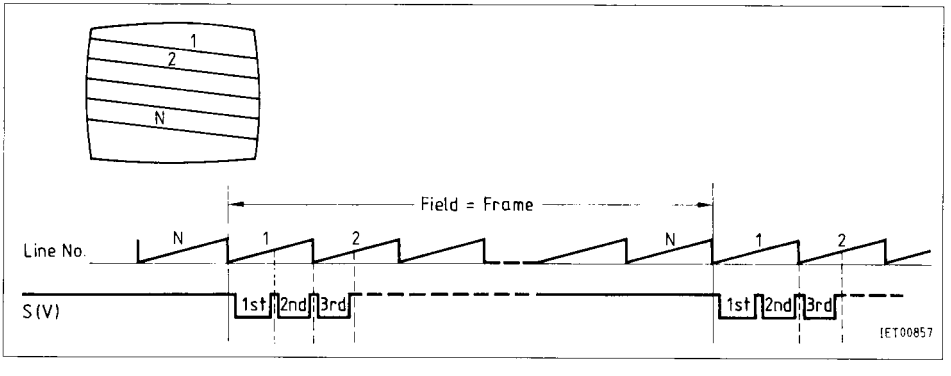
The 2nd fields begins with a half line and ends with a whole one, so it is automatically written into the spaces between the lines of the 1st field.

Both fields are initiated by the 1st V_{sync} pulse, each have (N + 1/2) lines and produce a frame of (2N + 1) lines.

(NB: Because of the finite picture flyback time the first lines of a field are not as visible as illustrated above).

Systems without Line Interlacing

The same field is written each time, into the same raster as the previous one. The field begins and ends with a whole line.



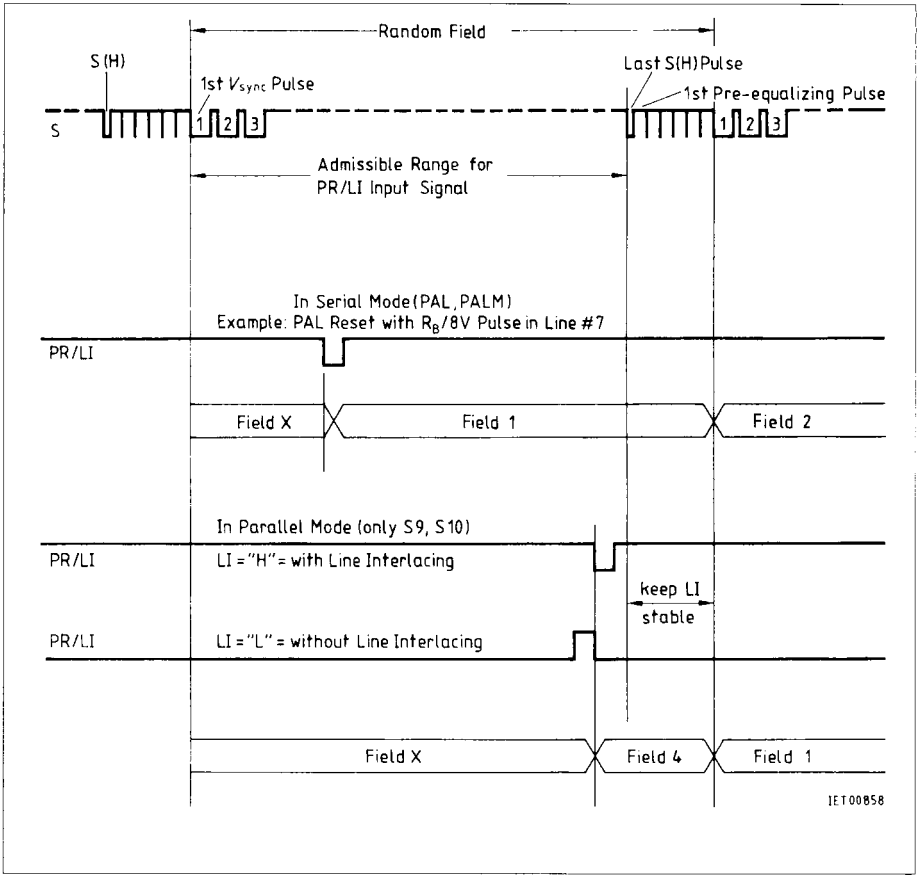


Figure 1
Timing Diagram for PR/LI Signal

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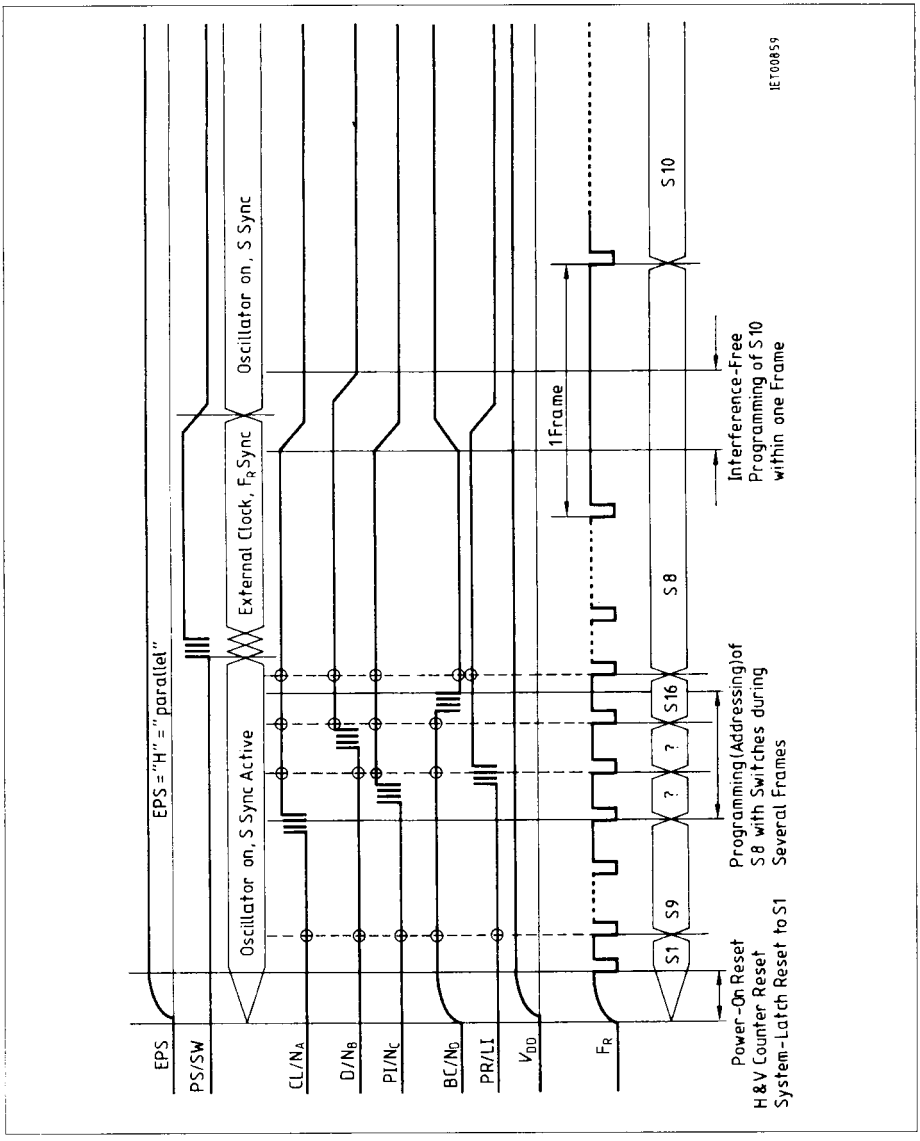

Figure 2
Pulse Diagram for Parallel Programming

Table 1
Parallel Programming

System	Lines per frame	Lines per field	Picture Frequency/Hz frame	Picture Frequency/Hz field	No. of Equ. & Int.	$f_{osc.}$ /MHz	f_o / f_Hs	remarks	Coding EPS	Coding LI	Coding PR/ N_D	Coding BC/ N_D	Coding PI/ N_C	Coding D/ N_B	Coding CL/ N_A	PS/ SW
S1	625	312 ½	25	50	5	4.000	0.5		H	H	L	L	L	L	L	
S2	525	262 ½	30	60	6	4.032	0.49603	**For LI = "L":** Number of lines/field is reduced by ½ to eliminate line interlacing.	H	H	L	L	L	L	H	**"H"** external clock with f_H-synchronization
S3	735	367 ½	30	60	6	5.6448	0.3543		H	H	L	L	L	H	L	
S4	875	437 ½	25	50	5	5.600	0.3571		H	H	L	L	L	H	H	
S5	1125	562 ½	30	60	10	8.640	0.23148		H	H	L	L	H	L	L	
S6	1023	511 ½	30	60	6	3.92832	0.2546	Frame frequency is doubled	H	H	L	L	H	L	H	
S7	1249	624 ½	25	50	6	3.9968	0.2502		H	H	L	L	H	H	L	
S8	1249	624 ½	40	80	none	12.7898	0.1564		H	H	L	L	H	H	H	
S9	3 × 256, 1 × 255			120	6	3.92832	0.2556	**for LI = "H":** Number of lines/field is reduced by ½ **for LI = "H":** Number of lines/field is increased by ½ to produce line interlacing **For LI = "L":** like in S1 thru S8	H	L*)	H	L	L	L	L	**or "L"** Oscillator mode with S-synchronization
S10	3 × 312, 1 × 313			100	6	3.9968	0.2502		H	L*)	H	L	L	H	H	
S11	1023			30	12	3.9283	0.2546		H	L	H	L	L	H	L	
S12	1249			25	12	3.9968	0.2502		H	L	H	L	L	H	H	
S13	2046		3		24	0.785664	1.2728		H	L	H	H	L	L	L	
S14	2498		2.5		24	0.79936	1.251		H	L	H	H	L	L	H	
S15	1251	625 ½	25	50	6	3.9968	0.2502		H	H	H	H	H	H	L	
S16	1125	562 ½	30	60	10	8.64	0.23148		H	H	H	H	H	H	H	

*) PR/LI: falling edge sets TBB 278 B to 1rst field

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Table 2
Pulse Widths for Systems Selectable in Parallel Mode

Parallel system / Output signals		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
Lines/frame		625	525	735	875	1125	1023	1249	1249	3...256 1...255	3...312 1...313	1023	1249	2046	2498	1251	1125
Frame frequency	/Hz	25	30	30	25	30	30	25	40	120	100	30	25	3	2.5	25	30
field frequency	/Hz	50	60	60	50	60	60	50	80	–	–	–	–	–	–	50	60
H line period	/µs	64	63.492	45.35	45.71	–	32.58	32.02	–	32.58	32.02	32.583	32.025	162.92	160.12	32.026	29.629
Line frequency	/KHz	15.625	15.750	22.05	21.877	33.75	30.69	37.224	49.95	30.69	31.22	30.69	31.226	6.138	6.245	31.224	33.75
t_o = H/128 = 1/f_o	/µs	.500	.49603	.3543	.3571	.23148	.2546	.2502	.1564	.2556	.2502	.2546	.2502	1.2728	1.251	.2502	.23148
f_{OSC}	/MHz	4.000	4.032	5.6448	5.600	8.64	3.92832	3.9968	12.7898	3.92832	3.9968	3.9283	3.9968	0.785664	0.79936	3.9968	8.64
t_{OSC} = 1/f_{OSC}[1]		0.5 to	0.5 to	0.5 to	0.5 to	0.5 to	to	to	0.5 to	to	to	to	to	to	to	to	0.5 to
Blanking signal	B(H)	24 to	22 to	20 to	24 to	26 to	28 to	24 to	34 to	28 to	24 to	28 to	24 to	28 to	24 to	24 to	16 to
	B(V)	25 H	20 H	30 H	30 H	42 H			40 H	20 H		80 H		160 H		39 H	45 H
Vidicon blanking signal	RB(H)	19 to	19 to	19 to	19 to	–	19 to		–	–		–		–		19 to	–
	RB(V)	15 H	15 H	20 H	20 H	–	30 H		–	–		–		–		30 H	–
Front porch	D	3 to	3 to	3 to	3 to	3 to	3 to		3 to	3 to		3 to		3 to		3 to	3 to
H-pulse		14 to	13 to	14 to	14 to	10 to	10 to		10 to	10 to		10 to		10 to		10 to	10 to
V-pulse		10 H	9.5 H	14.5 H	15 H	5 H	20 H		20 H	10 H		40 H		80 H		20 H	20 H
Clamping pulse	C_1	2 to	3 to	2 to	2 to	3 to	3 to		–	3 to		3 to		3 to		3 to	2 to
C_1 delay	DC_1	17 to	16 to	17 to	17 to	13 to	20 to		–	20 to		20 to		20 to		20 to	13 to
S signal	S(H)	9.5 to	9.5 to	7 to	7 to	10 to	11 to		10 to	10 to		10 to		10 to		11 to	2.5 to
Equalizing pulse	Equ.	4.5 to	4.5 to	4 to	4 to	5 to	5 to		–	4 to		4 to		4 to		5 to	2.5 to
V_{sync} interrupt	Int.	9.5 to	9.5 to	7 to	7 to	9 to	8 to		10 to[2]	7 to		7 to		7 to		8 to	3.5 to
No. of Equ. & Int.		5	6	6	5	10	6		–	6		12		24		6	10
or DV_{imp}		2.5 H	3 H	3 H	2.5 H	5 H	3 H		5 H	3 H		6 H		12 H		3 H	5 H

$f_o = 1/t_o = 128 \times$ line number (frame) $\times$ frame frequency

1) t_{OSC} = oscillator or external clock period. Prescaler is bypassed for $t_{OSC} = t_o$ (Systems S6, S7, S9 thru S14)

2) No Equ. & Int. in middle of line. Int. corresponds to S(H) shifted. **See figures 4 and 5.**

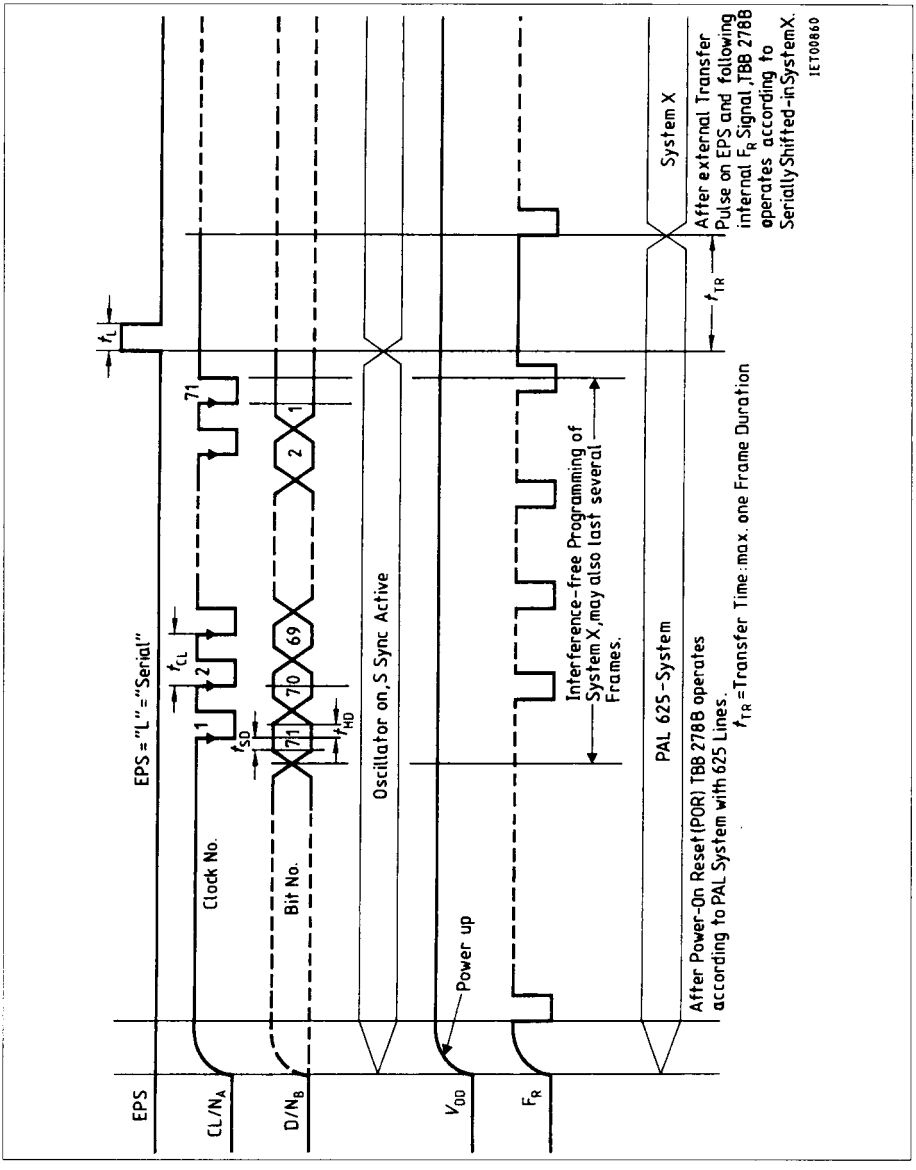


Figure 3
Pulse Diagram for Serial Programming

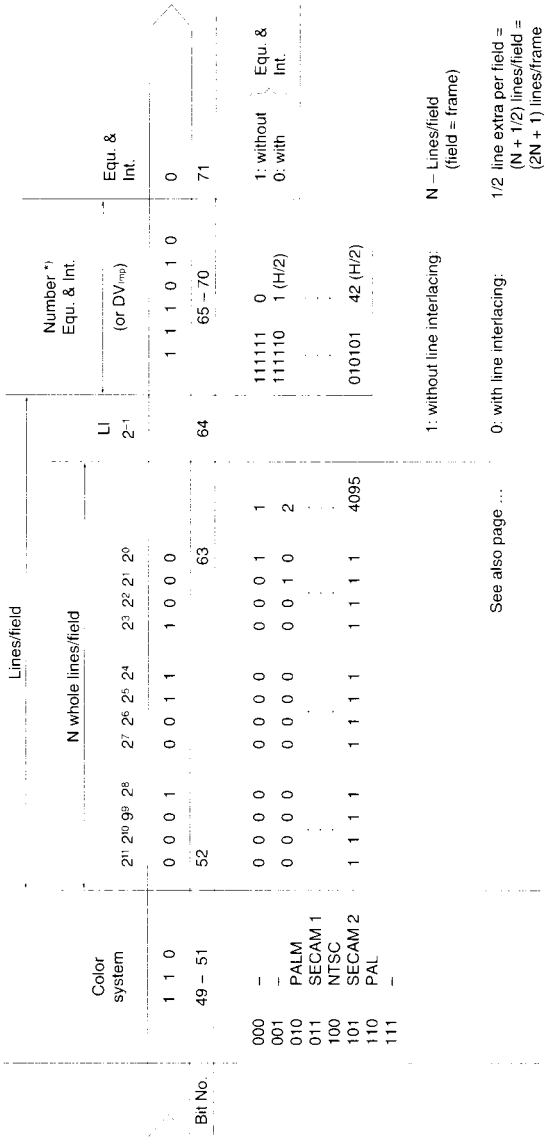
Table 3
Coding for Serial Programming
As an example the PAL system with 625 lines is entered in the register, which is written in automatically at power-on reset.

Sync select	B (H)	S (H)	H_{max}	C_1	DC	Equ.	Int.	B (V)	V_{max}
Sy									
1	1 0 0 1 1 1	0 1 1 1 0	0 1 0 1	1 0 1	0 1 1 1 0	1 0 0 0	1 1 0 0	0 0 0 1 1 0 0 1	1 1 1 0 1 0 1 1
Bit No.1	2 – 7	8 – 12	13 – 16	17 – 19	20 – 24	25 – 28	29 – 32	33 – 40	41 – 48
					11110	1 f_O			
					11101	2 f_O			
	11111	1.0 f_O	110	1 f_O			1111	11.0 f_O	1111 1110 0.5_H
	11110	1.5 f_O*)	101	2 f_O			1110	10.5 f_O*)	1111 1101 1.0_H
	11101	2.0 f_O					1101	10.0 f_O	
					00000	31 f_O			
	00001	16.0 f_O					0001	4.0 f_O	
	00000	16.5 f_O*)	000	7 f_O			0000	3.5 f_O*)	0000 0000 127.5_H
	111110 1 f_O		1111	9.0 f_O					
	111101 2 f_O		1110	9.5 f_O*)		1111	1.0 f_O	0000 0001	1_H
			1101	10.0 f_O		1110	1.5 f_O*)		1_H
						1101	2.0 f_O		
			0001	16.0 f_O					
	000000 63 f_O		0000	16.5 f_O*)		0001	8.0 f_O		
						0000	8.5 f_O*)	1111 1111	255_H

1: Oscillator and S sync active
0: external clock, f_H sync

*) In high-definition systems (line number > 768/field) the prescaler for 0.5 f_O resolution is bypassed: all-line-period pulses can then only be programmed in integer f_O.

Table 3 (cont'd)
Coding for Serial Programming



*) Number Equ. & Int. = number of pre-equalizing pulses = number of V_{sync} pulses = number of post-equalizing pulses. Different numbers of equalizing and V_{sync} pulses cannot be programmed.

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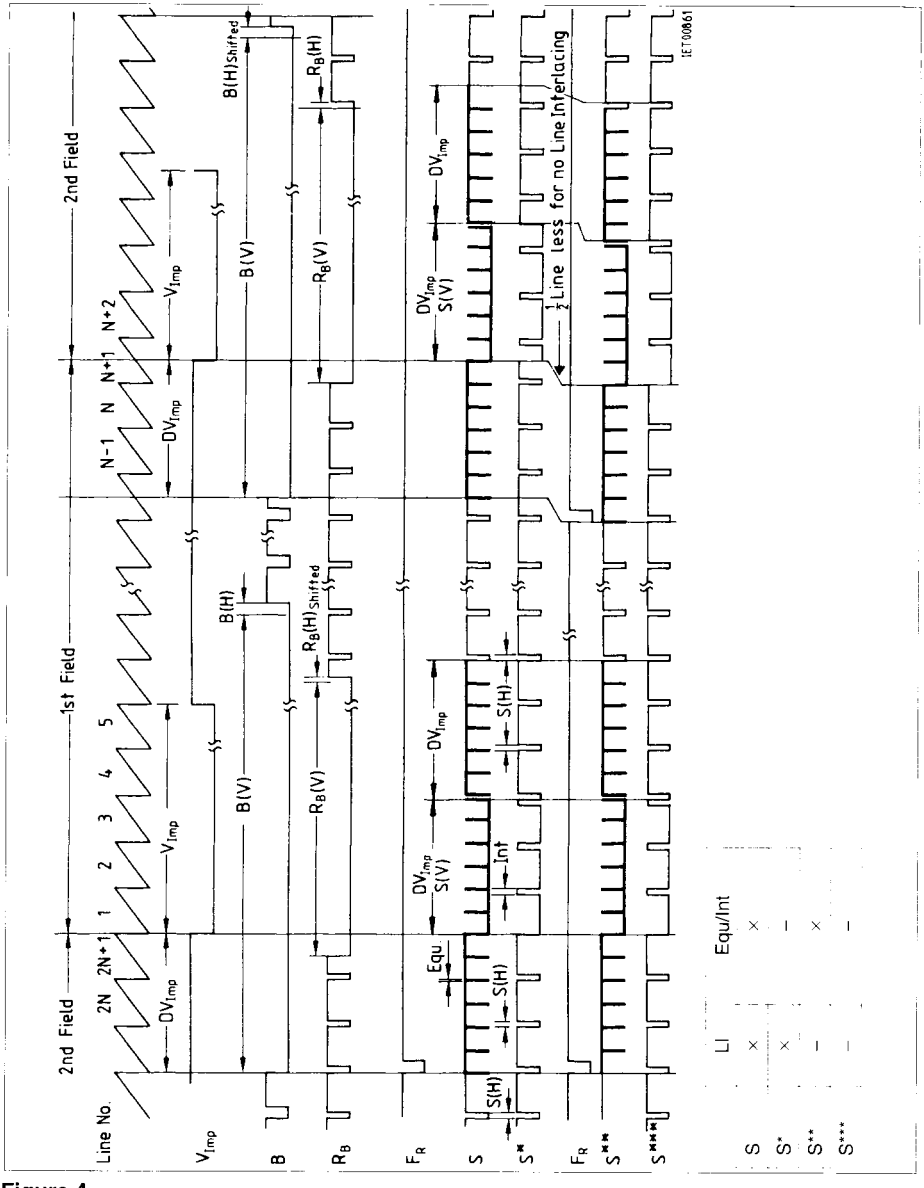

Figure 4
Composite Frame Signals for Even Number of Equalizing Pulses

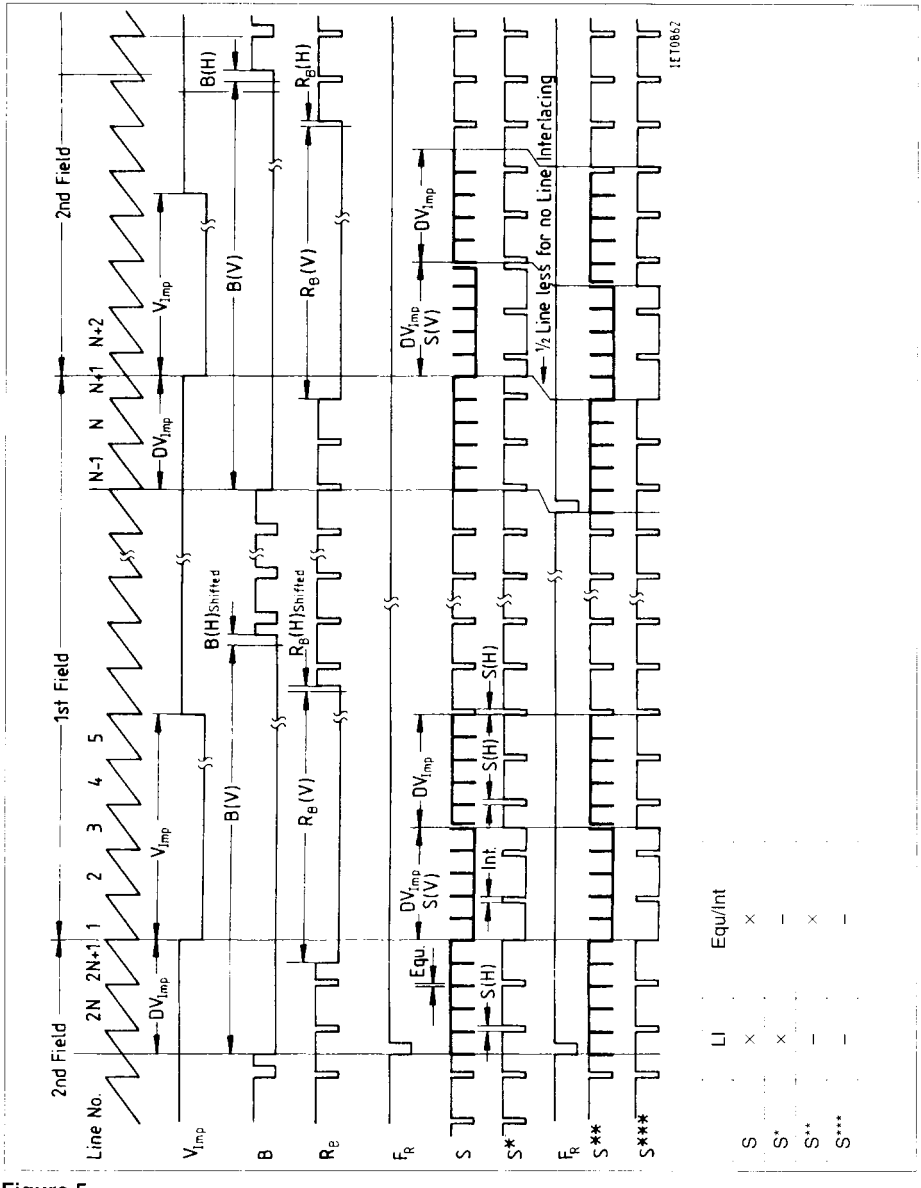

Figure 5
Composite Frame Signals for Odd Number of Equalizing Pulses

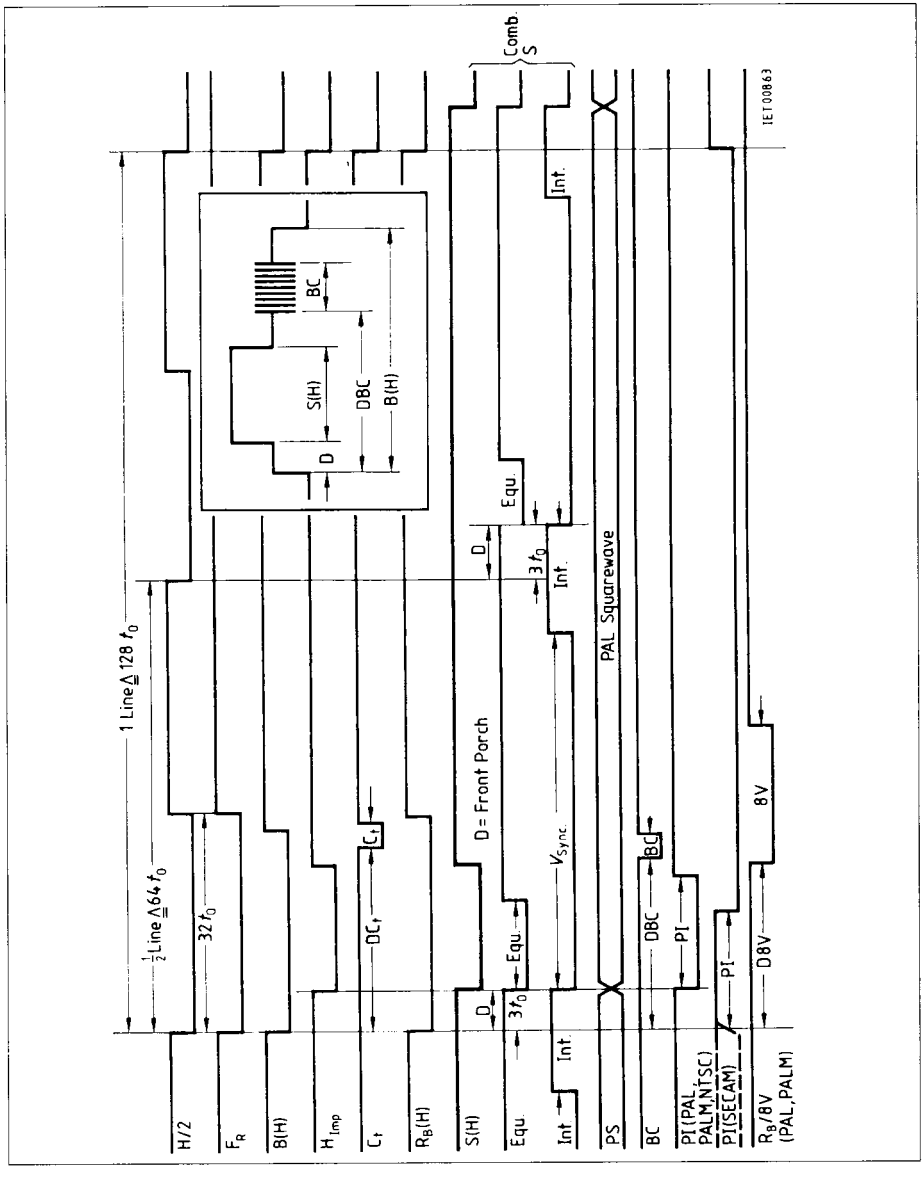

Figure 6
Line-Period Output Signals

Table 4
Pulse Widths for Auxiliary Color Signals

	PAL	SECAM	NTSC	PAL-M
S, H_{Imp}, V_{Imp}, V_R, B, B(H), C_t	refer to parallel system S1		refer to parallel system S2	
to	0.5 µs	0.5 µs	0.4965 µs	0.4965 µs
BC	2.25 µs 4.5 *to*	7.00 µs 14.0 *to*	2.5 µs 5 *to*	2.5 µs 5 *to*
DBC	7.00 µs 14.0 *to*	0	6.75 µs 13.5 *to*	7.25 µs 14.5 *to*
PI	4.75 µs 9.5 *to*	12.00 µs 24 *to*	–	4.75 µs 9.5 *to*
RB/8V	10 µs 20. *to*	–	–	10 µs 20 *to*
D8V	13.5 µs 27.0 *to*	–	–	13.5 µs 27.0 *to*
Field:		BC suppression (line number)*)		
4-1	623 ... 6	622.5 ... 22	523 ... 6	523 ... 8
1-2	310 ... 318	311. ... 335	261 ... 269	260 ... 270
2-3	622 ... 5	622.5 ... 22	523 ... 6	522 ... 7
3-4	311 ... 319	311. ... 335 **)	261 ... 269	259 ... 269

*) Assumption: line # 1 begins in all systems with the first V_{sync} pulse
**) In SECAM 1 BC appears during lines 7-15 and 320-328

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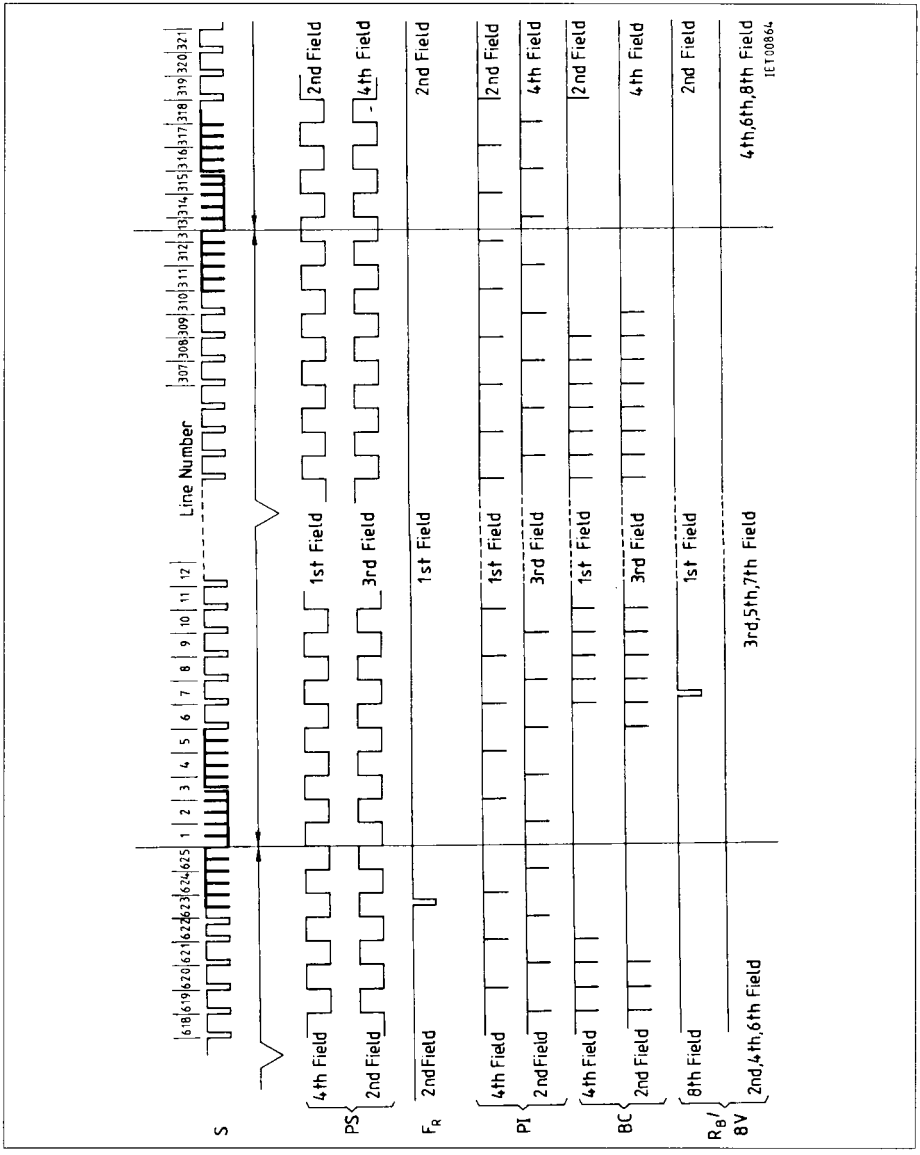

Figure 7
Color Identification Signals in PAL

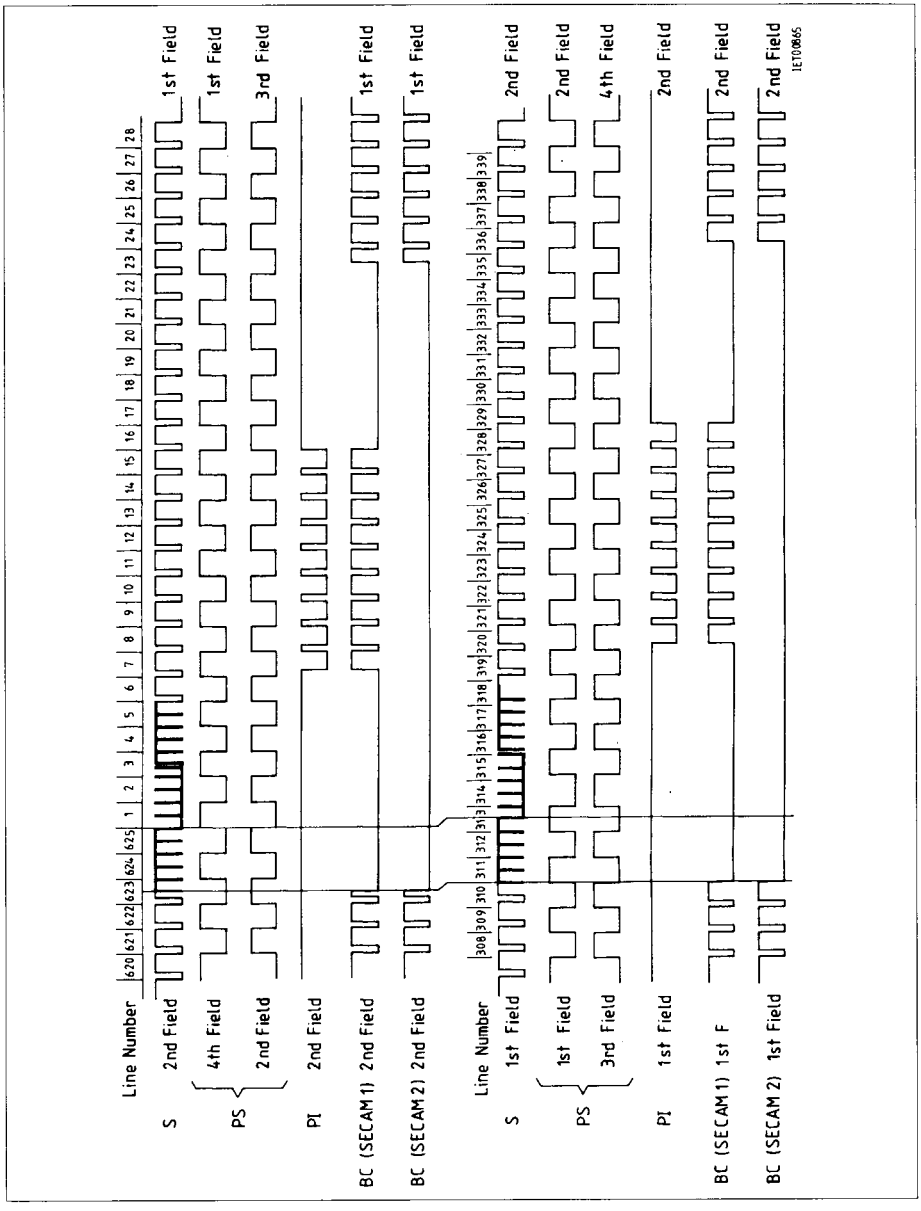

Figure 8
Color Identification Signals in SECAM

8

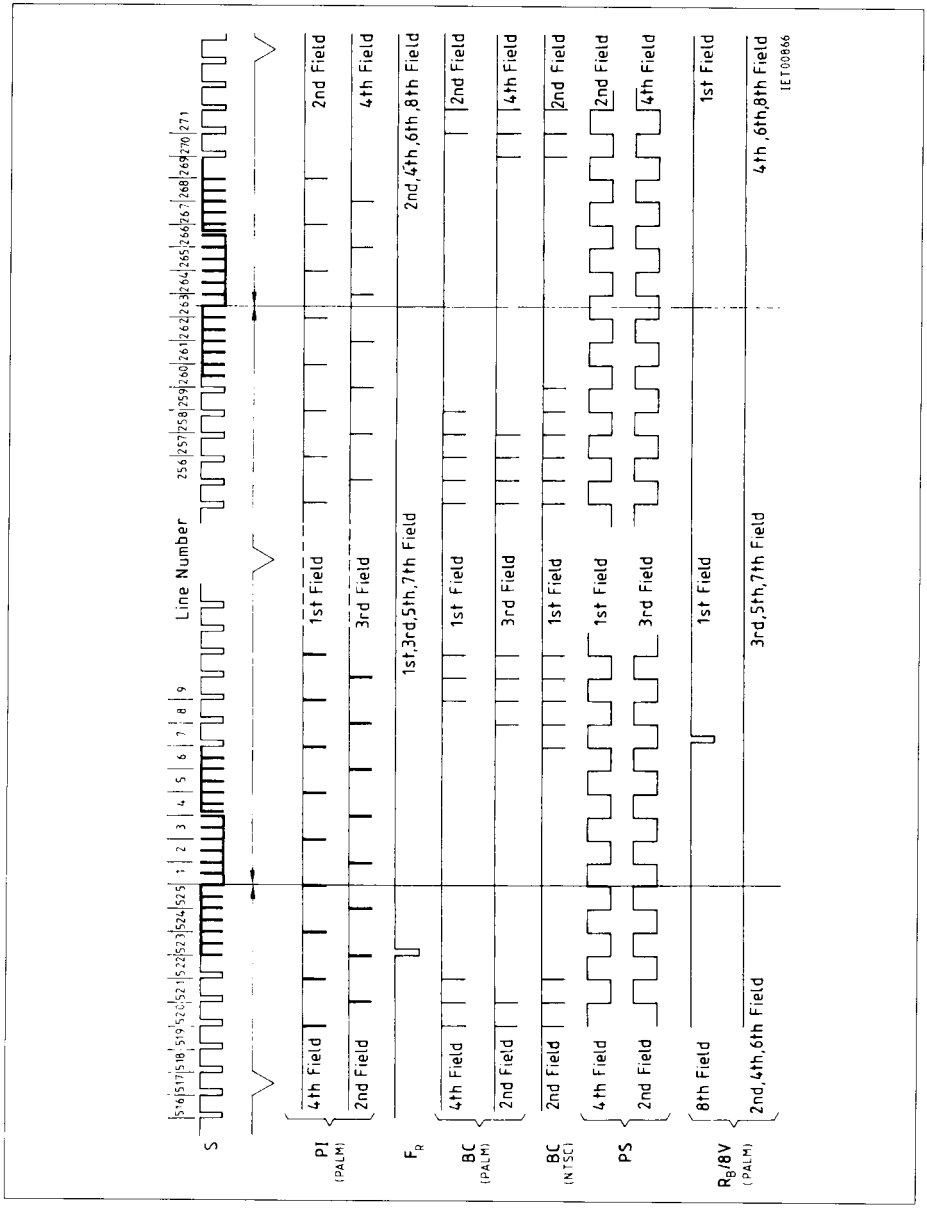

Figure 9
Color Identification Signals in NTSC and PAL-M