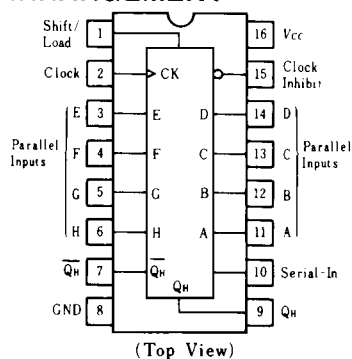


HD74HC165 ● Parallel-load 8-bit Shift Register

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the Shift/Load input. Also included is a gated clock input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the Shift/Load input high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

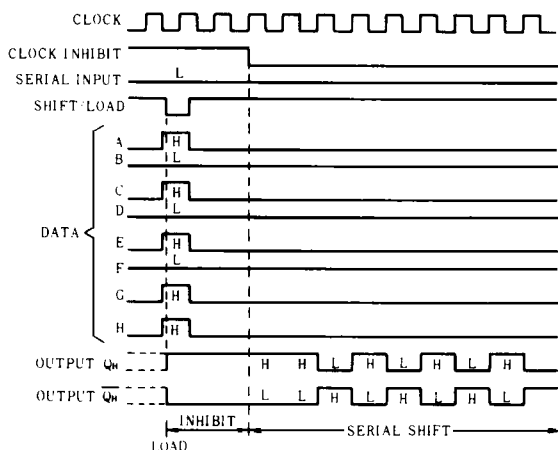
PIN ARRANGEMENT



FEATURES

- High Speed Operation: t_{pd} (Clock to Q_H)=21ns typ. (C_L =50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} =2~6V
- Low Input Current: $1\mu A$ max.
- Low Quiescent Supply Current: I_{CC} (static)=4 μA max. (T_a =25°C)

TIMING DIAGRAM



FUNCTION TABLE

Shift/Load		Inputs				Internal Outputs		Output
		Clock Inhibit	Clock	Serial	Parallel	Q_A	Q_B	Q_H
L	X	X	X	A.....H	Q_A	Q_B	Q_H	
H	L	L	X	a.....h	Q_{A0}	Q_{B0}	Q_{H0}	
H	L		H	X	H	Q_{An}	Q_{Gn}	
H	L		L	X	L	Q_{An}	Q_{Gn}	
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}	

DC CHARACTERISTICS

Item	Symbol	$V_{CC}(V)$	Test Conditions	$T_a = 25^\circ C$			$T_a = -40 \sim +85^\circ C$		Unit	
				min	typ	max	min	max		
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu A$	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5			4.18	—	—	4.13	—	
		6.0			5.68	—	—	5.63	—	
		6.0			—	—	—	—	—	
	V_{OL}	2.0	$V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu A$	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5			—	—	0.26	—	0.33	
		6.0			—	—	0.26	—	0.33	
		6.0			—	—	—	—	—	
Input Current	I_{in}	6.0	$V_{in} = V_{CC} \text{ or } GND$	—	—	± 0.1	—	± 1.0	μA	
Quiescent Supply Current	I_{CC}	6.0	$V_{in} = V_{CC} \text{ or } GND, I_{out} = 0 \mu A$	—	—	4.0	—	40	μA	

■ AC CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6\text{ns}$)

Item	Symbol	$V_{CC}(\text{V})$	Test Conditions	$T_a=25^\circ\text{C}$			$T_a=-40\sim+85^\circ\text{C}$		Unit		
				min	typ	max	min	max			
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz		
		4.5		—	—	27	—	21			
		6.0		—	—	32	—	25			
Propagation Delay Time	t_{PLH}	2.0	Clock to Q_H or \overline{Q}_H	—	—	150	—	190	ns		
		4.5		—	21	30	—	38			
		6.0		—	—	26	—	33			
	t_{PHL}	2.0	Shift/Load to Q_H or \overline{Q}_H	—	—	160	—	200			
		4.5		—	23	32	—	40			
		6.0		—	—	27	—	34			
			2.0	H to Q_H or \overline{Q}_H	—	—	150	—		190	
			4.5		—	21	30	—		38	
			6.0		—	—	26	—		33	
Setup Time	t_{su}	2.0	Parallel Data Inputs to Shift/Load	100	—	—	125	—	ns		
		4.5		20	-3	—	25	—			
		6.0		17	—	—	21	—			
		2.0	Serial Input to Clock	100	—	—	125	—			
		4.5		20	3	—	25	—			
		6.0		17	—	—	21	—			
			2.0	Shift/Load to Clock	100	—	—	125		—	
			4.5		20	—	—	25		—	
Removal Time	t_{rem}	2.0	Clock to Clock Inhibit or Clock Inhibit to Clock	100	—	—	125	—	ns		
		4.5		20	6	—	25	—			
		6.0		17	—	—	21	—			
Hold Time	t_h	2.0	Shift/Load to Parallel Data Input	5	—	—	5	—	ns		
		4.5		5	-3	—	5	—			
		6.0		5	—	—	5	—			
		2.0	Clock to Serial Data Input	5	—	—	5	—			
		4.5		5	3	—	5	—			
		6.0		5	—	—	5	—			
				2.0	Clock to Shift/Load	5	—	—		5	—
				4.5		5	—	—		5	—
6.0	5			—		—	5	—			
Pulse Width	t_w	2.0	Clock, Shift/Load	80	—	—	100	—	ns		
		4.5		16	6	—	20	—			
		6.0		14	—	—	17	—			
Output Rise/Fall Time	t_{TLH}	2.0		—	—	75	—	95	ns		
		4.5		—	5	15	—	19			
	t_{THL}	6.0		—	—	13	—	16			
Input Capacitance	C_{in}	—		—	5	10	—	10	pF		