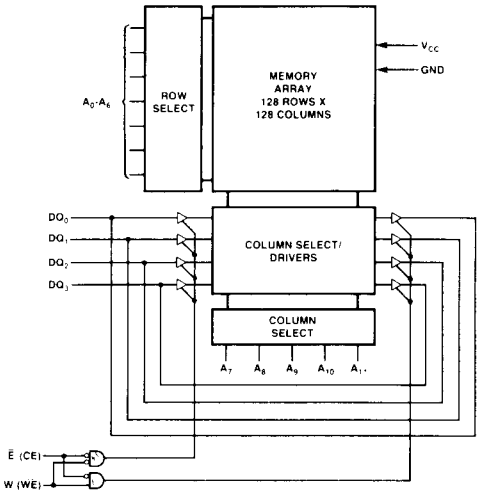
SR16K4

HIGH-SPEED 16K STATIC RAM (4K x 4)

FEATURES

- FULLY STATIC CMOS
  - No Clocks Required
- FAST ACCESS TIME = CYCLE TIME
  - SR16K4-25: 25 ns Max
  - SR16K4-35: 35 ns Max
  - SR16K4-45: 45 ns Max
- SINGLE POWER SUPPLY
  - 5V ± 10%
- LOW POWER
  - I_{CC} Active = 120 mA Max
  - I_{CC} Standby = 20 mA Max
- SMALL
  - 20 PIN 300 mil DIP
- STANDARD PINOUT
  - JEDEC-Approved
- TTL LOGIC LEVELS ON ALL PINS
- THREE STATE I/O

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The LATTICE SR16K4 is a 16,384-bit CMOS static RAM organized as 4096 words of 4 bits each. The SR16K4 is fabricated using LATTICE's advanced process Ultra-MOS®, offering the unprecedented combination of very high speed capability *and* low power in the same device.

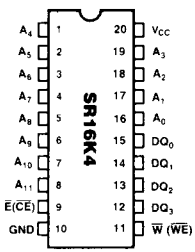
The $\overline{CE}$ pin, when logically high, holds the device in the low power standby mode, regardless of the levels on other pins. This feature provides substantial savings in both power and cooling requirements of many systems and contributes to enhanced reliability by lowering operating temperatures.

All inputs and outputs of the SR16K4 are completely TTL compatible and it operates from the standard, 5V ± 10%, logic power supply. Logic compatibility and the fully static nature of the SR16K4 combine to simplify the design of high performance memory systems.

PIN NAMES

A_0-A_{11}	ADDRESS	DQ_0-DQ_3	DATA IN/DATA OUT
$\overline{W}$ ($\overline{WE}$)	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{E}$ ($\overline{CE}$)	CHIP ENABLE	GND	GROUND

PIN CONFIGURATION



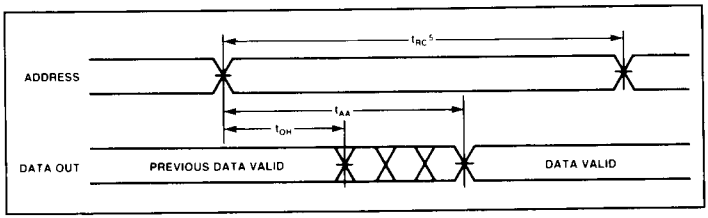
January 1986

LATTICE SEMICONDUCTOR CORP. 15400 NW GREENBRIER PKWY. BEAVERTON, OR 97006 503/629-2131 FAX 503/645-7921 TELEX 277338 LSC UR

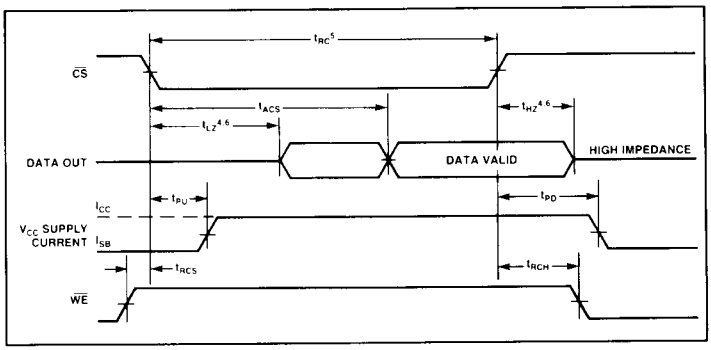
AC ELECTRICAL CHARACTERISTICS (READ CYCLE) (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

		SR16K4-25		SR16K4-35		SR16K4-45		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address Access Time	—	25	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	25	—	35	—	45	ns
t_{OH}	Output Hold From Address Change	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	—	10	—	10	—	15	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	20	—	30	—	40	ns
t_{RCS}	Read Command Set-up Time	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	ns

TIMING OF READ CYCLE NO. 1(1,2)

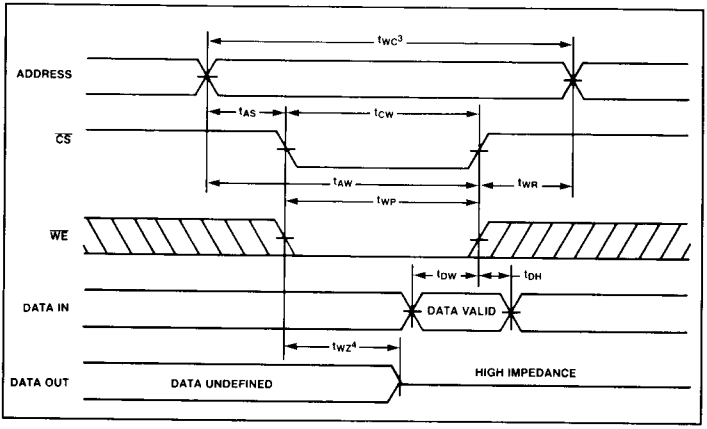


TIMING OF READ CYCLE NO. 2(1,3)



NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 1.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1,2]



NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200|mV from steady voltage with specified loading in Figure 1.
This parameter is sampled and not 100% tested.

TRUTH TABLE

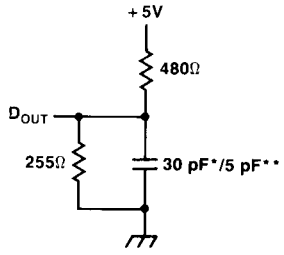
MODE	$\overline{CS}$	$\overline{WE}$	DQn	POWER
Standby	H	X	High Z	Standby
Read	L	H	Q (out)	Active
Write	L	L	D (in)	Active

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5|ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF



* Including scope and jig.
** 5 pF load used for testing t_{LZ}, t_{HZ}.

Figure 1. Output Load

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−3.0 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

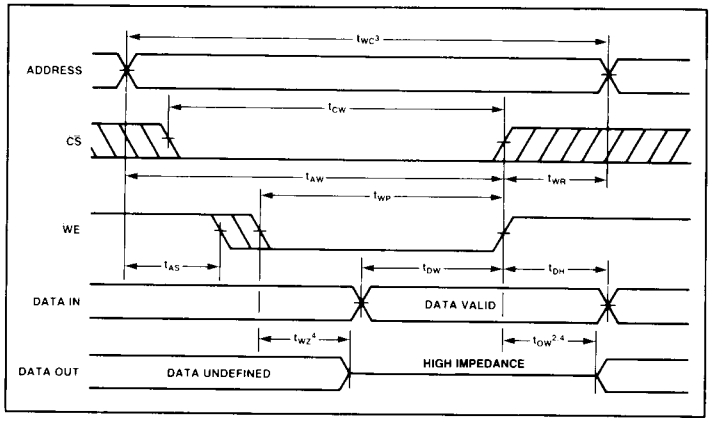
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNITS
$\|I_L\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, Output Open Min. Duty Cycle = 100%	—	120	mA
I_{SB}	Standby Power Supply Current	$\overline{CE} \geq V_{IH}$	—	20	mA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4.0mA	2.4	—	V
V_{IL}	Input Low Voltage		−2.0	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V

TTL ? CMOS STBY CURR

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE) (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

		SR16K4-25		SR16K4-35		SR16K4-45		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS
t_{WC}	Write Cycle Time	25	—	35	—	45	—	ns
t_{CW}	Chip Selection to End of Write	20	—	25	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	35	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	25	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	15	—	20	—	ns
t_{DH}	Data Hold Time	3	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	—	10	—	15	—	20	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	ns

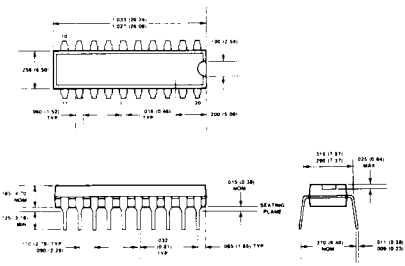
TIMING OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



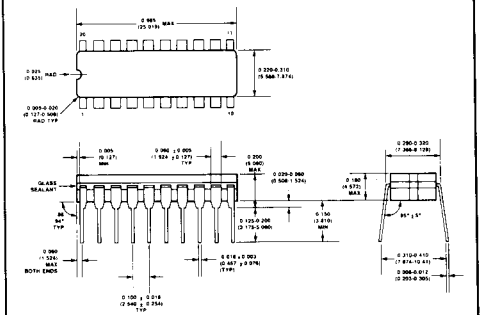
NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady voltage with specified loading in Figure 1. This parameter is sampled and not 100% tested.

PACKAGE INFORMATION

20-PIN, 300-MIL PLASTIC DIP



20-PIN, 300-MIL CERDIP



ORDERING INFORMATION

SR16K4-35 X X X /883C

*Mil Process:	Blank	No Mil. Process
	/883C	883C Process
Burn In:	Blank	No Burn-in
	B	Burned In
Temperature:	Blank	0°-70°
	M	-55°-125°
	I	-25°-85°
Package:	C	Sidebrazed Dip
	D	CERDIP
	P	Plastic Dip
	R	LCC
	J	PLCC (J Lead)
	U	DIE
Speed (ns)	(i.e. -35, -45, etc.)	
Device Name:	SR16K4	

*Omit temperature and burn in letter designators when ordering 883C processed devices.