

SN54AS8838, SN74AS8838 32-BIT BARREL SHIFTERS

D2938, NOVEMBER 1985—REVISED MARCH 1986

- High-Speed "Flash" Shift Operations
- Shifts up to 32 Positions in Less than 25 ns
- Performs Logical, Circular, and Arithmetic Shifts
- 3-State Outputs Allow 32-Bit and 16-Bit Bus Interface
- 24-mA Bus Drivers
- 84-Pin Package
- Uses Less than 1.5 W (Max)
- Texas Instruments Quality and Reliability

description

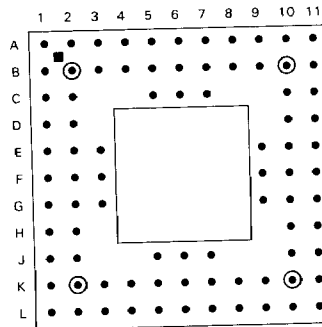
The SN54AS8838 and SN74AS8838 are high-speed 32-bit barrel shifters in an 84-pin ceramic pin-grid array. The devices can shift up to 32 bits in a single instruction cycle of under 25 nanoseconds. Five basic shifts can be programmed: circular left and right, logical left and right, and arithmetic right.

Unlike conventional shift registers, whose shift operations are controlled by the number of input clock pulses applied, the number of positions to be shifted by the 'AS8838 is determined by an input decoder. This form of implementation does not require an input clock, thus, the shift operation is restricted only by internal propagation delays. The delay is the same regardless of the number of positions to be shifted, resulting in a high-speed "flash" shift.

Three-state output controls allow the devices to be interfaced with 32- or 16-bit data buses.

The SN54AS8838 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS8838 is characterized for operation from 0°C to 70°C.

SN54AS8838, SN74AS8838
GB PIN-GRID-ARRAY PACKAGE
(TOP VIEW)



PIN		PIN	
NO.	NAME	NO.	NAME
A1	GND	F9	Y0EL
A2	VCC2	F10	Y7
A3	Y30	F11	Y6
A4	Y28	G1	D20
A5	Y25	G2	D19
A6	Y23	G3	D18
A7	GND	G9	Y4
A8	Y20	G10	Y5
A9	Y18	G11	GND
A10	Y16	H1	D17
A11	GND	H2	D16
B1	D31	H10	Y2
B2	GND	H11	Y3
B3	Y31	J1	D15
B4	Y29	J2	D14
B5	Y26	J5	D7
B6	Y24	J6	D2
B7	Y22	J7	MUX1
B8	Y19	J10	Y0
B9	Y17	J11	Y1
B10	VCC1	K1	VCC1
B11	Y15	K2	D13
C1	D29	K3	D11
C2	D30	K4	D9
C5	Y27	K5	D6
C6	Y0EM	K6	D3
C7	Y21	K7	D0
C10	Y14	K8	SFT4
C11	Y13	K9	GND
D1	D27	K10	SFT1
D2	D28	K11	SFT0
D10	Y12	L1	GND
D11	Y11	L2	D12
E1	D24	L3	D10
E2	D25	L4	D8
E3	D26	L5	D5
E9	Y10	L6	D4
E10	Y9	L7	D1
E11	Y8	L8	MUX0
F1	D23	L9	SFT3
F2	D22	L10	VCC2
F3	D21	L11	SFT2

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This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

TEXAS
INSTRUMENTS

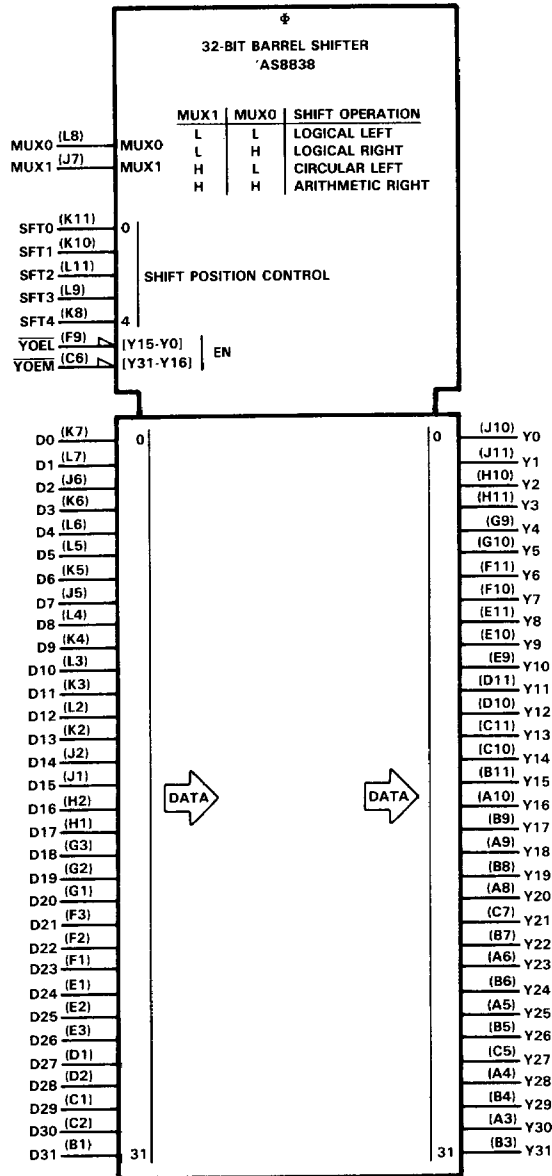
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32-BIT BARREL SHIFTERS

logic symbol†



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†This symbol is in accordance with ANSI/IEEE Std 91-1984.

PIN		I/O	DESCRIPTION
NAME	NO.		
D0	K7	I	Input data bits 0 through 31
D1	L7		
D2	J6		
D3	K6		
D4	L6		
D5	L5		
D6	K5		
D7	J5		
D8	L4		
D9	K4		
D10	L3		
D11	K3		
D12	L2		
D13	K2		
D14	J2		
D15	J1		
D16	H2		
D17	H1		
D18	G3		
D19	G2		
D20	G1		
D21	F3		
D22	F2		
D23	F1		
D24	E1		
D25	E2		
D26	E3		
D27	D1		
D28	D2		
D29	C1		
D30	C2		
D31	B1		
GND	A1		Ground (All ground pins must be used.)
GND	A7		
GND	A11		
GND	B2		
GND	G11		
GND	L1		
MUX0	L8	I	Shift instruction control. Specifies the type of shift operation to be performed. See Table 1 for further information.
MUX1	J7		
SFT0	K11	I	Shift position control. Specifies the number of bit positions to shift. See Table 1 for further information.
SFT1	K10		
SFT2	L11		
SFT3	L9		
SFT4	K8		
VCC1	B10		5-Volt supply for TTL-compatible I/O
VCC1	K1		
VCC2	A2		2-Volt supply for internal Schottky Transistor Logic (STL)
VCC2	L10		

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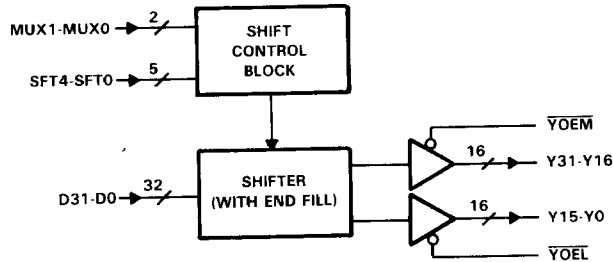
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PIN		I/O	DESCRIPTION
NAME	NO.		
Y0	J10	O	Output data bits 0 through 10
Y1	J11		
Y2	H10		
Y3	H11		
Y4	G9		
Y5	G10		
Y6	F11		
Y7	F10		
Y8	E11		
Y9	E10		
Y10	E9		
Y11	D11	O	Output data bits 11 through 31
Y12	D10		
Y13	C11		
Y14	C10		
Y15	B11		
Y16	A10		
Y17	B9		
Y18	A9		
Y19	B8		
Y20	A8		
Y21	C7		
Y22	B7		
Y23	A6		
Y24	B6		
Y25	A5		
Y26	B5		
Y27	C5		
Y28	A4		
Y29	B4		
Y30	A3		
Y31	B3		
Y0EL	F9	I	Control input for the Y15-Y0 output port. When Y0EL is low, Y15-Y0 is enabled.
Y0EM	C6	I	Control input for the Y31-Y16 output port. When Y0EM is low, Y31-Y16 is enabled.

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functional block diagram



data input/output

Data is input to the 'AS8838 through the D31-D0 data port and output through two 16-bit data ports, Y31-Y16 and Y15-Y0. Two 3-state output controls enable the Y data ports. The most significant half of the shift result is enabled when $\overline{YOEM}$ is low, the least significant half when $\overline{YOEL}$ is low.

shift control block

The shift control block decodes the MUX1-MUX0 instruction inputs and the SFT4-SFT0 shift position controls and transmits the resulting control signals to the shifter. MUX1-MUX0 control shift instruction selection as shown in Table 1. SFT4-SFT0 specify the number of bit positions to be shifted. For right shifts, the two's complement of the number of bit positions must be placed on SFT4-SFT0.

TABLE 1. INSTRUCTION SET

MUX1	MUX0	FUNCTION	OPERATION
L	L	Logical Left Shift	Shift left the number of bit positions defined by SFT4-SFT0. Fill vacated bit positions with zeros.
L	H	Logical Right Shift	Shift right the number of bit positions specified by the two's complement of SFT4-SFT0. Fill vacated bit positions with zeros. (A logical right shift with SFT4-SFT0 = 0 will fill all bits with zeros.)
H	L	Circular Left Shift	Circular left shift the number of bit positions defined by SFT4-SFT0. (A circular right shift can be performed by putting the two's complement of number of bits to be shifted on SFT4-SFT0.)
H	H	Arithmetic Right Shift	Shift right the number of bit positions defined by the two's complement of SFT4-SFT0. Fill vacated bit positions with the D31 input value (sign bit). (An arithmetic right shift with SFT4-SFT0 = 0 will fill all bits with the sign bit.).

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shift operation examples

logical shift left (M1 – M0 = LL)

In the shift left mode, SFT4-SFT0 define the number of bit positions to be shifted. The following example shifts a 32-bit word 8 positions to the left and fills the vacated bit positions with zeros.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
00	01000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data

1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result

1100 1101 0000 0001 0010 0011 0000 0000

logical shift right (M1 – M0 = LH)

In the shift right mode, the two's complement of the number of bit positions to be shifted must be placed on SFT4-SFT0. The following example shifts a 32-bit word 8 positions to the right and fills the vacated bit positions with zeros.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
01	11000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data

1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result

0000 0000 1010 1011 1100 1101 0000 0001

circular shift left ($M1 - M0 = HL$)

In the circular shift left mode, SFT4-SFT0 define the number of bit positions to be shifted. The following example circular shifts a 32-bit word 8 positions to the left.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
10	01000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data

1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result

1100 1101 0000 0001 0010 0011 1010 1011

circular shift right ($M1 - M0 = HL$)

A circular right shift can be performed by placing the two's complement of the number of bit positions to be shifted on SFT4-SFT0 and using the circular left shift mode ($M1 - M0 = HL$). The following example circular shifts a 32-bit word 8 positions to the right.

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
10	11000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data

1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result

0010 0011 1010 1011 1100 1101 0000 0001

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arithmetic shift right (M1 – M0 = HH)

In the arithmetic shift right mode, SFT4-SFT0 define the number of bit positions to be shifted. The following example shifts a 32-bit word 8 positions to the right and fills the vacated bit positions with the sign bit (D31 from the input data).

CONTROL SIGNALS

SHIFT INSTRUCTION M2-M0	NUMBER OF BITS TO SHIFT SFT4-SFT0
11	11000

Assume D31-D0 is hex ABCD0123.

D31-D0

Input Data 1010 1011 1100 1101 0000 0001 0010 0011

Y31-Y0

Result 1111 1111 1010 1011 1100 1101 0000 0001

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, VCC1	7 V
Supply voltage, VCC2	3 V
Input voltage	7 V
Operating case temperature range: SN54AS8838	–55°C to 125°C
Operating free-air temperature range: SN74AS8838	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

PARAMETER	SN54AS8838			SN74AS8838			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
VCC1 I/O supply voltage	4.5	5	5.5	4.5	5	5.5	V
VCC2 STL internal logic supply voltage	1.9	2	2.1	1.9	2	2.1	V
VIH High-level input voltage	2			2			V
VIL Low-level input voltage			0.8			0.8	V
IOH High-level output current			–1			2.6	mA
IOL Low-level output current			12			24	mA
TA Operating free-air temperature	–55			0		70	°C
TC Operating case temperature			125				°C