BURR - BROWN®

ADS7809

ADVANCE INFORMATION
SUBJECT TO CHANGE

16-Bit 10µs Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

FEATURES

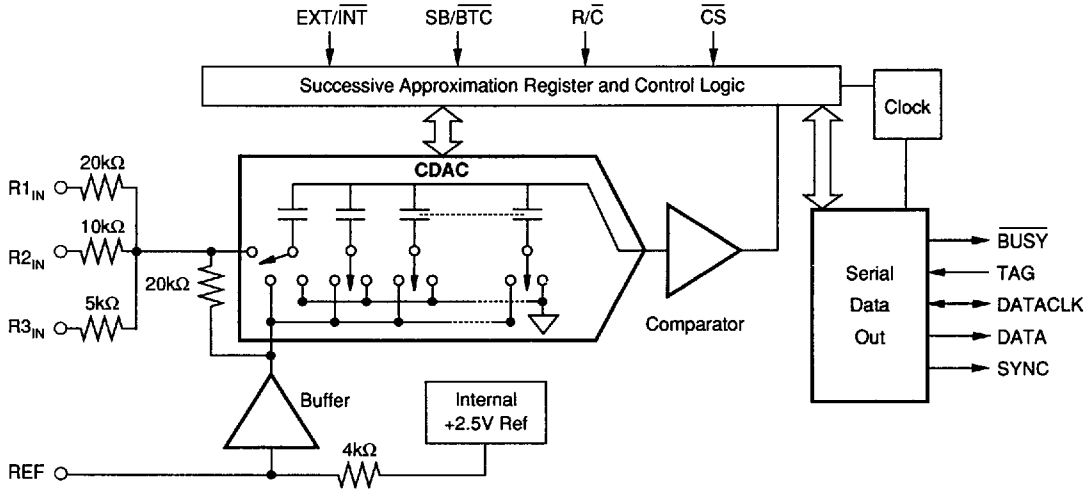
- 100kHz SAMPLING RATE
- 86dB SINAD WITH 45kHz INPUT
- ±1 LSB INL AND DNL
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7808
- USES INTERNAL OR EXTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- SERIAL DATA w/INTERNAL OR EXTERNAL CLOCK
- 100mW MAX POWER DISSIPATION
- 20-PIN 0.3" PLASTIC DIP AND SOIC
- SIMPLE DSP INTERFACE

DESCRIPTION

The ADS7809 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The 20-pin ADS7809 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range. It is also available in die form.



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SPECIFICATIONS

ELECTRICAL

T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809AP/AU MIN	ADS7809AP/AU TYP	ADS7809AP/AU MAX	ADS7809BP/BU MIN	ADS7809BP/BU TYP	ADS7809BP/BU MAX	UNITS
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges				±10, 0V to 5V, etc. (See Table I)			V	
Impedance				See Table I				
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			7	8		*	*	µs
Complete Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
Recovery to Rated Accuracy after Power Down			35			*		µs
DC ACCURACY								
Integral Linearity Error				±3			±1	LSB[1]
Differential Linearity Error				±3			±1	LSB
No Missing Codes		14			16			Bits
Transition Noise[2]			1.6			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±15			*	LSB
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10			*	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2			*		ppm/°C
Unipolar Zero Error[3]	Unipolar Ranges			±10			*	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2			*		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 45kHz	90			96			dB[5]
Total Harmonic Distortion	f_{IN} = 45kHz			–90			–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 45kHz	83			86			dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 45kHz	83			86			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			Sufficient to meet AC specs			*		ns
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.4	2.5	2.6	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		µA
External Reference Voltage Range For Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D+0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA

SPECIFICATIONS (CONT)

ELECTRICAL

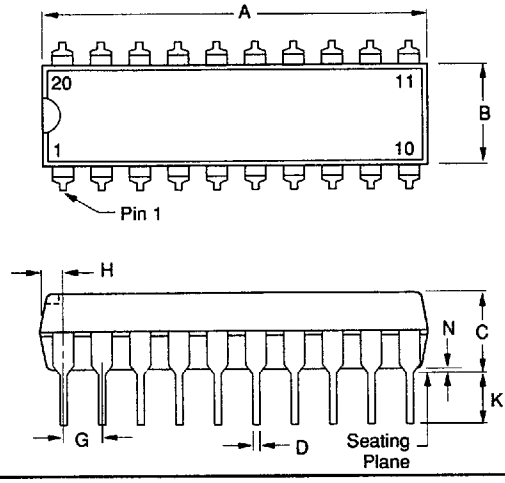
T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809AP/AU MIN	ADS7809AP/AU TYP	ADS7809AP/AU MAX	ADS7809BP/BU MIN	ADS7809BP/BU TYP	ADS7809BP/BU MAX	UNITS
DIGITAL OUTPUTS								
Data Format				Serial 16-bits				
Data Coding				Selectable for Binary Two's Complement or Straight Binary				
Pipeline Delay				Conversion results only available after completed conversion.				
Data Clock				Selectable for internal or external data clock				
Internal	EXT/$\overline{INT}$ LOW		1.3			*		MHz
(Output Only When Transmitting Data)								
External	EXT/$\overline{INT}$ HIGH	0.1		10	*		*	MHz
(Can Run Continually)								
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
Power Dissipation	f_S = 100kHz			100			*	mW
	PWRD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305uV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

MECHANICAL

P Package — 20-Pin Plastic DIP

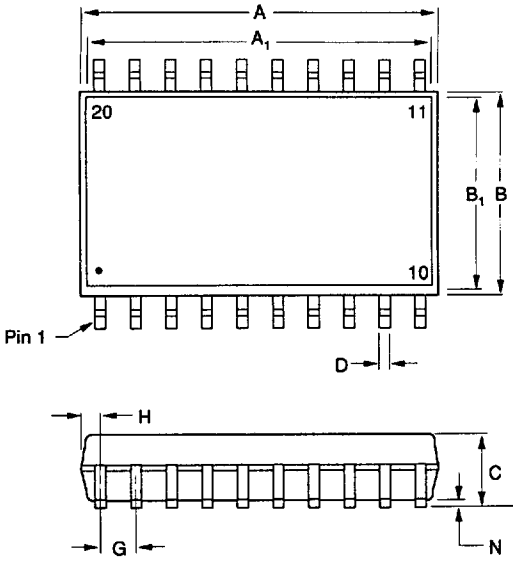


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.980	1.020	24.89	25.91
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.59
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	.000	.020	0.00	0.51

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

MECHANICAL (CONT)

U Package — 20-Pin Plastic SOIC



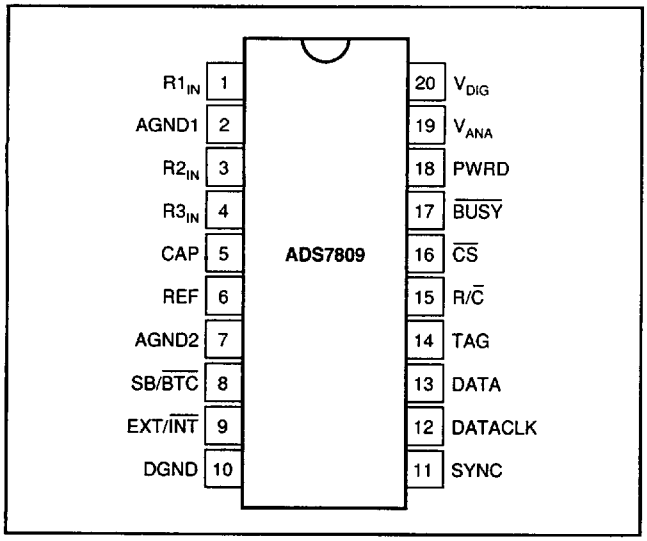
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.502	.518	12.75	13.16
A_1	.495	.518	12.57	13.16
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	$R1_{IN}$	Analog Input. See Table I for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	$R2_{IN}$	Analog Input. See Table I for input range connections.
4	$R3_{IN}$	Analog Input. See Table I for input range connections.
5	CAP	Reference Compensation Capacitor. 2.2µF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal reference of 2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 2.2µF Tantalum capacitor.
7	AGND2	Analog Ground.
8	SB/$\overline{BTC}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/$\overline{INT}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	SYNC	Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If INT/$\overline{EXT}$ is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. If EXT/$\overline{INT}$ is HIGH, data will be valid on the falling edge of DATACLK. In this external clock mode, after 16-bits of data, the ADS7809 will output the level input on TAG, delayed by 16 DATACLK pulses. If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK. Between conversions, DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses.
15	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC for synchronization to processors, and initiates the transmission of data from the previous conversion.
16	$\overline{CS}$	Chip Select. Is internally OR'ed with R/$\overline{C}$ so that whichever falls last starts the conversion cycle.
17	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start, without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register, which can be read during the power down mode in the external clock mode (EXT/$\overline{INT}$ HIGH).
19	V_{ANA}	Analog Supply Input. Nominally +5V. Connect directly to pin 19, and decouple with to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
20	V_{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 20. Must be ≤ V_{ANA}.

PIN CONFIGURATION



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40			ns
t_2	BUSY Delay from R/C LOW			65	ns
t_3	BUSY LOW			8	µs
t_4	BUSY Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		7	8	µs
t_7	Acquisition Time	2			µs
t_8	R/C LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns
$t_6 + t_7$	Throughput Time		9	10	µs

TABLE II. Conversion Timing.

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 100Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ VIA 50Ω TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ

TABLE I. Input Range Connections.

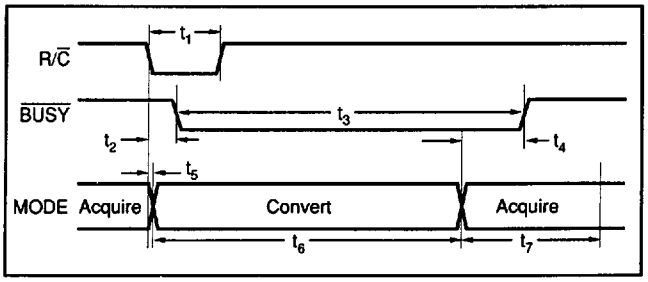


FIGURE 1. Conversion Timing (CS Tied LOW.)

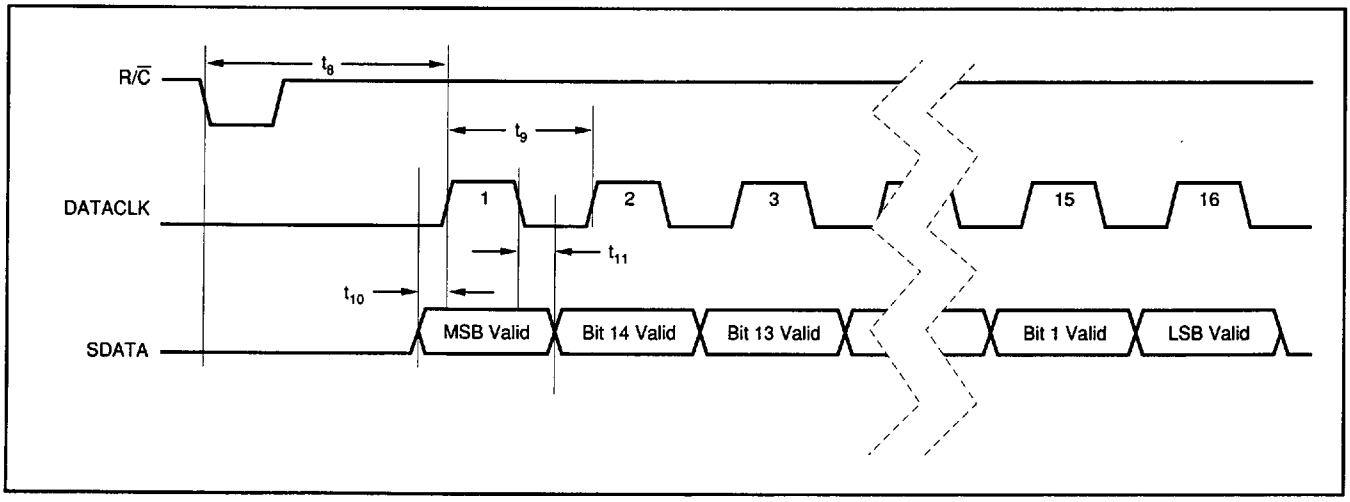


FIGURE 2. Serial Data Timing Using Internal Clock. (CS, EXT/INT and TAG Tied LOW.)