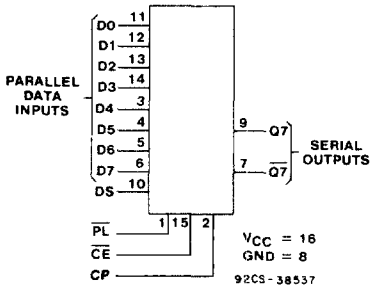
CD54/74HC165
CD54/74HCT165

File Number **1672**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Bit Parallel-In/ Serial-Out Shift Register

Type Features:

- *Buffered Inputs*
- *Asynchronous Parallel Load*
- *Complementary Outputs*
- *Typical f_{MAX} = 60 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25°C*

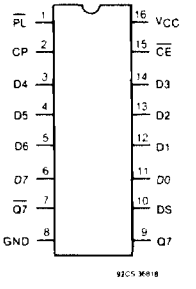
The RCA-CD54/74HC165 and CD54/74HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs (Q7 and $\overline{Q7}$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously. When the $\overline{PL}$ is HIGH, data enters the register serially at the DS input and shifts one place to the right (Q0→Q1→Q2, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q7 output to the DS input of the succeeding device.

For predictable operation the LOW-to-HIGH transition of $\overline{CE}$ should only take place while CP is HIGH. Also, CP and $\overline{CE}$ should be LOW before the LOW-to-HIGH transition of PL to prevent shifting the data when $\overline{PL}$ goes HIGH.

The CD54HC/HCT165 devices are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT165 devices are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC165
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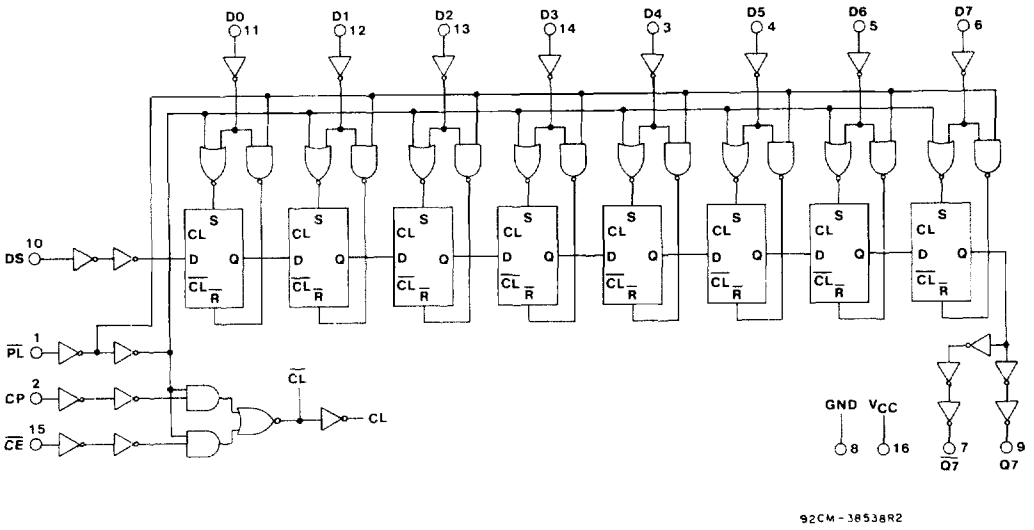

Fig. 1 — Logic diagram for the CD54/74HC165 and CD54/74HCT165.

TRUTH TABLE

Operating Modes	Inputs					Q_n Register	Outputs		
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0-D7	Q0	Q1-Q6	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial Shift	H	L	⎍	l	X	L	q_0-q_5	q_6	$\overline{q_6}$
	H	L	⎍	h	X	H	q_0-q_5	q_6	$\overline{q_6}$
Hold "Do Nothing"	H	H	X	X	X	q_0	q_1-q_6	q_7	$\overline{q_7}$

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
⎍ = LOW-to-HIGH clock transition.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC165/CD54HC165										CD74HCT165/CD54HCT165									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5 to 5.5								
			4.5	3.15	—	—	3.15	—	3.15	—	—		2	—	—	2	—	2	—	V
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5 to 5.5								
			4.5	—	—	1.35	—	1.35	—	1.35	—		—	—	0.8	—	0.8	—	0.8	V
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DS, D0 to D7	0.35
CP, $\overline{PL}$	0.65

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5$V) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay					
CP to Q7	15	t_{PHL}	13	17	ns
$\overline{PL}$ to Q7	15	t_{PLH}	14	17	ns
D7 to Q7	15		12	14	ns
Power Dissipation Capacitance*	—	C_{PD}	17	24	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t_{WL}	2	80	—	—	—	100	—	—	—	120	—	—	—	
	t_{WH}	4.5	16	—	18	—	20	—	23	—	24	—	27	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{PL}$ Pulse Width	t_{WL}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time		2	80	—	—	—	100	—	—	—	120	—	—	—	
DS to CP	t_{SU}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{CE}$ to CP	$t_{SU(\overline{CE})}$	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
D0-D7 to $\overline{PL}$	t_{SU}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time		2	35	—	—	—	45	—	—	—	55	—	—	—	
DS to CP	t_H	4.5	7	—	7	—	9	—	9	—	11	—	11	—	ns
or $\overline{CE}$		6	6	—	—	—	8	—	—	—	9	—	—	—	
		2	0	—	—	—	0	—	—	—	0	—	—	—	
$\overline{CE}$ to CP	t_H	4.5	0	—	0	—	0	—	0	—	0	—	0	—	ns
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Recovery Time		2	100	—	—	—	125	—	—	—	150	—	—	—	
$\overline{PL}$ to CP	t_{REC}	4.5	20	—	20	—	25	—	25	—	30	—	30	—	ns
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Maximum Clock		2	6	—	—	—	5	—	—	—	4	—	—	—	
Pulse Frequency	f_{MAX}	4.5	30	—	27	—	24	—	22	—	20	—	18	—	MHz
		6	35	—	—	—	28	—	—	—	24	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
CP or $\overline{CE}$ to	t_{PHL}	4.5	—	33	—	40	—	41	—	50	—	50	—	60	ns
Q7 or $\overline{Q7}$		6	—	28	—	—	—	35	—	—	—	43	—	—	
	t_{PLH}	2	—	175	—	—	—	220	—	-	—	265	—	—	
$\overline{PL}$ to Q7 or	t_{PHL}	4.5	—	35	—	40	—	44	—	50	—	53	—	60	ns
$\overline{Q7}$		6	—	30	—	—	—	37	—	—	—	45	—	—	
	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
D7 to Q7 or	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
$\overline{Q7}$		6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Output Transition	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Time		6	—	13	—	—	—	16	—	—	—	19	—	—	
			—	—	—	—	—	—	—	—	—	—	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
			—	—	—	—	—	—	—	—	—	—	—	—	

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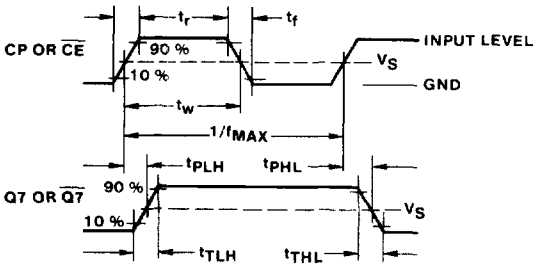
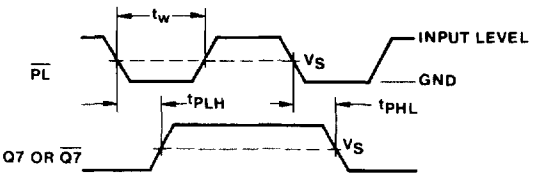
CD54/74HCT165



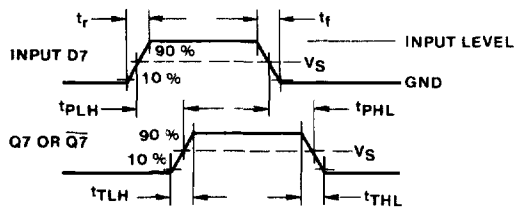
(a) SERIAL-SHIFT MODE

92CS-38539



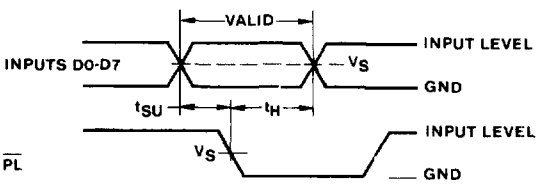
(b) PARALLEL-LOAD MODE

92CS-38540



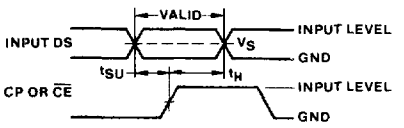
(c) PARALLEL-LOAD MODE

92CS-38541

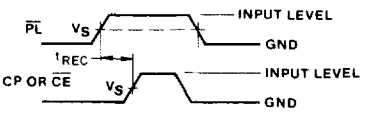


(d) PARALLEL-LOAD MODE

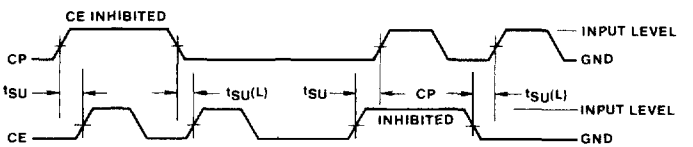
92CS-38542



(e) SERIAL-SHIFT MODE



(f) SERIAL-SHIFT MODE



(g) SERIAL-SHIFT, CLOCK-INHIBIT MODE

92CM-38543R2

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 — Switching waveforms for the CD54/74HC165 and the CD54/74HCT165