UM3881B

Dot Matrix LCD Controller and Driver

Features

- Internal LCD drivers
  - 16 common signal drivers
  - 40 segment signal drivers
  - (can be externally extended to 400 segments using UM3882)
- Maximum display dimensions
  - 40 characters * 2 lines or
  - 80 characters * 1 line
- Interfaces with 4-bit or 8-bit MPU
- Versatile display functions provided on-chip:
  - Display Clear, Cursor Home, Display ON/OFF Cursor ON/OFF, Character Blinking, Cursor Shift, Display Shift
- Three duty factors, selected by PROGRAM:
  - 1/8 , 1/11, and 1/16
- Display Data RAM (DD RAM): 80 x 8 bits (displays up to 80 characters)
- Character Generator RAM (CG RAM):
  - 64x8 bits for general data,
  - 8 5x8 programmable dot patterns, or
  - 4 5x10 programmable dot patterns
- Character Generator ROM (CG ROM):
  - 3 kinds of CG ROM sizes:
    - 192 characters:
      - 160 5x8 dot patterns
      - 32 5x10 dot patterns
    - 240 characters:
      - 192 5x8 dot patterns
      - 48 5x10 dot patterns
    - 256 characters:
      - 192 5x8 dot patterns
      - 64 5x10 dot patterns
  - Custom CG ROM is also available
- Built-in power-on reset function
- Logic power supply: single + 5V supply
- LCD driver power supply: V1 - V5 (V_{DD} + 0.3 - V_{DD} - 13.5)
- Three oscillator operations (Freq. = 250KHz - 270KHz):
  - .Internal oscillation
  - .Ceramic filter
  - .External clock
- CMOS Process
- 80-Pin Quad Flat Package (QFP) or in CHIP FORM

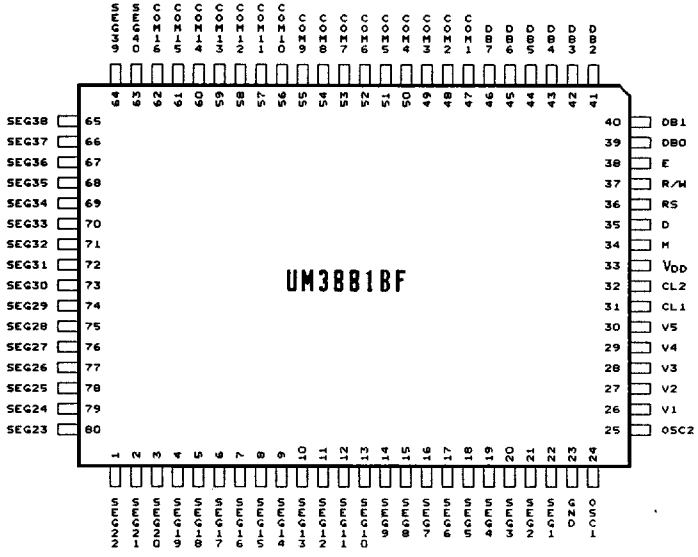
General Description

The UM3881B is a dot matrix LCD controller and driver LSI that can operate with either a 4-bit or an 8-bit microprocessor (MPU). UM3881B receives control character codes from the MPU, stores them in an internal RAM (up to 80 characters), transforms each character code into a 5x7, 5x8, or 5x10 dot matrix character pattern, and then displays the codes on the LCD panel. The built-in Character Generator ROM consists of 256 different character patterns.

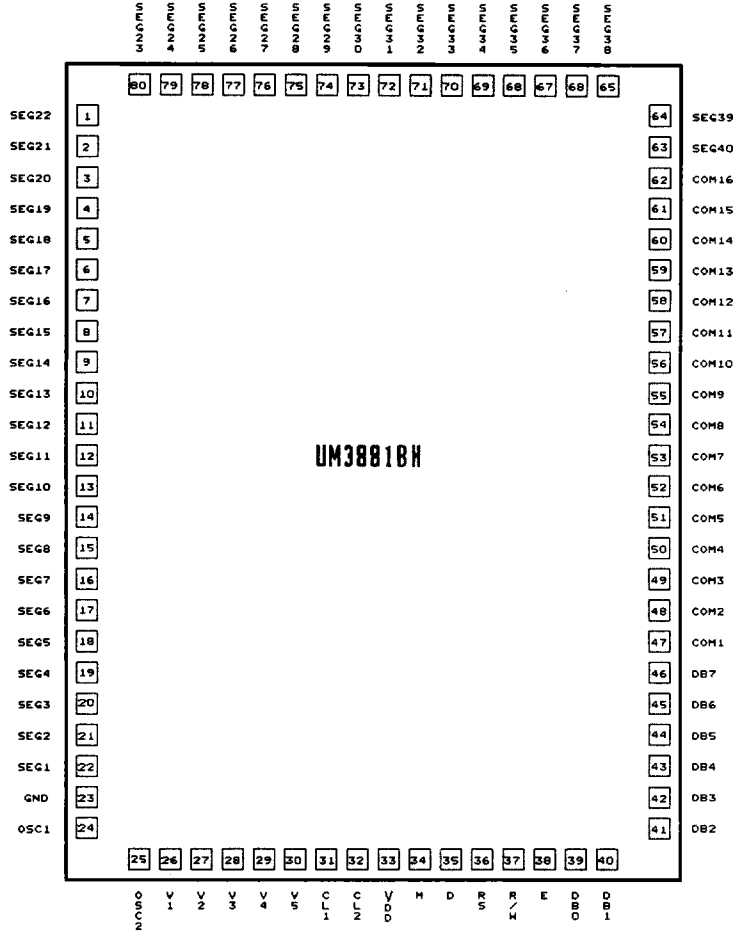
The UM3881B also contains Character Generator RAM where the user can store 8 different character patterns at run time. These memory features make character display flexible. UM3881B also provides many display instructions to achieve versatile LCD display functions. The UM3881B is fabricated on a single LSI chip using CMOS process, resulting in very low power requirements.

With several UM3882 driver ICs connected to the UM3881B, up to 80 characters can be displayed.

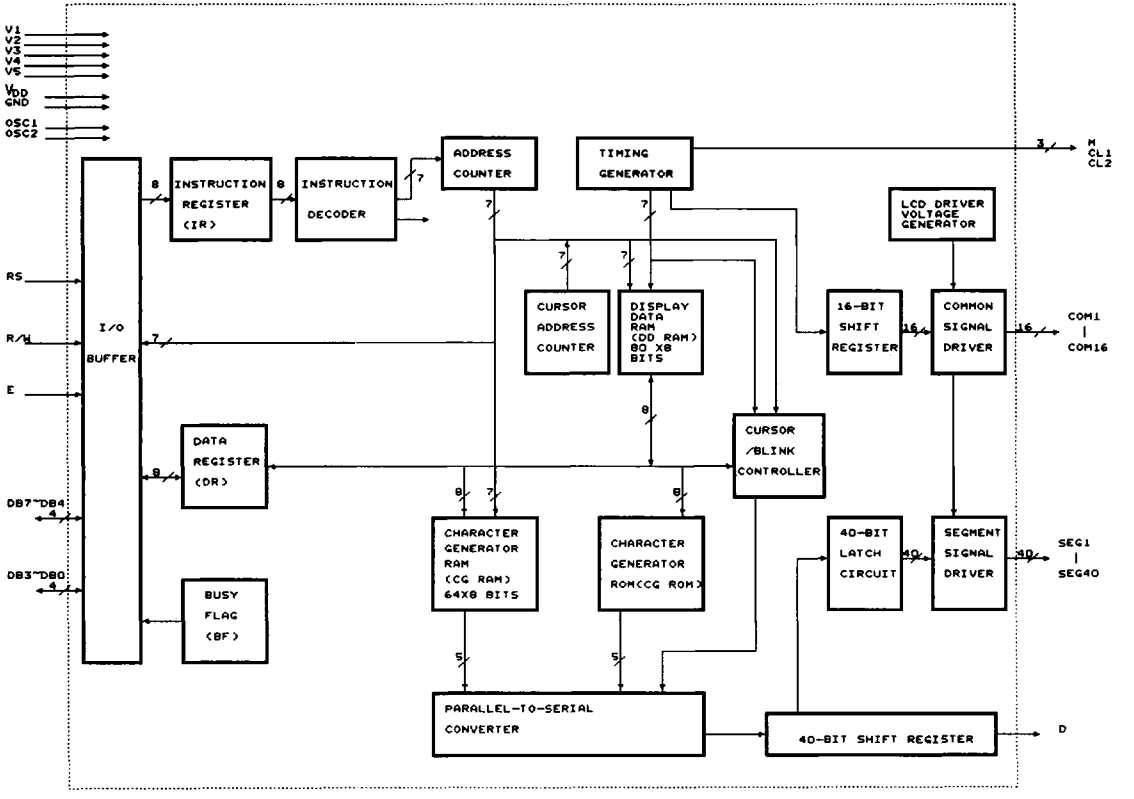
Pin Configuration



Pad Configuration



Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage (V_{DD}) . . . . –0.3V to + 7.0V
Power Supply Voltage (V1 to V5) . . . .
. . . . . V_{DD} –13.5V to V_{DD} + 0.3V
Input Voltage (V_T) . . . . . –0.3V to V_{DD} + 0.3V
Operating Temperature (Topr) . . . . –20°C to + 75°C
Storage Temperature (Tstg) . . . . –55°C to + 125°C

- All voltage values are referenced to GND = 0V
- V1 to V5, must maintain $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5.0V ± 10%, GND = 0V, Ta = –20 to 75°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin
"H" level input voltage (1)	V_{IH1}	2.2	–	V_{DD}	V		DB0 - DB7,
"L" level input voltage (1)	V_{IL1}	–0.3	–	0.8	V		RS, R/W, E
"H" level input voltage (2)	V_{IH2}	V_{DD} – 1.0	–	V_{DD}	V		OSC1
"L" level input voltage (2)	V_{IL2}	GND	–	1.0	V		
"H" level output voltage (1)	V_{OH1}	2.4	–	–	V	IOH = –0.25mA	DB0-DB7
"L" level output voltage (1)	V_{OL1}	–	–	0.4	V	IOL = 1.2mA	(TTL)
"H" level output voltage (2)	V_{OH2}	0.9 V_{DD}	–	–	V	IOH = –0.04mA	CL1, CL2 M, D
"L" level output voltage (2)	V_{OL2}	–	–	0.1V_{DD}	V	IOL = 0.04mA	(CMOS)
Driver voltage descending (COM)	V_{COM}	–	–	2.9	V	Id = 0.05mA	COM1 – 16
Driver voltage descending (SEG)	V_{SEG}	–	–	3.8	V	Id = 0.05mA	SEG1 – 40
Input leakage current	I_{IL}	–1	–	1	µA	VIN = 0 to V_{DD}	
Pull-up MOS current	-IP	50	125	250	µA	V_{DD} = 5V	RS, R/W, DB0-DB7
Supply current Power supply current	I_{OP}	–	0.3	0.5	mA	Rf oscillation, from external clock V_{DD} = 5V, fosc = fcp = 270 KHz	V_{DD}

DC Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin
External clock operation							
External clock operating frequency	fcp	125	270	350	KHz		
External clock duty cycle	Duty	45	50	55	%		
External clock rise time	t_{rcp}	0.1	–	0.5	μs		
External clock fall time	t_{fcp}	0.1	–	0.5	μs		
Internal clock operation (Rf oscillation)							
Oscillation frequency	fosc	190	270	350	KHz	Rf = 91k Ω ± 2%	
Internal clock operation (ceramic filter oscillation)							
Oscillation frequency	fosc	245	250	255	KHz	Ceramic Filter	
LCD driving voltage	V_{LCD1} V_{LCD2}	4.6 3.0	–	V_{DD}	V	V_{DD} - V5 1/5 bias 1/4 bias	

AC Characteristics

■ Read cycle (V_{DD} = 5.0V ± 10%, GND = 0V, Ta = –20 to 75°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Enable cycle time	t_{CYCE}	500	–	–	ns	Fig 1
Enable "H" level pulse width	t_{WEH}	300	–	–	ns	Fig 1
Enable rise/fall time	t_{RE}, t_{FE}	–	–	25	ns	Fig 1
RS, R/W setup time	t_{AS}	60[1] 100[2]	–	–	ns	Fig 1
RS, R/W address hold time	t_{AH}	10	–	–	ns	Fig 1
Read data output delay	t_{RD}	–	–	190	ns	Fig 1
Read data hold time	t_{DHR}	20	–	–	ns	Fig 1

AC Characteristics (continued)

■ Write Cycle (V_{DD} = 5.0V ± 10%, GND = 0V, Ta = -20 to 75°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Enable cycle time	t_{CYCE}	500	–	–	ns	Fig 2
Enable "H" level pulse width	t_{WEH}	300	–	–	ns	Fig 2
Enable rise/fall time	t_{RE}, t_{FE}	–	–	25	ns	Fig 2
RS, R/W setup time	t_{AS}	60[1] / 100[2]	–	–	ns	Fig 2
RS, R/W address hold time	t_{AH}	10	–	–	ns	Fig 2
Data setup time	t_{DS}	100	–	–	ns	Fig 2
Data hold time	t_{DHW}	10	–	–	ns	Fig 2

Notes : 1 : 8-bit operation mode
2 : 4-bit operation mode

Timing Characteristics of Interface Signals with Segment Driver LSI UM3882

(V_{DD} = 5V ± 10%, GND = 0V, T_A = -20 to + 75°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock pulse width high	t_{CWH}	800	–	—	ns	Fig 3
Clock pulse width low	t_{CWL}	800	–	–	ns	Fig 3
Data set-up time	t_{SU}	300	–	–	ns	Fig 3
Data hold time	t_{DH}	300	–	–	ns	Fig 3
Clock set-up time	t_{CSU}	500	–	–	ns	Fig 3
M Delay time	t_{DM}	-1000	–	1000	ns	Fig 3

Power Supply Conditions Using Internal Reset Circuit

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply Rise Time	t_{RON}	0.1	–	10	ns	Fig 4
Power Supply OFF Time	t_{OFF}	1	–	–	ms	Fig 4

Timing Waveforms

Read Operation

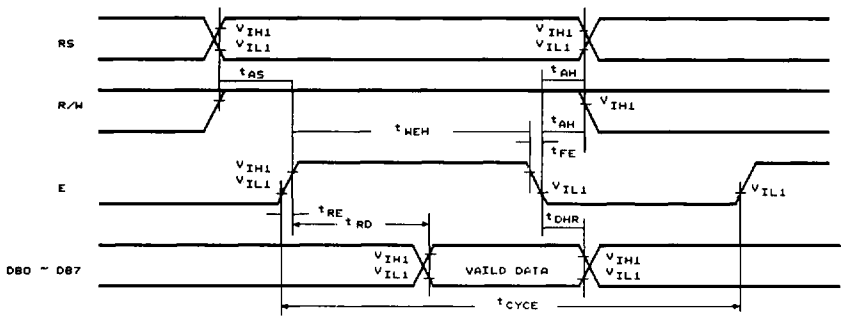


Fig 1: Bus Read Operation Sequence
(Reading out data from UM3881B to MPU)

Write Operation

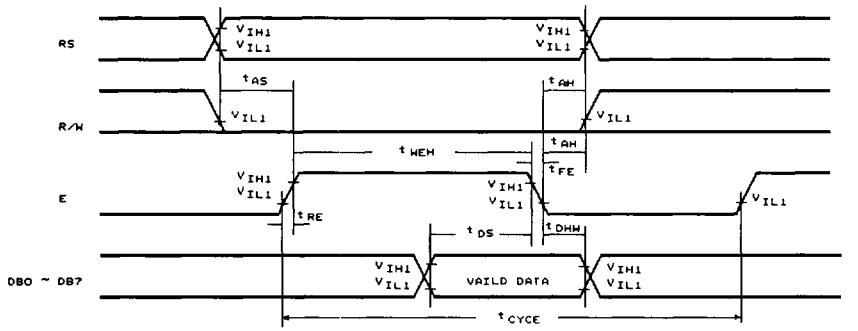


Fig 2: Bus Write Operation Sequence
(Writing data from MPU to UM3881B)

Interface Signals with Segment Driver LSI

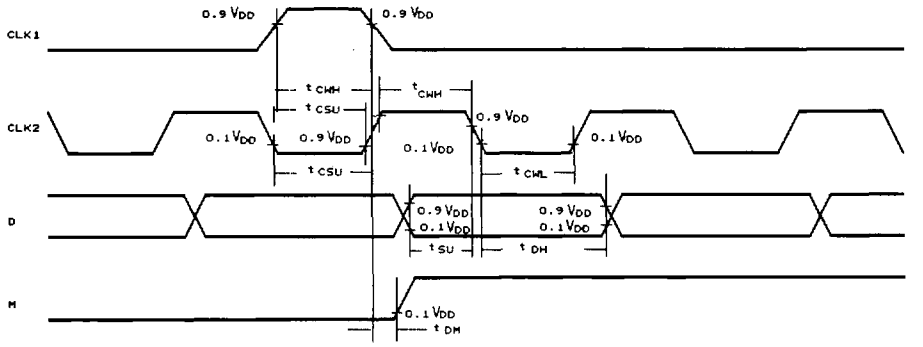


Fig 3: Sending Data to Segment Driver LSI UM3882

Interface Signals with Segment Driver LSI (continued)

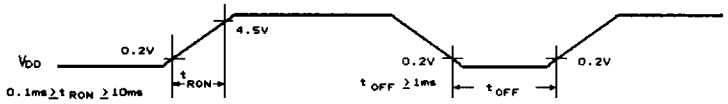


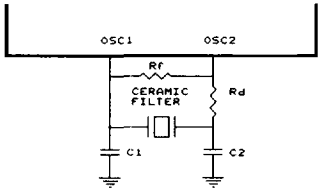
Fig 4 : t_{OFF} stipulates the time of power OFF for instantaneous power supply dip or when power supply repeats ON and OFF.

Pin and Pad Descriptions

Pin and Pad No.	Designation	I/O	External Connection	Description
43 - 46	DB4 - DB7	I/O	MPU	Higher 4 tristate bidirectional data bus for transmitting data between MPU and UM3881B. DB7 is also used as a busy flag
39 - 42	DB0 - DB3	I/O	MPU	Lower 4 tristate bidirectional data bus for transmitting data between MPU and UM3881B. Not used during 4-bit operation
38	E	I	MPU	Start signal for data read/write
36	RS	I	MPU	Register select signal 0: Instruction register (write) Busy flag, address counter (read) 1: Data register (write, read)
37	R/W	I	MPU	Read/Write control signal 0: Write 1: Read
26 - 30	V1 – V5	P	Power supply	Power supply for LCD driver
33, 23	VDD, GND	P	Power supply	VDD: +5V, GND: 0V
47 - 62	COM1 - COM16	O	LCD panel	Common signal output pins
1 - 22	SEG22 - SEG1	O	LCD panel	Segment signal output pins
63 - 80	SEG40 - SEG23			
24, 25	OSC1, OSC2			Pins connected to resistor or ceramic filter for internal clock oscillation. For external clock operation, clock inputs to OSC1
31	CL1	O	UM3882	Clock to latch serial data D sent to UM3882
32	CL2	O	UM3882	Clock to shift serial data D
34	M	O	UM3882	Switch signal to convert LCD drive waveform to AC
35	D	O	UM3882	Character pattern data corresponding to each common signal is transmitted serially from this output. 0-Non selection, 1-selection

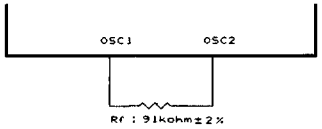
Note 1 : The UM3881B has three clock options

A. Internal Oscillator Operation (With Ceramic Filter).



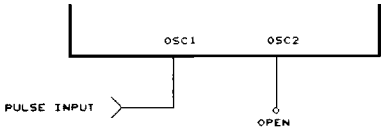
Rf : 1M Ω ± 10%
Rd : 3.3K Ω ± 5%
C1 = C2 : 680pF ± 10%

B. Internal Oscillation (With Rf Resistor).



Only Rf may be connected between OSC1 and OSC2. The wire connecting Rf must be as short as possible.

C. External Clock Operation

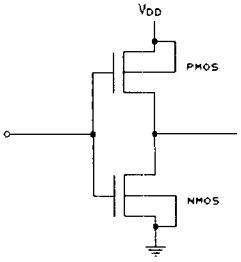


OSC1 and OSC2.

Note 2 : Input/Output Terminals

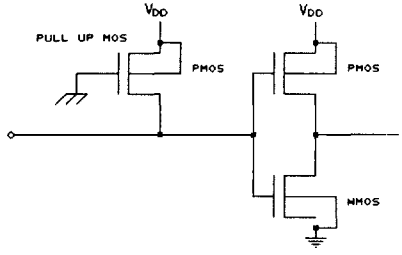
A. Input Terminal

Applicable Terminal : E (No Pull Up MOS)



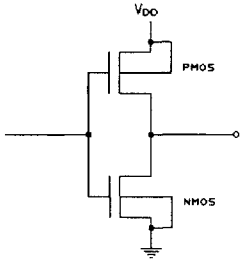
A. Input Terminal

Applicable Terminals: RS, R/W (with Pull Up MOS)



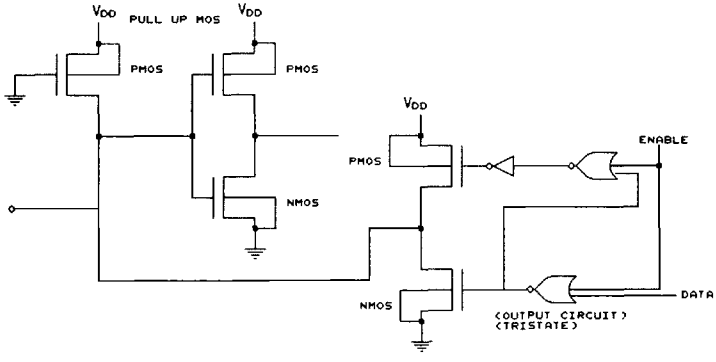
B. Output Terminal

Applicable Terminals: CL1, CL2, M, D



C. I/O Terminal

Applicable Terminals: DB0 to DB7



Functional Description

The UM3881B is a dot-matrix LCD controller and driver LSI. It operates with either a 4-bit or an 8-bit microprocessor (MPU). The UM3881B receives both instructions and data from the MPU. Some instruction set operation modes, such as function mode, data entry mode, and display mode, and some control LCD display functions, such as clear display, restore display, shift display and cursor. Other instructions include read and write both data and addresses. All instructions afford users convenient and powerful functions to control LCD dot-matrix displays.

Data are written into and read from the Data Display RAM (DD RAM) or the Character Generator RAM (CG RAM). As display character codes, those data stored in the DD RAM decode a set of dot-matrix character patterns that are built into the Character Generator ROM (CG ROM). The CG ROM with many character patterns (up to 256 patterns) defines the character pattern fonts. The UM3881B regularly scans the character patterns through the segment drivers. The CG RAM stores character pattern fonts at run time if users intend to show character patterns that are not defined in the CG ROM. This feature makes character display flexible. Other unused bytes can be used as general-purpose data storage.

The LCD driver circuit consists of 16 common signal drivers and 40 segment signal drivers allowing variety of application configurations to be implemented. Furthermore, user can extend display size by cascading segment driver LSI UM3882. The maximum display dimension can be either 80 characters in 1-line display or 40 characters in 2-line display.

Character Generator ROM (CG ROM)

The character generator ROM generates LCD dot character patterns from 8-bit character pattern codes. The UM3881B provides 3 CG ROM configurations:

1. 192 Characters:

The CG ROM contains 160 5x8 dot character patterns and 32 5x10 dot character patterns. An example is the UM3881B-01, in which the relation between character codes and character patterns is shown in Table 1. The character codes from 00H to 0FH are used to get character patterns from the CG RAM. Character codes from 10H to 1FH and from 80H to 9FH map to null character patterns. Character codes from E0H to FFH are assigned to generate 5x10 dot character patterns, and other codes are used to generate 5x8 dot character patterns.

2. 240 Characters:

The CG ROM contains 192 5x8 dot character patterns and 48 5x10 dot character patterns. An example of this type is the UM3881B-02, in which the relation between character codes and character patterns is shown in Table 2.
The character codes from 00H to 0FH are used to get character patterns from the CG RAM. Character codes from 10H to 1FH and from E0H to FFH are assigned to generate 5x10 dot character patterns, and other codes to generate 5x8 dot character patterns. No null character pattern exists in this type. Note that the underlined cursor, displayed on the 8th duty may be obscure if the 8th row of a dot character pattern is coded. We recommend that users display cursor at blinking mode if they code 5x8 dot character patterns in their custom CG ROM.

3. 256 Characters:

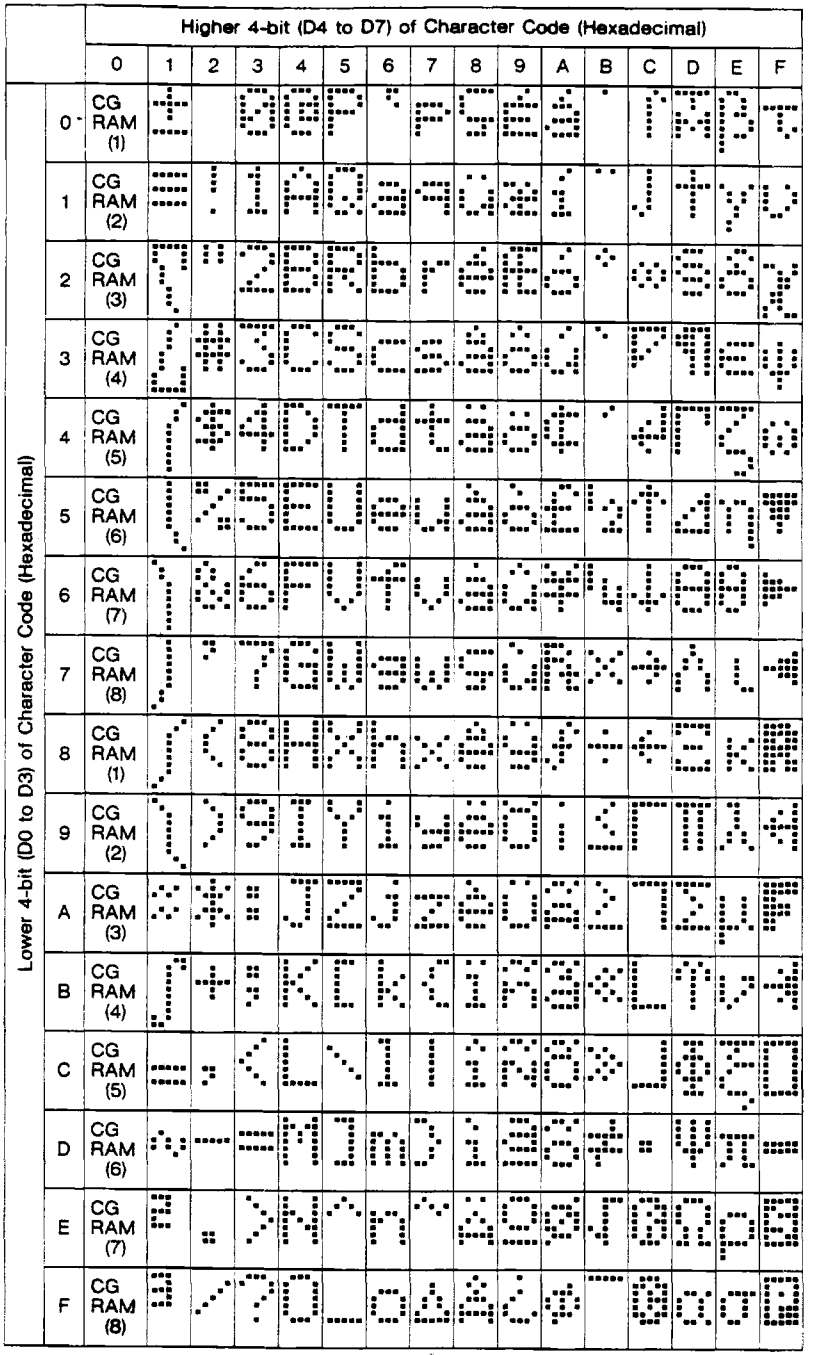
The CG ROM contains 192 5x8 dot character patterns and 64 5x10 dot character patterns. No adequate example is presented here.
The only difference between this type and the second type is that the character codes from 00H to 0FH get character patterns from the CG ROM rather than from the CG RAM. These character codes are assigned to generate 5x10 dot character patterns. In this application, the CG RAM would be employed as a general-purpose data storage.

Custom character patterns, user-defined character patterns, are also available by mask-programming ROM. For convenience of character pattern development, UMC has developed a user-friendly editor program for the UM3881B to help determine the character patterns users prefer. By executing the program at computers, users can easily create and modify their character patterns. By transferring the resulting files generated by the program through modem or other communication path, you and UMC have established a reliable, fast link for programming the CG ROM.

Table 1 : Correspondence between Character Codes and Character Patterns (UMC Standard UM3881B-01)

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

Table 2 : Correspondence between Character Codes and Character Patterns (UMC Standard UM3881B-02)



Instruction Set

Instruction	Code										Function	Execution time (max) (Icp of focs =250KHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	BD1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area,restore display from shift, and load address counter with DD RAM address 00H.	1.64ms
Display/ Cursor Home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00H.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specify direction of cursor movement and display shift mode. This operation takes place after each data transfer (read/write).	40 μs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D) cursor (C) and blinking of character at cursor position (B)	40 μs
Display/ Cursor Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Set interface data length (DL), number of display lines (N), and character font (F).	40 μs
RAM Address Set	0	0	0	1	ACG						Load the address counter with a CG RAM address. Subsequent data access is for CG RAM data.	40 μs
DD RAM Address Set	0	0	1	ADD							Load the address counter with a DD RAM address. Subsequent data access is for DD RAM data.	40 μs
Busy flag/ Address Counter Read	0	1	BF	AC							Read Busy Flag (BF) and contents of Address Counter (AC).	0 μs
CG RAM/ DD RAM Data Write	1	0	Write data								Write data to CG RAM or DD RAM.	40 μs
CG RAM/ DD RAM Data Read	1	1	Read data								Read data from CG RAM or DD RAM.	40 μs
	I/D = 1 : Increment. I/D = 0 : Decrement S = 1 : Display Shift On D = 1 : Display On C = 1 : Cursor Display On B = 1 : Cursor Blink On S/C = 1 : Shift Display. S/C = 0 : Move Cursor R/L = 1 : Shift Right. R/L = 0 : Shift Left DL = 1 : 8-Bit. DL = 0 : 4-Bit N = 1 : Dual Line. N = 0 : Single Line F = 1 : 5x10 dts. F = 0 : 5x8 dots BF = 1 : Internal Operation. BF = 0 : Ready for Instruction											DD RAM : Display Data RAM CG RAM : Character Generator RAM ACG : Character Generator RAM Address ADD : Display Data RAM Address AC : Address Counter	

Note 1 : Symbol "*" signifies a "don't care" bit.
Note 2 : Correct input value for "N" is predetermined for each model.

Interface to LCD

(1) Character Font and Number of Lines

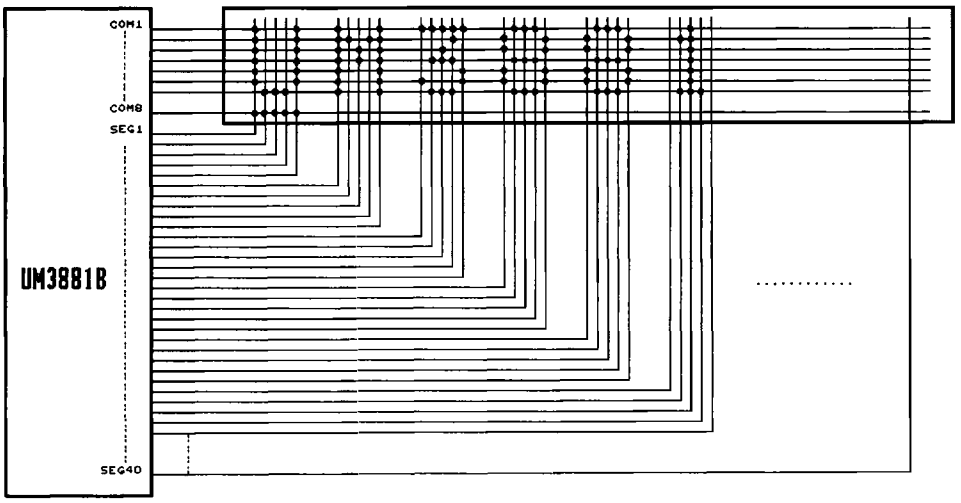
The UM3881B provides 5x7 dot character font 1-line mode, 5x10 dot character font 1-line mode and 5x7 dot character font 2-line mode, as shown in the table below. Three types of common signals are available as displayed in the table. The number of lines and the font type can be selected by program.

Number of Lines	Character font	Number of Common Signals	Duty Factor
1	5x7 dots + Cursor (or 5x8 dots)	8	1/8
1	5x10 dots + Cursor	11	1/11
2	5x7 dots + Cursor (or 5x8 dots)	16	1/16

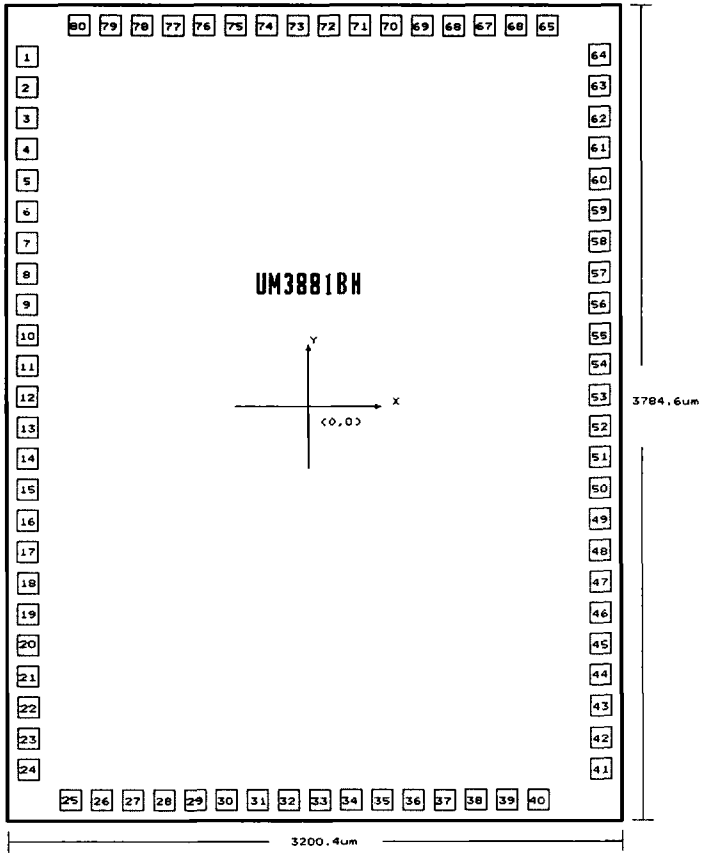
(2) Connection to LCD

— In the case of a 1-line, 8 character display (5x7 dot, 1/4 bias, 1/8 duty), connection to the LCD is shown as follows :

LCD panel (8 characters x1 line)



Bonding Diagram



* Substrate Connect to V_{DD}

Bonding Dimensions

(unit: μm)

No.	Designation	X	Y	No.	Designation	X	Y
1	SEG22	-1444	1725	41	DB2	1444	-1725
2	SEG21	-1444	1575	42	DB3	1444	-1575
3	SEG20	-1444	1425	43	DB4	1444	-1425
4	SEG19	-1444	1275	44	DB5	1444	-1275
5	SEG18	-1444	1125	45	DB6	1444	-1125
6	SEG17	-1444	975	46	DB7	1444	-975
7	SEG16	-1444	825	47	COM1	1444	-825
8	SEG15	-1444	675	48	COM2	1444	-675
9	SEG14	-1444	525	49	COM3	1444	-525
10	SEG13	-1444	375	50	COM4	1444	-375
11	SEG12	-1444	225	51	COM5	1444	-225
12	SEG11	-1444	75	52	COM6	1444	-75
13	SEG10	-1444	-75	53	COM7	1444	75
14	SEG09	-1444	-225	54	COM8	1444	225
15	SEG08	-1444	-375	55	COM9	1444	375
16	SEG07	-1444	-525	56	COM10	1444	525
17	SEG06	-1444	-675	57	COM11	1444	675
18	SEG05	-1444	-825	58	COM12	1444	825
19	SEG04	-1444	-975	59	COM13	1444	975
20	SEG03	-1444	-1125	60	COM14	1444	1125
21	SEG02	-1444	-1275	61	COM15	1444	1275
22	SEG01	-1444	-1425	62	COM16	1444	1425
23	GND	-1444	-1575	63	SEG40	1444	1575
24	OSC1	-1444	-1725	64	SEG39	1444	1725
25	OSC2	-1140	-1740	65	SEG38	1125	1740
26	V1	- 969	-1740	66	SEG37	975	1740
27	V2	- 818.3	-1740	67	SEG36	825	1740
28	V3	- 668.3	-1740	68	SEG35	675	1740
29	V4	- 518.3	-1740	69	SEG34	525	1740
30	V5	- 368.3	-1740	70	SEG33	375	1740
31	CL1	- 218.3	-1740	71	SEG32	225	1740
32	CL2	-68.3	-1740	72	SEG31	75	1740
33	V_{DD}	81.7	-1740	73	SEG30	-75	1740
34	M	231.7	-1740	74	SEG29	-225	1740
35	D	381.7	-1740	75	SEG28	-375	1740
36	RS	535.3	-1740	76	SEG27	-525	1740
37	R/W	689.1	-1740	77	SEG26	-675	1740
38	E	839.1	-1740	78	SEG25	-825	1740
39	DB0	994.8	-1740	79	SEG24	-975	1740
40	DB1	1144.8	-1740	80	SEG23	-1125	1740

Ordering Information

Part No.	Package	Remarks
UM3881BH-01	CHIP FORM	Ref. TABLE 1
UM3881BF-01	80L QFP	Ref. TABLE 1
UM3881BH-02	CHIP FORM	Ref. TABLE 2
UM3881BF-02	80L QFP	Ref. TABLE 2