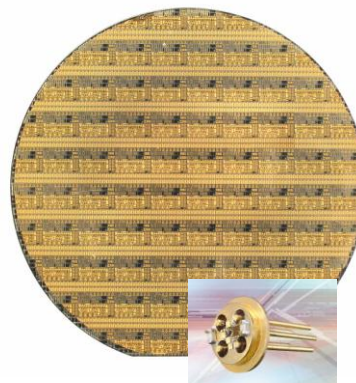


IN4701

11.3 Gbps TIA / LIA

Data Sheet



Applications

- TO-can receivers
- SONET OC-192 and SDH STM-64 transponders
- Short, intermediate, long reach, and long haul optical receiver modules
- 10 Gbps Ethernet
- Broadband instrumentation

Features

- Supports data rates up to 11.3 Gbps
- Input sensitivity: -20 dBm
- Input overload $+2$ dBm
- Fast rise and fall times: 15 ps
- Low power consumption: 105 mW
- Through-wafer vias on ground pads
- Adjustable DC offset control
- Single $+3.3$ V power supply
- Available in die form
- Small die size: $880 \mu\text{m} \times 1100 \mu\text{m}$

Description

The IN4701 transimpedance amplifier / limiting amplifier (TIA/LIA) is designed to support data rates up to 11.3 Gbps. It maintains an open eye with little duty cycle distortion for inputs up to $+2$ dBm. The IN4701 exhibits a typical input sensitivity of -20 dBm while maintaining a BER of 10^{-12} (assuming PD $\rho = 0.9$ A/W, data pattern is $2^{31}-1$ PRBS at 11.3 Gbps).

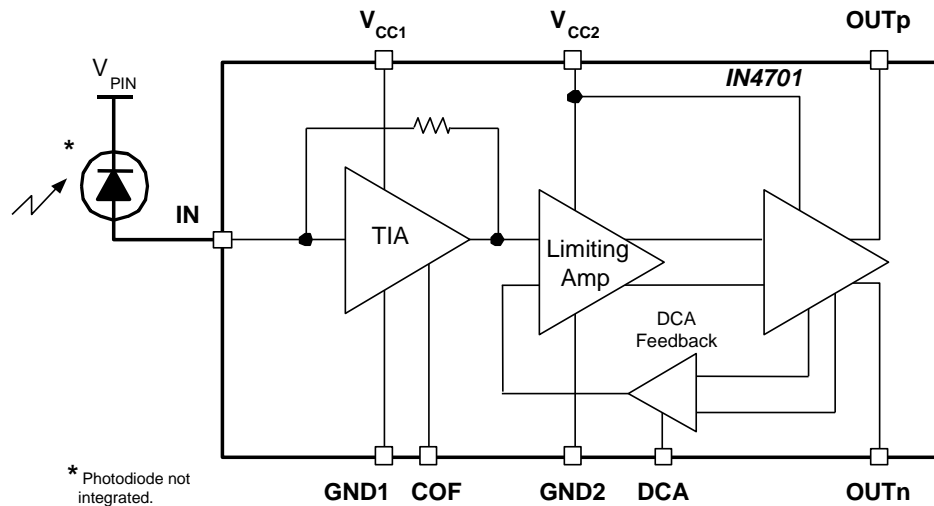
With $12 \text{ k}\Omega$ of differential gain, the IN4701 eliminates the need for a stand-alone limiting amplifier to amplify signals from the TIA. The saturated output amplitude of the TIA/LIA is typically $450 \text{ mV}_{\text{pp}}$ differential. This part includes an integrated feedback circuit to control the decision threshold of the limiting amplifier, maintaining 50% eye crossing. In addition, the

eye crossing can be externally adjusted through an offset pin, DCA.

To facilitate TO-can assembly, the IN4701 is small ($880 \mu\text{m} \times 1100 \mu\text{m}$), with output pads on opposite sides of the die. Also, the backside of the TIA is grounded using through-wafer vias so that ground bonds are not required.

The IN4701 has fast rise and fall times and low power consumption. The TIA/LIA operates from a single $+3.3$ V power supply and is available in die form. Evaluation kits are available.

Block Diagram



Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the “Operating Conditions” and “Electrical Specifications” of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameter | Symbol | Conditions | Min | Max | Unit |
|-----------------------------------|--------------------|--|------|------|------------------|
| Power Supply Voltage | V_{CC1}, V_{CC2} | $T_C = 25\text{ }^\circ\text{C}$ 6 seconds stress time | -0.5 | 4.0 | V |
| | | $-40\text{ }^\circ\text{C} < T_C < 90\text{ }^\circ\text{C}$ 6 seconds stress time | -0.5 | 3.8 | V |
| | | $-40\text{ }^\circ\text{C} < T_C < 90\text{ }^\circ\text{C}$ 1000 hours stress time | -0.5 | 3.7 | V |
| Continuous Input Current | I_{IN} | 5 minute stress time | -1.5 | 10 | mA |
| DCA Voltage ¹ | V_{DCA} | | 0 | 4 | V |
| Junction Temperature | T_J | | --- | +175 | $^\circ\text{C}$ |
| Shipping/Storage Temperature | T_{STORE} | | --- | +125 | $^\circ\text{C}$ |
| ESD protection (HBM) ² | V_{ESD} | V_{CC1pad} | 500 | --- | V |
| | | V_{CC2pad} | 400 | --- | V |
| | | Output pads | 200 | --- | V |
| | | Input pad | 200 | --- | V |
| | | COF pad | 150 | --- | V |
| | | DCA pad | 200 | --- | V |

Notes:

¹ DCA voltage must be $< V_{CC} + 0.5\text{ V}$ at all times during power up/down

² As per JESD22-A114-B

Operating Conditions

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------------------------|--------------------|--|--------|--------|--------|--------------------|
| Power Supply Voltage | V_{CC1}, V_{CC2} | $-20\text{ }^{\circ}\text{C} \leq T_C \leq 95\text{ }^{\circ}\text{C}$ | +2.970 | +3.300 | +3.530 | V |
| | | $-40\text{ }^{\circ}\text{C} \leq T_C \leq 95\text{ }^{\circ}\text{C}$ | +3.135 | +3.300 | +3.465 | V |
| Supply Current | I_{CC} | | --- | 32 | 50 | mA |
| On-Chip Power Dissipation | P_D | | 85 | 105 | 176 | mW |
| DCA Input Current ¹ | I_{DCA} | | -30 | --- | 30 | μA |
| DCA Input Voltage ¹ | V_{DCA} | | 2.5 | --- | 3.5 | V |
| Operating Temperature (Die backside) | T_C | $+2.970\text{ V} \leq V_{CC1}, V_{CC2} \leq +3.530\text{ V}$ | -20 | --- | +95 | $^{\circ}\text{C}$ |
| | | $+3.135\text{ V} \leq V_{CC1}, V_{CC2} \leq +3.465\text{ V}$ | -40 | --- | +95 | $^{\circ}\text{C}$ |

Note:

¹ These are the minimum and maximum inputs to DCA required to adjust V_{OS} over its full range. DCA is normally self-adjusting. **Only** apply I_{DCA} or V_{DCA} if different eye crossing is required. Current control (I_{DCA}) is recommended.

Electrical Specifications



WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications are guaranteed when the part is operated within either of the two specified sets of Operating Conditions: Normal or extended V_{CC} range.
Electrical specifications are based on *Photodiode Specification Assumptions* on page 5, and ER = 10 dB.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------------|--|------|----------|----------|------------|
| Maximum Data Rate | | 10 ⁻¹² BER (NRZ format) | 11.3 | --- | --- | Gbps |
| Input Sensitivity ¹ | | @ 11.3 Gbps ($\rho = 0.9$ A/W, ER = 10 dB) | --- | -20 | -18 | dBm |
| Input Overload ¹ | | @ 11.3 Gbps ($\rho = 0.9$ A/W, ER = 10 dB) | +2 | --- | --- | dBm |
| Stressed Receiver Sensitivity (OMA) | | 10GBASE-LR | --- | -15.5 | --- | dBm |
| Input Current | I_{IN} | Input signal 50% crossing | 0.02 | | 2.5 | mApp |
| Small Signal Transimpedance, differential peak-to-peak | Z_T | $f = 1$ GHz | 8 | 12 | 16 | k Ω |
| Output Amplitude, differential peak-to-peak (Limited) ² | $V_{OUTp} - V_{OUTn}$ | | 300 | 450 | 680 | mVpp |
| Small Signal Z_T BW (3 dB) | BW | 50 Ω environment | 8 | 9 | 12.5 | GHz |
| Low Frequency Cut-off | f_{Low} | Pin = -20 dBm | --- | 40 | 100 | kHz |
| Rise/Fall Time | t_r/t_f | 20–80%, for $I_{IN} > 0.4$ mApp | 10 | 15 | 25 | ps |
| Added Peak-to-Peak Deterministic Jitter | J_D | | --- | --- | 10 | ps |
| Random Jitter | J_R | $I_{IN} > 0.2$ mApp | --- | 0.4 | 1.0 | ps RMS |
| Output Return Loss | RL_{OUT} | $f < 10$ GHz, 50 Ω environment. | 8 | --- | --- | dB |
| Output Ripple | r_{OUT} | 50 Ω environment | -0.5 | --- | 0.5 | dB |
| Peaking | | 50 Ω environment | --- | 1 | 1.5 | dB |
| Z_T Group Delay Variation | | 100 MHz – 8 GHz, 50- Ω environment | --- | ± 14 | ± 28 | ps |
| Open-circuit Input DC Level | V_{IN} | Generated on chip | 1.18 | 1.35 | 1.52 | V |
| Open-circuit DCA Voltage ³ | V_{DCAOC} | Typical operating conditions | --- | 3.0 | --- | V |

Notes:

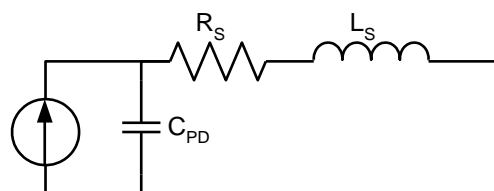
¹ Sensitivity and overload depend on photodiode, packaging, BERT sensitivity, input eye quality and optical coupling.

² Output fully limited for inputs greater than 0.1 mApp.

³ Open-circuit, DCA voltage is dependent on power supply level, temperature, and average input current.

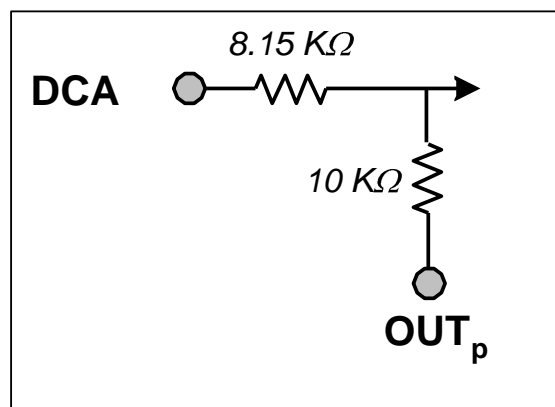
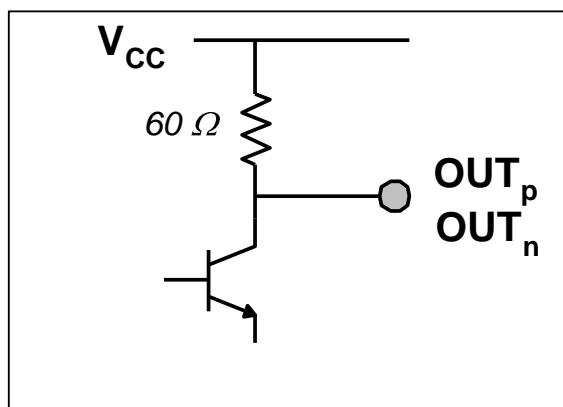
Photodiode Specification Assumptions

| Parameter | Symbol | Typ |
|-------------------------------------|----------|-------------|
| Photodiode Capacitance | C_{PD} | 0.20 pF |
| Photodiode Resistance | R_S | 20 Ω |
| Photodiode and Bond wire Inductance | L_S | 600 pH |
| Photodiode Responsivity | ρ | 0.9 A/W |



Photodiode electrical model

I/O Equivalent Circuits



Optical Receiver and Stressed Receiver Sensitivity

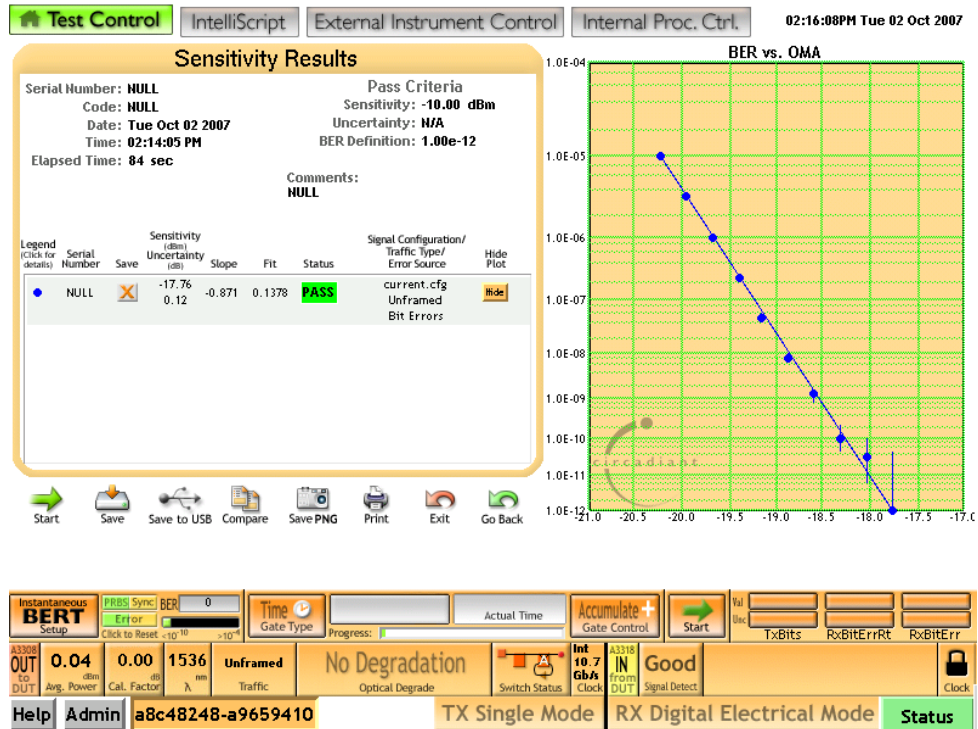


Figure 1. Receiver sensitivity, -17.8 dBm (OMA) @ 10.7 Gbps

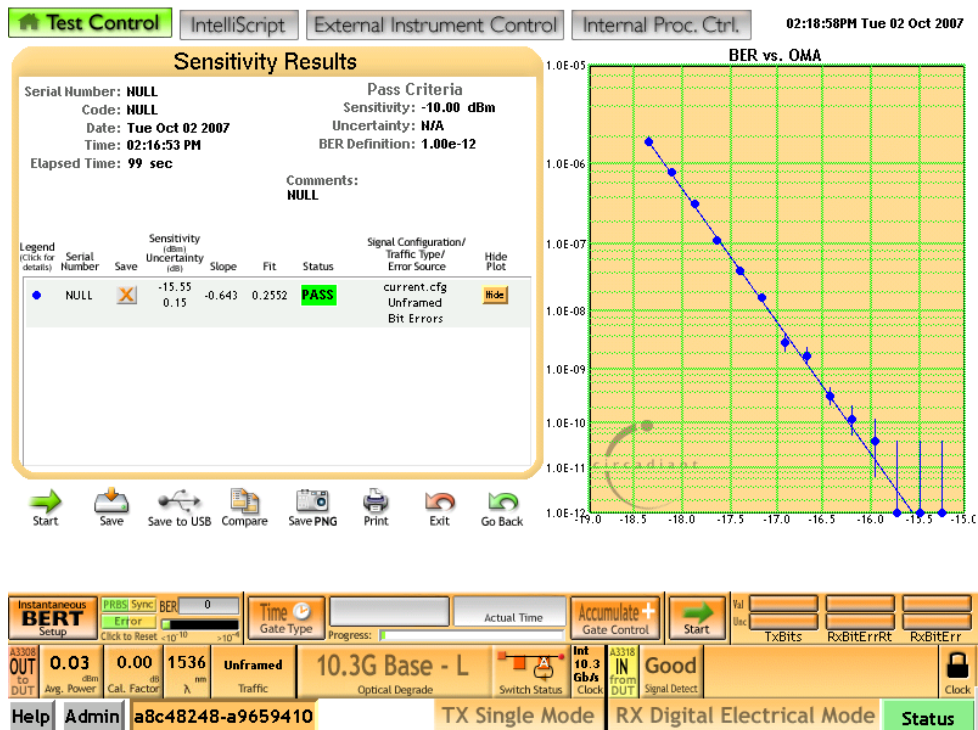


Figure 2. Stressed receiver sensitivity, 10GBASE-LR, -15.5 dBm (OMA) @ 10.7 Gbps

Optical Receiver and Stressed Receiver Sensitivity (cont'd.)

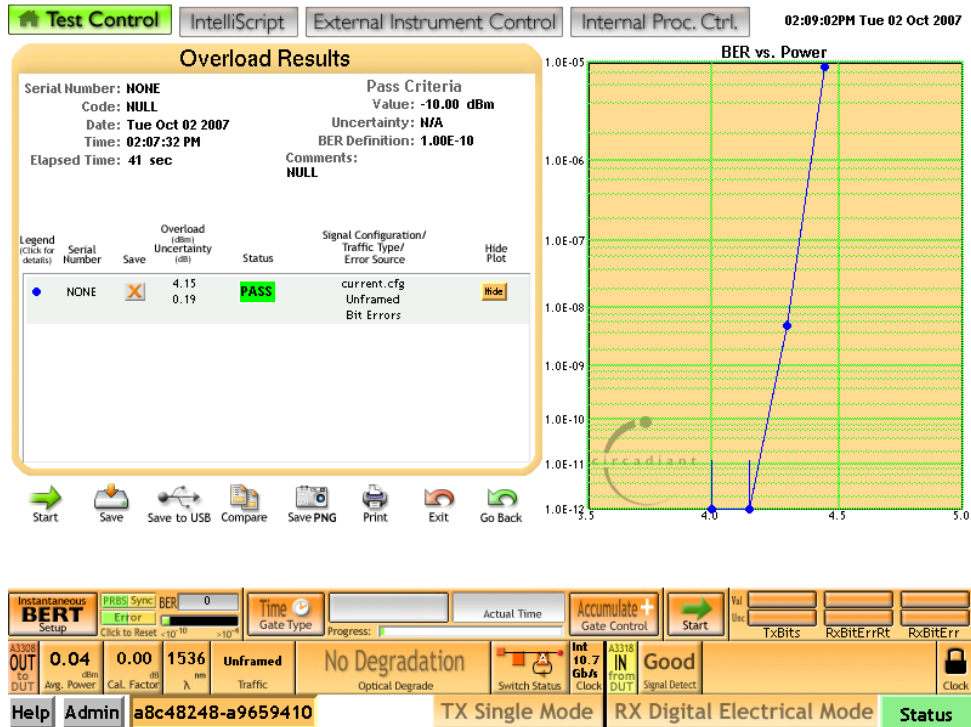


Figure 3. Receiver overload, 4.1 dBm (average) @ 10.7 Gbps

Time Domain Operating Characteristics

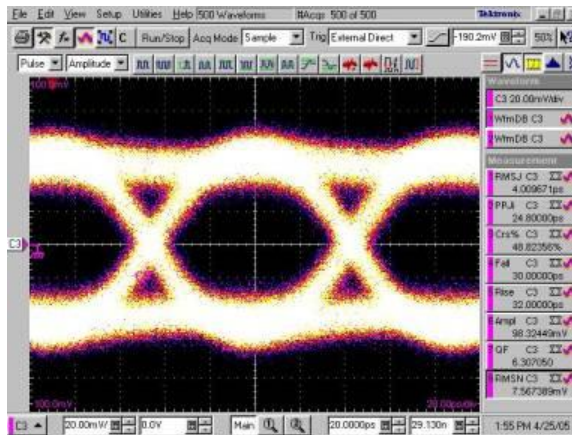


Figure 4. Output eye measured in TO-can ROSA with -20 dBm input power (+3.3 V, 25 °C, 2^{31} -1 pattern).
Note: input optical source peak-to-peak jitter was 20 ps.

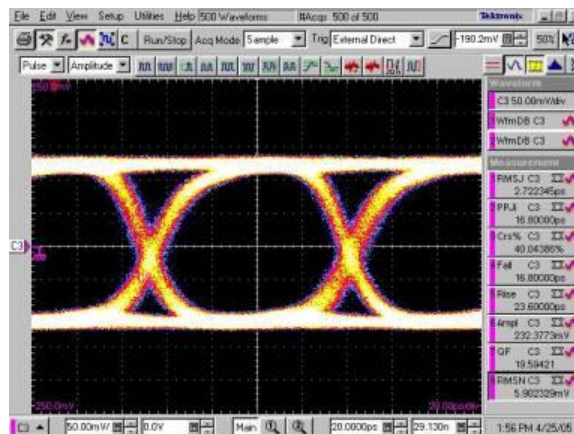


Figure 5. Output eye measured in TO-can ROSA with -10 dBm input power (+3.3 V, 25 °C, 2^{31} -1 pattern).
Note: input optical source peak-to-peak jitter was 20 ps.

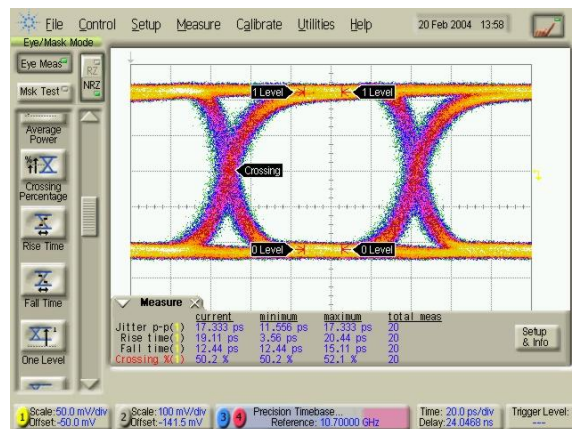


Figure 6. Output eye measured on wafer with 2.5 mApp input current (+3.3 V, 25 °C, 2^{31} -1 pattern).
Note: input optical source peak-to-peak jitter was 20 ps.

Frequency Domain Operating Characteristics

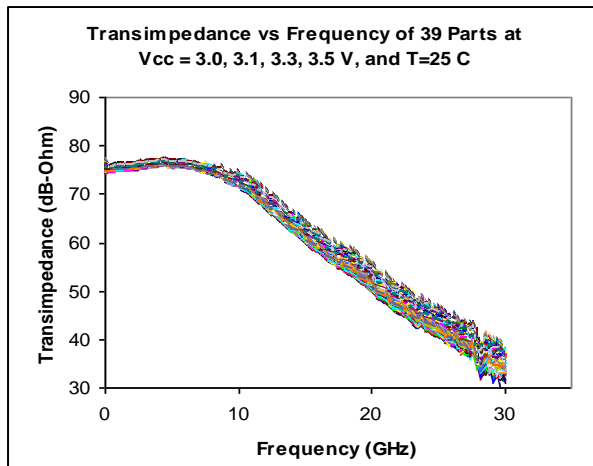


Figure 7. Transimpedance (dB-ohms) vs. frequency with supply as parameter ($T = 25\text{ }^{\circ}\text{C}$). Taken from wafer probe measurements.

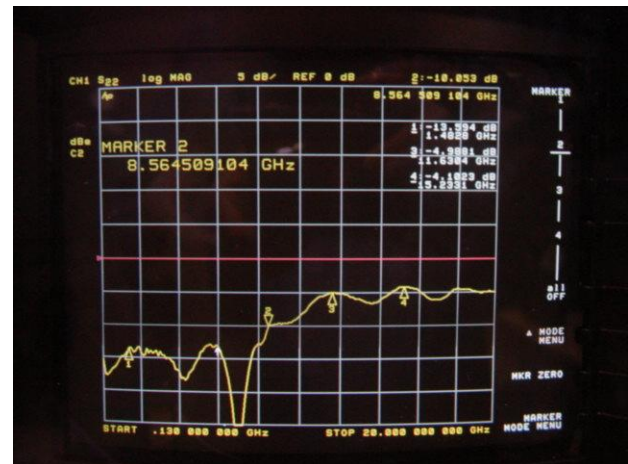


Figure 8. Typical single-ended output return loss (dB) versus frequency. The base line is 0 dB and the vertical scale is 5 dB/div. Tested on a TO-can at 3.3 V & $25\text{ }^{\circ}\text{C}$. See Figure 23 for assembly drawing.

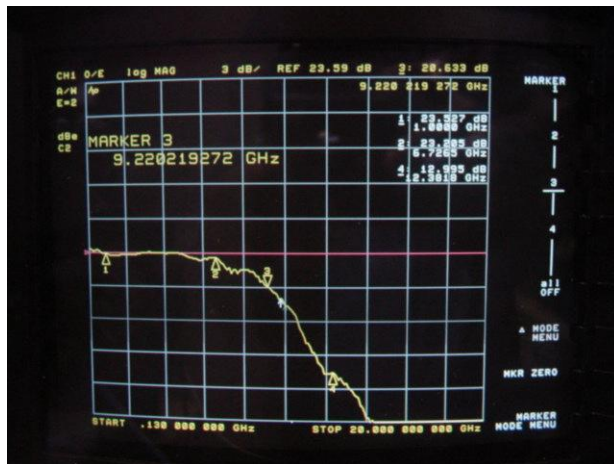


Figure 9. Typical single-ended transimpedance (dB-ohms) versus frequency. The base line is the low frequency (flat) response level and the vertical scale is 3 dB-ohms/div. Tested on a TO-can at 3.3 V & $25\text{ }^{\circ}\text{C}$. See Figure 23 for assembly drawing.

| 3 dB Bandwidth | | | |
|----------------|-------|-------|-------|
| Temp \ Vcc | 3.1 V | 3.3 V | 3.5 V |
| -40 C | 10.2 | 10.7 | 11.1 |
| -10 C | 10.1 | 10.5 | 10.8 |
| 25 C | 10.0 | 10.3 | 10.6 |
| 95 C | 9.7 | 10.0 | 10.2 |

Table 1. 3 dB transimpedance bandwidth as a function of operating conditions. From electrical-to-electrical S-parameter measurements in a $50\ \Omega$ environment.

DC Operating Characteristics

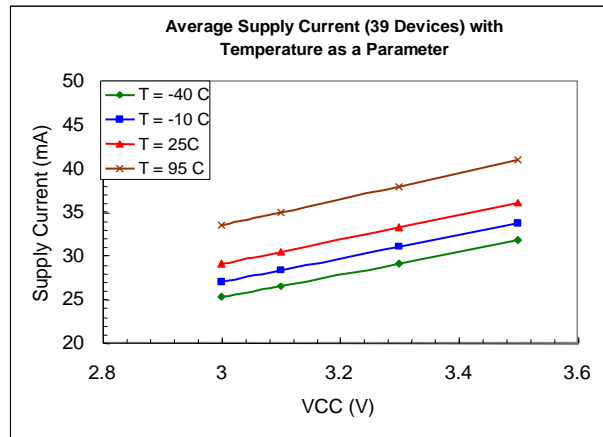


Figure 10. Power supply current ($I_{VCC1}+I_{VCC2}$) versus supply voltage with temperature as a parameter.

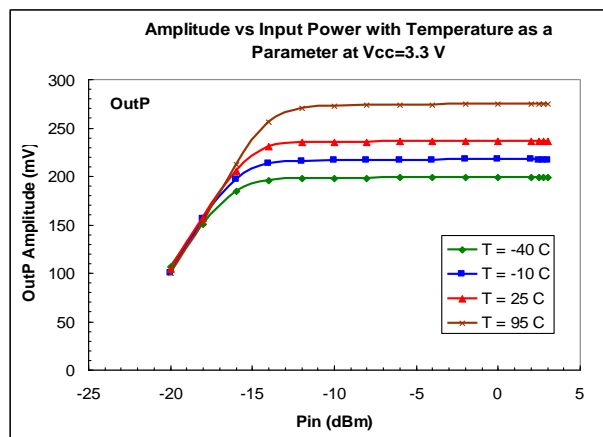


Figure 11. Single-ended output amplitude vs. input power with temperature as parameter ($V_{cc} = 3.3$ V)

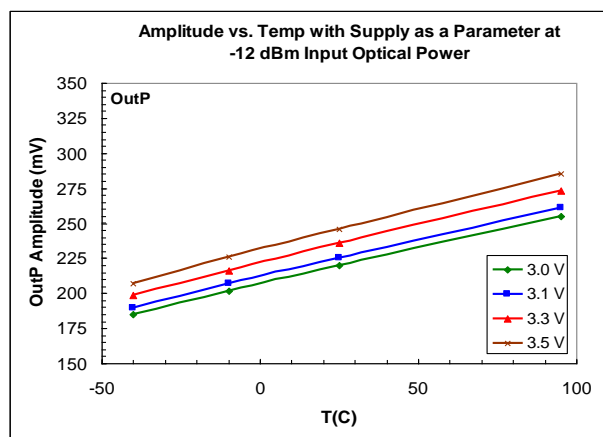


Figure 12. Differential output amplitude vs. temperature with supply as parameter.

Time Domain Operating Characteristics

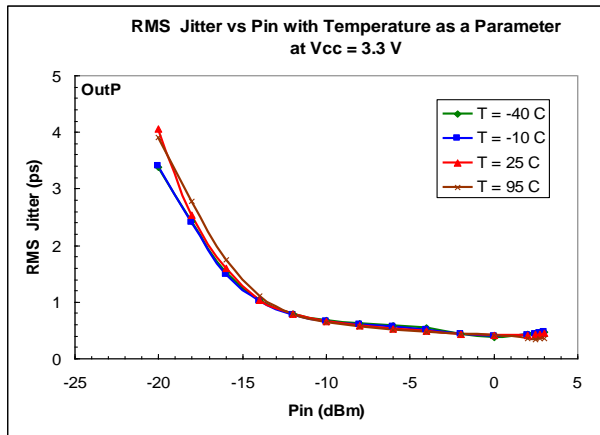


Figure 13. RMS Jitter (not de-embedded) versus input power with temperature as parameter ($V_{CC} = 3.3\text{ V}$).

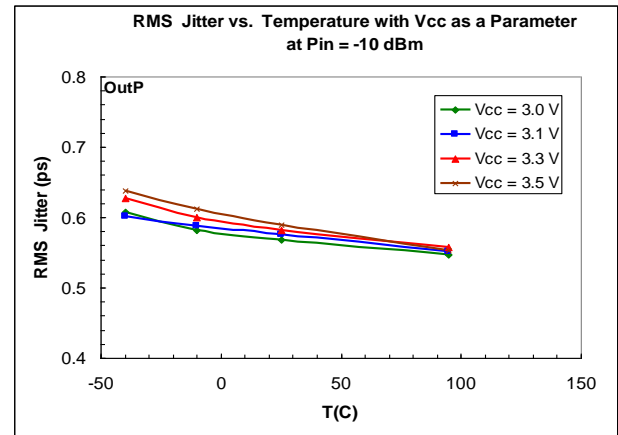


Figure 14. RMS jitter (not de-embedded) vs. temperature with V_{CC} as parameter ($I_{in} = 164\ \mu\text{App}$).

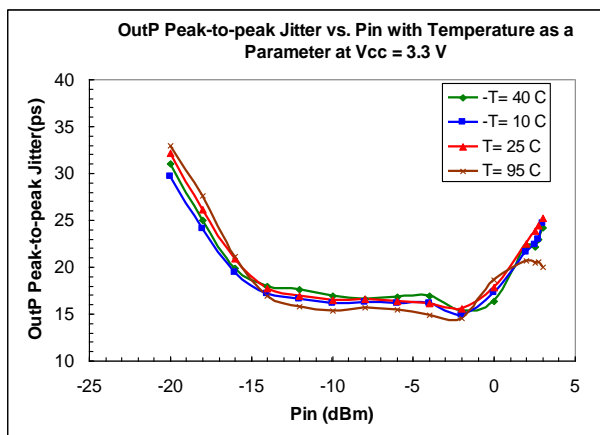


Figure 15. Peak-to-peak jitter (source jitter not de-embedded) vs. input power with temperature as a parameter ($V_{CC} = 3.3\text{ V}$).

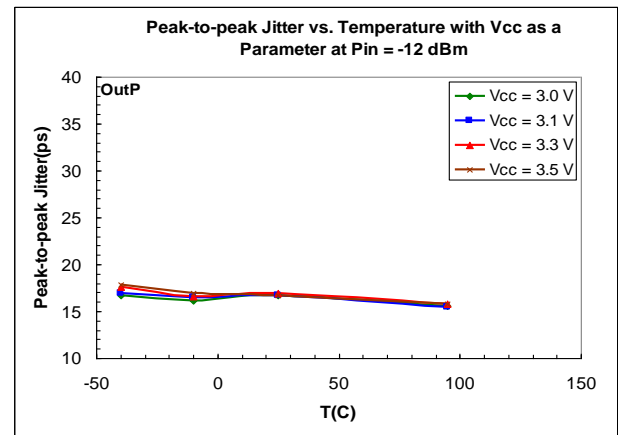


Figure 16. Peak-to-peak jitter (not de-embedded) vs. temperature with V_{CC} as parameter ($I_{in} = 100\ \mu\text{App}$).

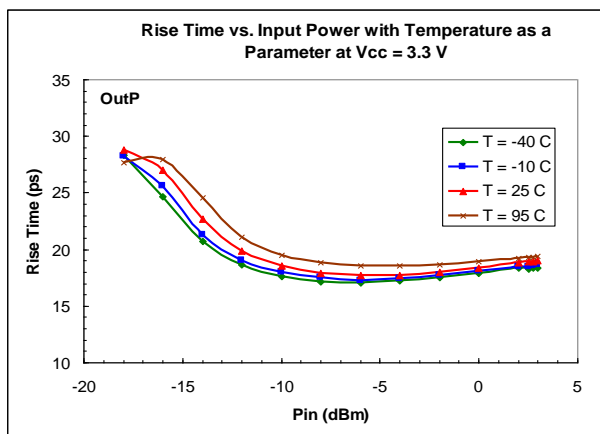


Figure 17. Rise time vs. input power with temperature as a parameter ($V_{CC} = 3.3\text{ V}$).

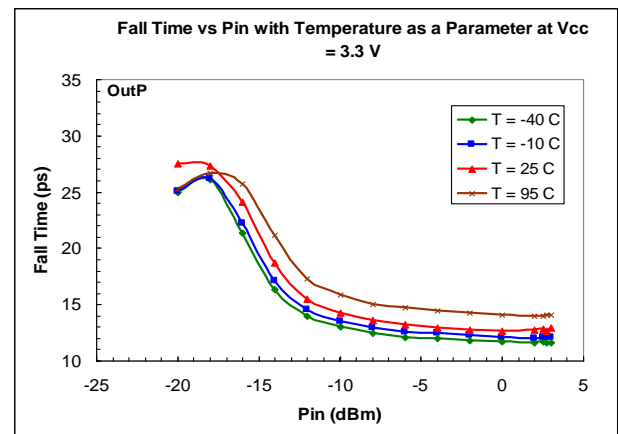


Figure 18. Fall time vs. input power with temperature as a parameter ($V_{CC} = 3.3\text{ V}$).

Time Domain Operating Characteristics

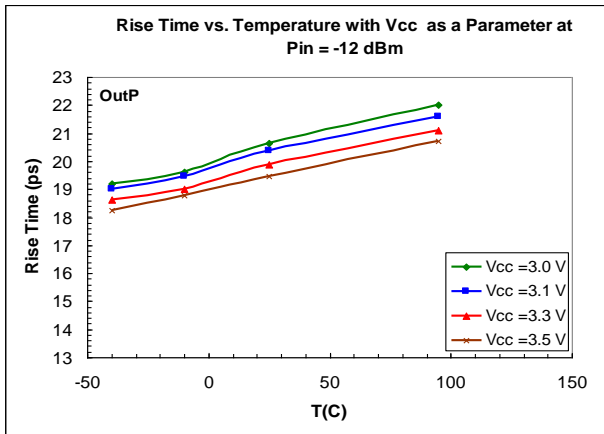


Figure 19. Rise time vs. temperature with Vcc as parameter (Pin = -12 dBm).

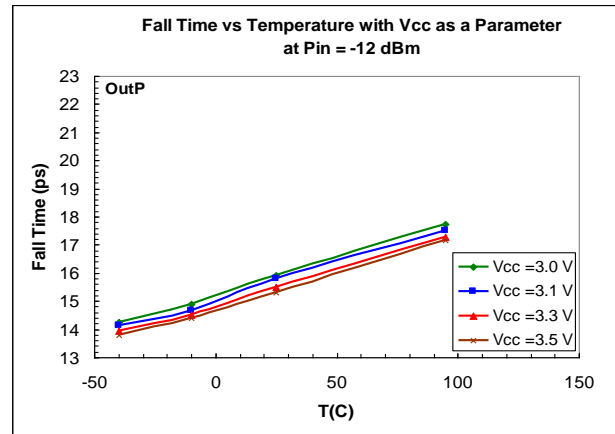


Figure 20. Fall time vs. temperature with Vcc as parameter (Pin = -12 dBm).

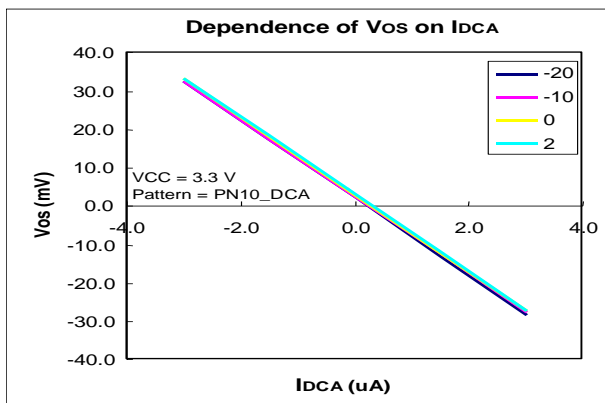


Figure 21. Output DC offset voltage vs. DCA current with input power (dBm optical, ER = 16 dB) as parameter, at T = 25 °C and VCC = 3.3 V.

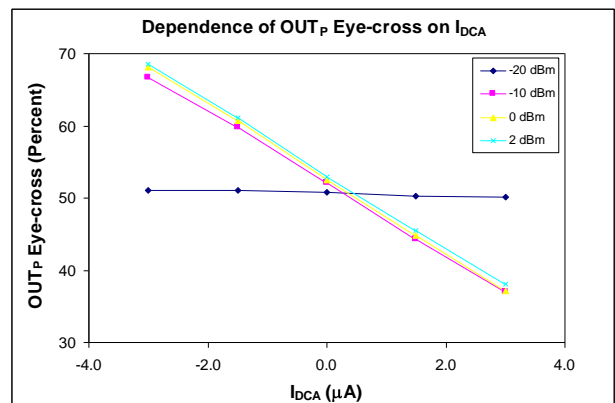


Figure 22. Output eye-cross vs. DCA current with input power (dBm optical, ER = 16 dB) as parameter, at T = 25 °C and VCC = 3.3 V.

Eye-Cross Level Adjustment

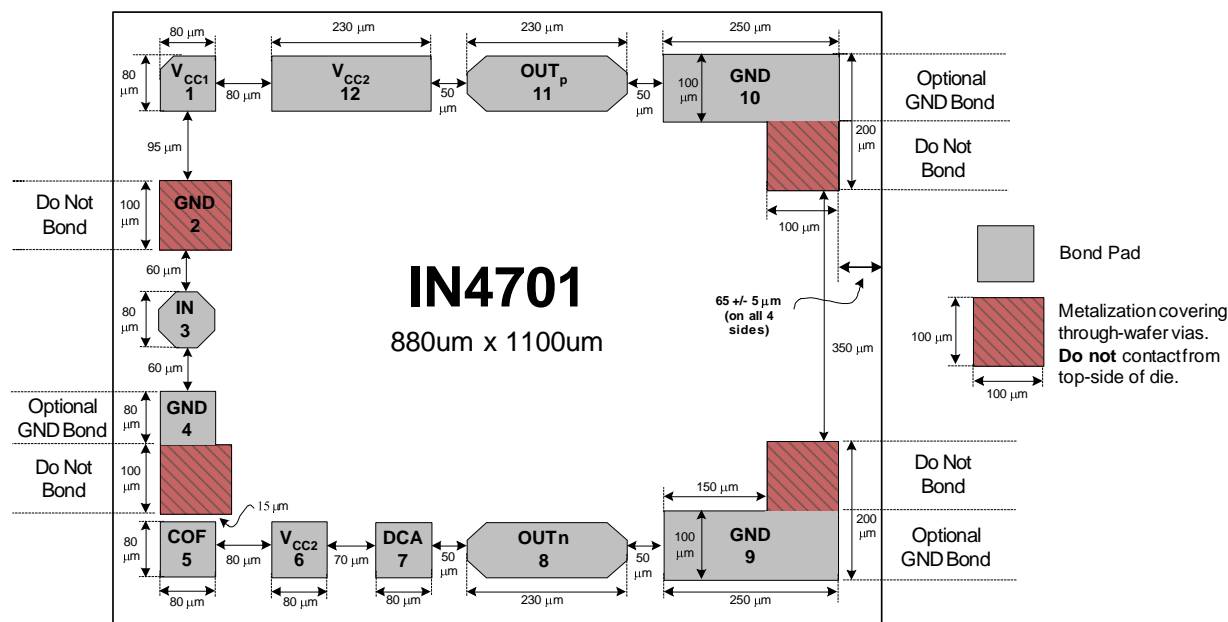
The IN4701 incorporates an internal feedback circuit to maintain zero differential output DC offset voltage, called V_{OS} . This voltage is the average over time of $(V_{OUTP} - V_{OUTA})$. The averaging time constant is internally fixed. This time constant also determines the low frequency cut-off, f_{LOW} (100 kHz maximum). The relationship between V_{OS} and the output eye-cross level depends on the signal amplitude. For moderate to high input signal level, where the output is saturated everywhere except during transitions, a zero value for V_{OS} maintains an eye-cross level close to 50%. For low signal level where the IN4701 is operating in linear mode, the output eye-cross level is the same as the input eye-cross level. To use the internal feedback circuit, the DCA pad should be left floating (not connected).

If an eye-cross level different from 50% is required, the DCA pad can be driven by an external source. There are two basic approaches to adjusting the eye-cross level. The first is to override the internal feedback control loop by adding an external feedback control loop that drives the DCA pad. Contact Inphi for an application note that includes an operational amplifier circuit implementing this approach.

The second approach to adjusting the eye-cross level is a feed-forward or set-and-forget eye-cross adjustment. In this case the DCA pad can be driven by a current source to change the eye-cross level. The equivalent circuit, looking into the DCA pad, is in the I/O Equivalent Circuits section above. The impedance is about 18 k Ω and the nominal open-circuit voltage is 3.0 volts. The DCA pad should be driven by a current source (not a voltage source) because the open-circuit DCA voltage varies over operating conditions. The relationship between V_{OS} and DCA input current is shown in Figure 21. The change in average differential output voltage is 10 k Ω times the DCA input current. Examples of the dependency of eye-cross level on DCA current are shown in Figure 22. For low input signal level, where the IN4701 output is not saturating, the eye pattern is just an amplified version of the input eye pattern, and eye-cross level does not change with DCA input current.

Note: The low frequency cut-off of the IN4701 is set internally. Adding capacitance to the DCA node does not affect the low frequency cut-off of the IN4701.

Die Pad Layout



Notes:

- ¹ Die size: 880 μm x 1100 μm nominal
- ² Pad frame border: $65 \pm 5 \mu\text{m}$
- ³ Die thickness: $110 \pm 10 \mu\text{m}$

- ⁴ Backside of die is metalized.
- ⁵ Metallization covering through-wafer vias cannot be contacted from top-side of die.

| Name | Pad | Description | Function |
|------------------|-------------|---|--------------|
| IN | 3 | Data Input from Photodiode | Input |
| OUT _p | 11 | Data Output positive (non-inverting): Back terminated with 60 Ω to V_{CC2} | Output |
| OUT _n | 8 | Data Output negative (inverting): Back terminated with 60 Ω to V_{CC2} | Output |
| DCA | 7 | DC Adjust: Typically not connected. Used for external DC slice-level adjust. Adding capacitance to DCA does not affect the low frequency cut-off of the IN4701. | Analog Input |
| V_{CC1} | 1 | Analog power supply. Connect to +3.3 V. Bypass to ground. | Supply |
| V_{CC2} | 6, 12 | Digital power supply. Connect pad 12 to +3.3 V and bypass to GND. Depending on user's ROSA assembly configuration, performance may be enhanced by bypassing pad 6 to GND as well. (See assembly drawing and application note.) | Supply |
| COF | 5 | To prevent an increase in the low frequency cut-off as average input power increases with a very low extinction ratio, bypass pad 5 with a 1nF capacitor to GND (See assembly drawing and application note.) | Analog Input |
| GND | 2, 4, 9, 10 | Important: Optional GND Bond. Users may wire bond to the GND portion only of these pads available as shown above. Do Not Bond to the indicated areas of these pads, as they are connected to the back of the die with through-wafer vias. The back of the die must be connected to electrical ground using conductive epoxy or eutectic die attach. | Supply |

Suggested Assembly

Because the IN4701 has high gain and bandwidth, it is important to provide good supply bypassing and to keep bond wire lengths as short as possible when assembling it in a TO-can ROSA. The recommended assembly for the IN4701 in a TO-can ROSA is shown below.

Two bypass capacitors are recommended for the IN4701 (photo on the right of figure 21). The capacitor values are 270 pF. While very good results have been achieved with only one bypass capacitor, the particulars of a customer's TO-can, photodiode and the gain band-width product variation of the IN4701 design (due to process variation) may result in low return loss at high frequencies when only one bypass capacitor is used (as in the photo on the left).

For best results, the bond wire from the photodiode to the TIA input should be perpendicular to the output bond wires. In the photos below, this is not the case because of the photodiodes that were available.

Ground is provided to the IN4701 from the back of the die using through-wafer vias found on pads 2, 4, 9 and 10. The back of the die is electrically connected to the TO-can using electrically conductive epoxy or eutectic die attach.

Important: Do not bond wires to pads 2, 4, 9 and 10 as these pads are connected to the chip's backside by through-wafer vias.

Important: The low cut-off frequency of the IN4701 is set internally. Adding capacitance to the DCA pad does not affect the low frequency cut-off of the IN4701.

Please read Inphi's Application Note on the IN4701 carefully.

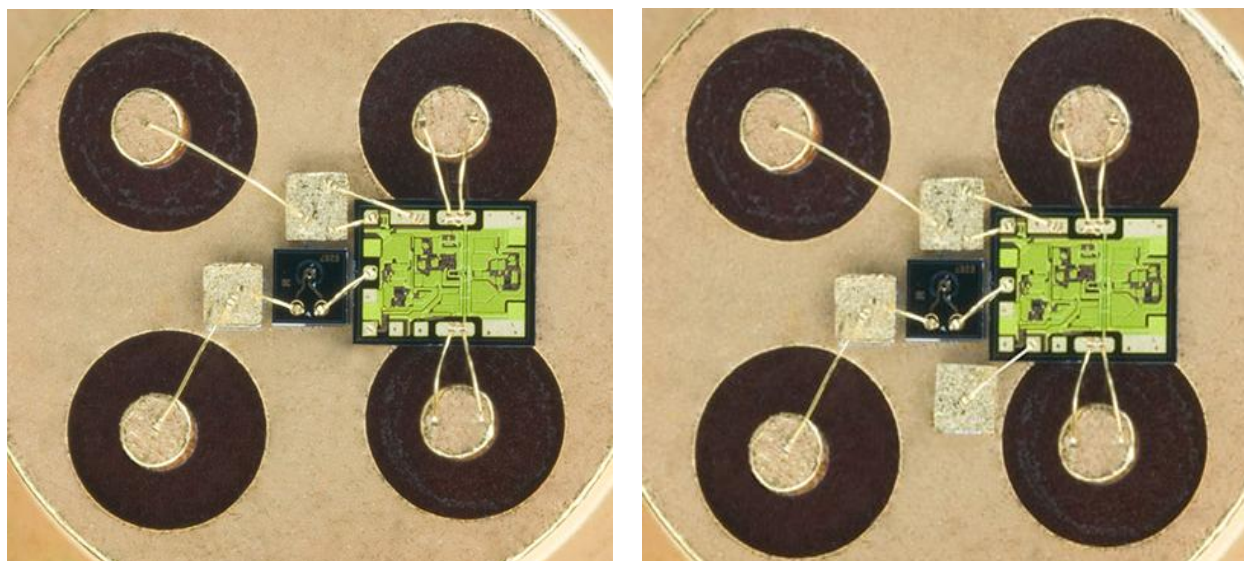


Figure 23. Suggested assemblies of IN4701 in a TO-can. To prevent any potential problems with output return loss, two bypass capacitors are recommended for the TIA power supplies (right photo)


Order Information

| Part No. | Description |
|--|--|
| IN4701-S01D | 11.3 Gbps TIA/LIA w/ TWV (12 k Ω Differential Gain) – Die |
| <i>For each customer application, customer's technical experts must validate all parameters. Inphi Corporation reserves the right to change product specifications contained herein without prior notice. No liability is assumed as a result of the use or application of this product. No circuit patent licenses are implied. Contact Inphi Corporation's marketing department for the latest information regarding this product.</i> | |

Contact Information

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- Fax: (805) 446-5189
- E-mail: products@inphi-corp.com

 Visit us on the Internet at: <http://www.inphi-corp.com>

Qualification Notification

The IN4701 uses the same die as the 1347TL-S01, which is fully qualified. Please contact Inphi for the qualification report.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

From 1347TL_DS_Ver1.6 to IN4701_DS_Ver1.0 (dated 2007-10-25)

1. Updated Features and Description sections (page 1):
 - a. Replaced Input overload current of 3.2 mA_{pp} with Input overload of +2 dBm.
 - b. Photodiode responsivity typical specification changed from 0.85 A/W to 0.9 A/W.
2. Updated Operating Conditions (page 3):
 - a. Removed parameters and specifications for “Operating Conditions, Normal V_{CC} Range”
 - b. Changed “Operating Conditions, Extended V_{CC} Range” to “Operating Conditions”.
 - c. Changed Supply Current parameter's maximum specification from 46 mA to 50 mA.
 - d. Changed On-Chip Power Dissipation parameter's max specification from 163 mW to 176 mW.
3. Updated Electrical Specifications (page 4):
 - a. Removed “10⁻¹² BER (NRZ format)” Conditions for Maximum Data Rate parameter.
 - b. Updated Input Sensitivity parameter:
 - i. Changed conditions from “@ 11.3 Gbps (ρ = 0.85 A/W, ER = 13 dB)” to “@ 11.3 Gbps (ρ = 0.9 A/W, ER = 10 dB)”
 - ii. Added maximum specification of – 18 dBm
 - c. Changed Input Overload parameter's conditions from “@ 10.7 Gbps, ρ = 1.0 A/W, ER = 13 dB” to “@ 11.3 Gbps, ρ = 0.9 A/W, ER = 10 dB”
 - d. Added Stressed Receiver Sensitivity (OMA) parameter, with Conditions = 10GBASE-ER and typical specification = -15.5 dBm.

Version Updates (cont'd.)

From 1347TL_DS_Ver1.6 to IN4701_DS_Ver1.0 (dated 2007-10-25) (cont'd.)

2. Updated Electrical Specifications (page 4) (cont'd.):
 - e. Updated Input Current parameter:
 - i. Changed Conditions from “V_{CC} = 3.3 V, T = 25 °C” to “Input signal 50% crossing”
 - ii. Changed max specification from 3.2 mA_{pp} to 2.4 mA_{pp}.
 - f. Updated Small Signal Transimpedance differential peak-to-peak parameter:
 - i. Removed “Normal V_{CC} range Operating Conditions, f=1—MHz” conditions and its specifications.
 - ii. Changed Conditions from “Extended V_{CC} range Operating Conditions, f=100 MHz” to “f = 1 GHz”.
 - iii. Changed minimum specification from 10 k Ω to 8 k Ω
 - iv. Changed maximum specification from 14.9 k Ω to 16 k Ω ,
 - g. Updated Output Amplitude differential peak-to-peak (Limited) parameter:
 - i. Removed both conditions as well as the specifications for “Normal V_{CC} range Operating Conditions, I_{IN} > 0.1 mA_{pp}”
 - ii. Changed maximum specification from 650 mV_{pp} to 680 mV_{pp}.
 - h. Updated Small Signal Z_T BW (3 dB) parameter:
 - i. Changed conditions from “Assumes photodiode specification on page 5” to “50 Ω environment”
 - ii. Changed maximum specification from 11.5 GHz to 12.5 GHz.
 - i. Updated Low Frequency Cutoff parameter:
 - i. Added Conditions = “P_{IN} = -20 dBm”
 - ii. Changed typical specification from 10 kHz to 40 kHz
 - iii. Changed maximum specification from 45 kHz to 100 kHz.
 - j. Removed one of the Added Peak-to-Peak Deterministic Jitter parameters, its conditions and specifications.
 - k. Updated the remaining Added Peak-to-Peak Deterministic Jitter parameter:
 - i. Removed the Conditions
 - ii. Maximum specification = 10 ps
 - l. Deleted Input Referred RMS Noise parameter, its conditions and specifications
 - m. Deleted Input Referred Noise Density parameter, its conditions and specifications
 - n. Changed Random Jitter parameter’s maximum specification from 0.8 ps RMS to 1.0 ps RMS.
 - o. Updated Output Return Loss parameter:
 - i. Changed condition from “f < 12 GHz” to “f < 10 GHz, 50 Ω environment”
 - ii. Removed footnote “Measured die on wafer”.
 - p. Changed parameter name from “Output Ripple” to “Z_T Ripple”
 - q. Updated Z_T Group Delay Variation parameter:
 - i. Changed conditions from “100 MHz – 8 GHz” to “100 MHz – 8 GHz, 50 Ω environment”.
 - ii. Removed footnote “Measured die on wafer”.
4. Updated Photodiode Specification Assumptions section (page 5)
 - a. Changed Photodiode Responsivity parameter’s typ specification from 0.85 A/W to 0.9 A/W.
5. Added Optical Receiver and Stressed Receiver Sensitivity section and Figures 1 - 3 (pages 6 - 7) and reordered figure numbering.
6. Removed “Over-Load Filter Capacitor” section and related figure.
7. Updated Order Information section to reflect IN4701 part information. (page 16)
8. Updated Qualification Notification section to indicate that this part is fully qualified. (page 16).

Version Updates (cont'd)

From Version 1.0 to 1.1 (dated 2007-11-26)

1. Removed “Preliminary” watermark from document.
2. Updated Electrical Specifications (page 4):
 - a. Changed Conditions for Stressed Receiver Sensitivity (OMA) parameter from 10GBASE-ER to 10GBASE-LR
 - b. Changed min specification for Output Amplitude, differential peak-to-peak (Limited) parameter from 340 mVpp to 300 mVpp.
3. Updated Figure 2 caption by changing “10GBASE-ER” to “10GBASE-LR” (page 6).

From Version 1.1 to 1.2 (dated 2007-12-18)

1. Updated Operating Conditions (page 3):
 - a. Updated Power Supply Voltage parameter:
 - i. Changed Conditions from “+7, -10% Tolerance” to “ $-20\text{ }^{\circ}\text{C} \leq T_C \leq 95\text{ }^{\circ}\text{C}$ ”
 - ii. Added second set of Conditions “ $-40\text{ }^{\circ}\text{C} \leq T_C \leq 95\text{ }^{\circ}\text{C}$ ” with the following specifications:
 1. Min spec = +3.135 V
 2. Typ spec = +3.300 V
 3. Max spec = +3.465 V
 - b. Updated Operating Temperature (Die backside) parameter:
 - i. Added Conditions “ $+2.970\text{ V} \leq V_{CC1}, V_{CC2} \leq +3.530$ “ $+2.970\text{ V} \leq V_{CC1}, V_{CC2} \leq +3.530\text{ V}$ ” to existing specifications.
 - ii. Added second set of Conditions “ $+3.135\text{ V} \leq V_{CC1}, V_{CC2} \leq +3.465\text{ V}$ ” with the following specifications:
 1. Min spec = $-40\text{ }^{\circ}\text{C}$
 2. Max spec = $+95\text{ }^{\circ}\text{C}$

From Version 1.2 to 1.3 (dated 2008-03-24)

1. Updated Operating Conditions (page 4):
 - a. Updated Input Current
 - i. Changed maximum value from 2.4 mApp to 2.5 mApp.

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