4027-2/4027-3/4027-4-F,I,N

DESCRIPTION

The 4027 is fabricated with n-channel silicon gate technology for high performance and high functional density, and uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 4027 allows it to be packaged in the industry standard 16-pin dual inline package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16-pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 4027 on 6 address input pins. The two 6-bit address words are latched into the device by the 2TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

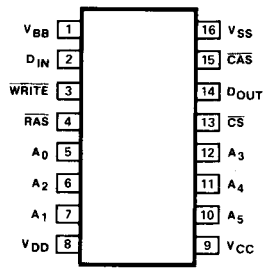
The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention, and this is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2ms, or by performing a $\overline{RAS}$ only cycle.

FEATURES

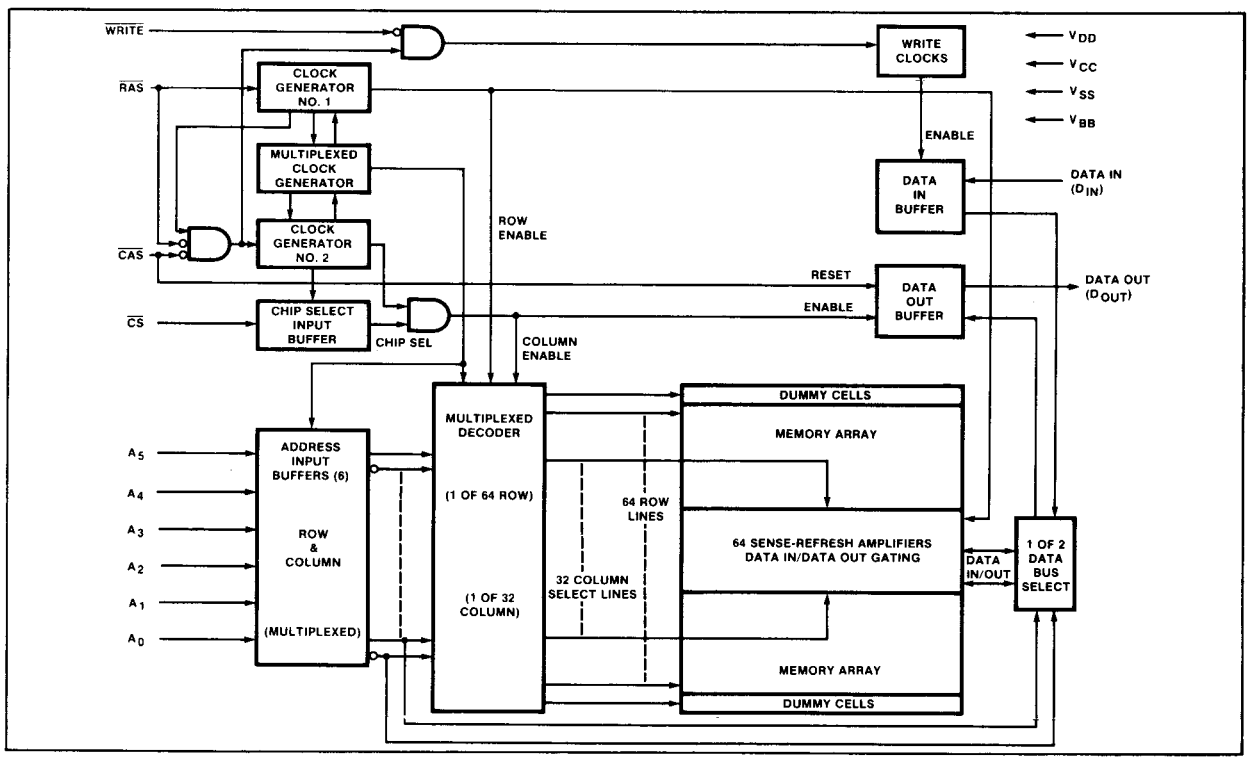
- **All inputs including clock TTL compatible**
- **On chip latches for address, chip select and data in**
- **3-state TTL compatible output**
- **Output data is latched and valid into next cycle**
- **Access time:**
  - **4027-2: 150ns**
  - **4027-3: 200ns**
  - **4027-4: 250ns**
- **Read and write cycle time:**
  - **4027-2: 320ns**
  - **4027-3: 375ns**
  - **4027-4: 375ns**
- **Low power:**
  - **Operating: 462mW**
  - **Standby: 27mW**
- **RAS only refresh (no dummy cycles required)**
- **Page mode addressing**
- **±10% power supply margins**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM

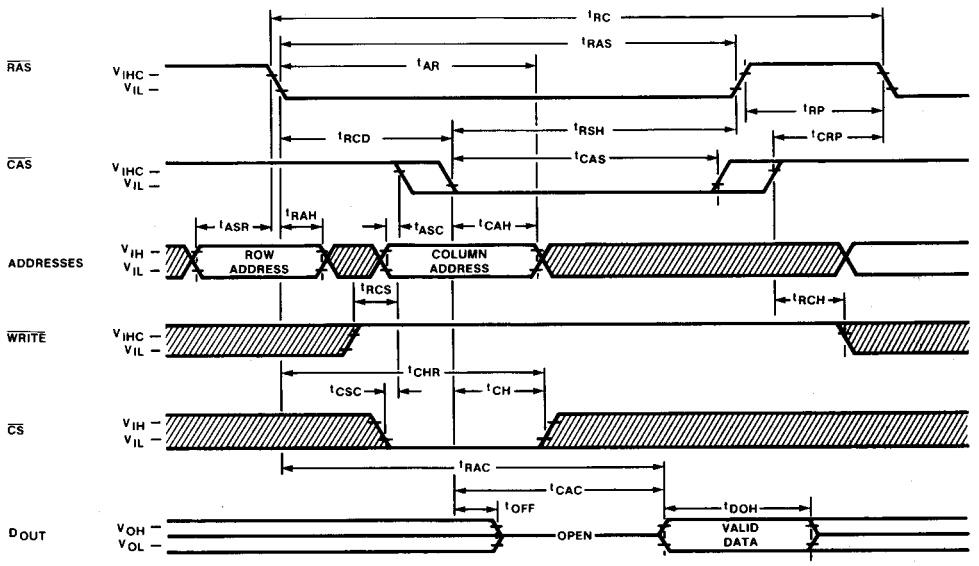


AC CHARACTERISTICS [3,11,12] T_A = 0°C to +70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0V unless otherwise specified.

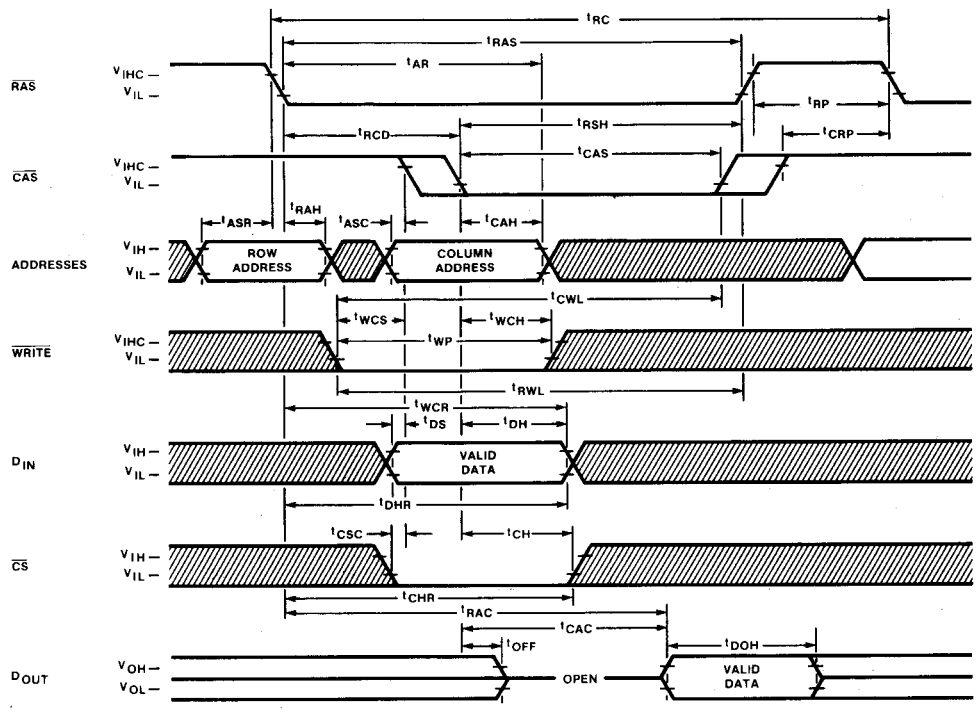
SYMBOL	PARAMETER	TEST CONDITIONS	4027-2		4027-3		4027-4		UNIT
			Min	Max	Min	Max	Min	Max	
	READ OR WRITE (EARLY) CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RC}[17]	Random cycle		320		375		375		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		120		ns
t_{RCD}[16]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100		135		165		ns
t_{CRP}	$\overline{CAS}$ precharge		0		0		0		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CSC}	Chip select address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{CH}	Chip select hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{CHR}	Chip select to $\overline{RAS}$ hold		95		120		160		ns
t_{OFF}	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[14,15]	Row access			150		200		250	ns
t_{CAC}[13,14]	Column access			100		135		165	ns
t_{DOH}	Data out hold			10		10		10	μs
	READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
	WRITE (EARLY) CYCLE								
t_{WCS}	Write set up		0		0		0		ns
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}[18]	Data set up		0		0		0		ns
t_{DH}[18]	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



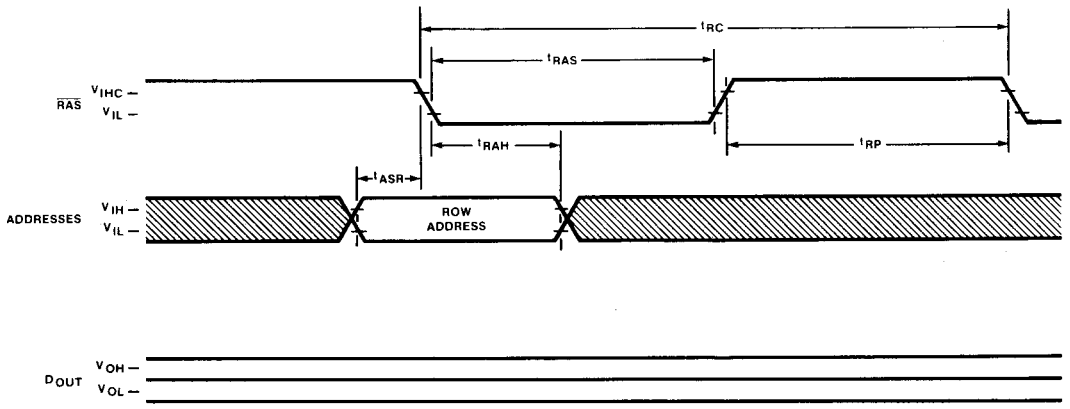
AC CHARACTERISTICS [3,11,12]

T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	4027-2		4027-3		4027-4		UNIT
			Min	Max	Min	Max	Min	Max	
	$\overline{RAS}$ ONLY REFRESH CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RC}[17]	Random cycle		320		375		375		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		120		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
	READ/WRITE OR READ/MODIFY/WRITE								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RWC}[17,20]	Read/write cycle		330		420		480		ns
t_{RMW}[17,20]	Read/modify/write cycle		380		470		530		ns
t_{RRAS}	R/W $\overline{RAS}$ duration		215	10000	300	10000	380	10000	ns
t_{MRAS}	RMW $\overline{RAS}$ duration		265	10000	350	10000	430	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[16]	Strobe delay		20	50	25	65	35	85	ns
t_{RCAS}	R/W $\overline{CAS}$ duration		165		235		295		ns
t_{MCAS}	RMW $\overline{CAS}$ duration		215		285		345		ns
t_{CRP}	$\overline{CAS}$ precharge		0		0		0		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CSC}	Chip select set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{CH}	Chip select hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{CHR}	Chip select to $\overline{RAS}$ hold		95		120		160		ns
t_{RCS}	Read set up		0		0		0		ns
t_{RWD}[19]	$\overline{RAS}$ to write delay		110		145		175		ns
t_{CWD}[19]	$\overline{CAS}$ to write delay		60		80		90		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WP}	Write duration		45		55		75		ns
t_{MOD}	Modify		0	9735	0	9650	0	9570	ns
t_{DS}	Data set up		0		0		0		ns
t_{DH}	Data hold		45		55		75		ns
t_{OFF}	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[14,15]	Row access		150		200		250		ns
t_{CAC}[13,14]	Column access		100		135		165		ns
t_{DOH}	Data out hold			10		10		10	μs

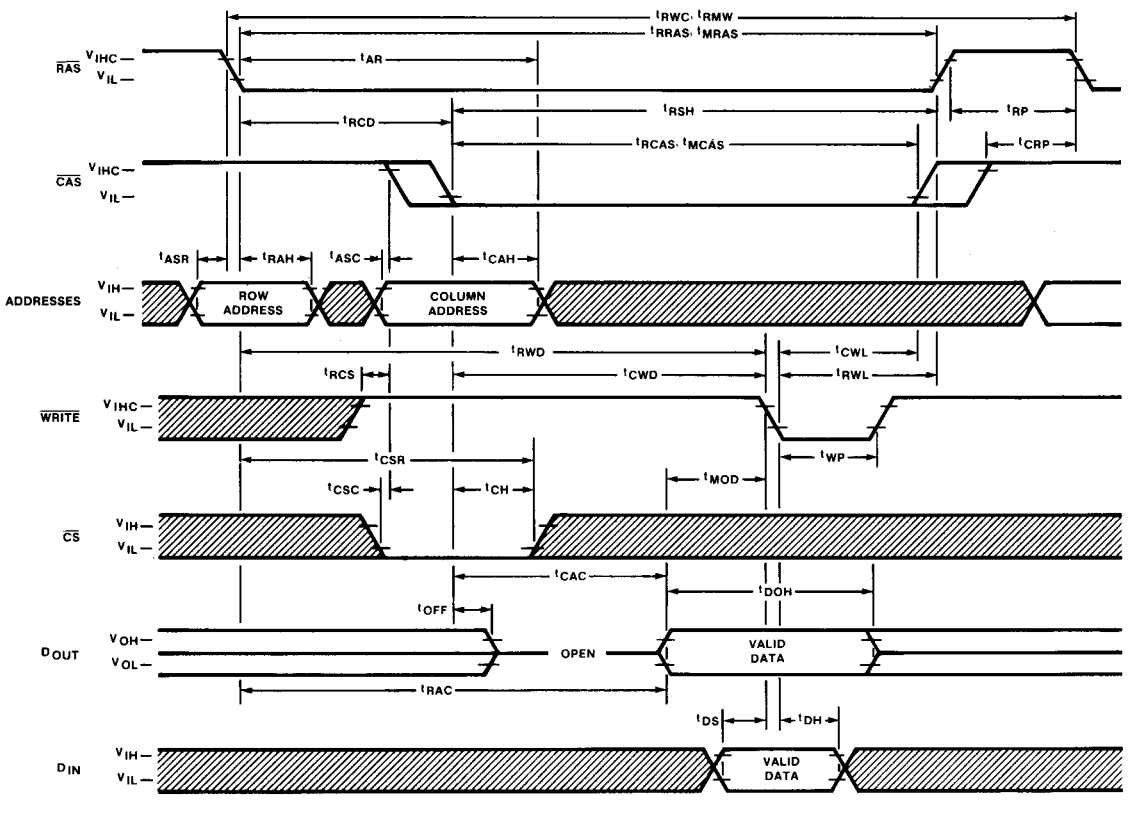
TIMING DIAGRAMS (Cont'd)

"$\overline{RAS}$ ONLY" REFRESH CYCLE



DOUT remains unchanged from previous cycle.

READ/WRITE, READ/MODIFY WRITE CYCLE

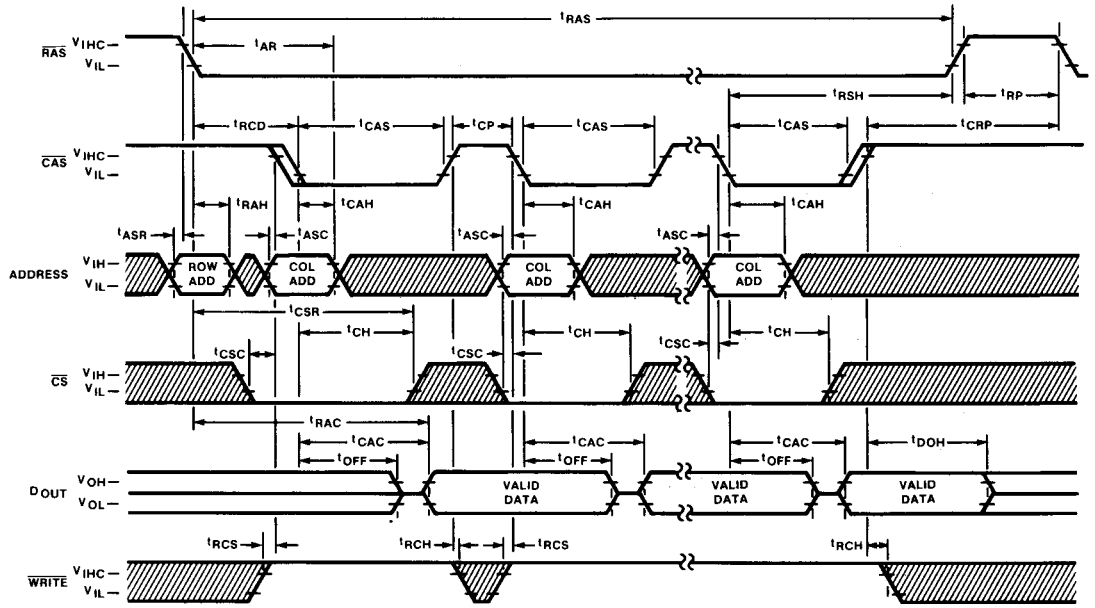


AC CHARACTERISTICS [3,11,12] T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = OV unless otherwise specified.

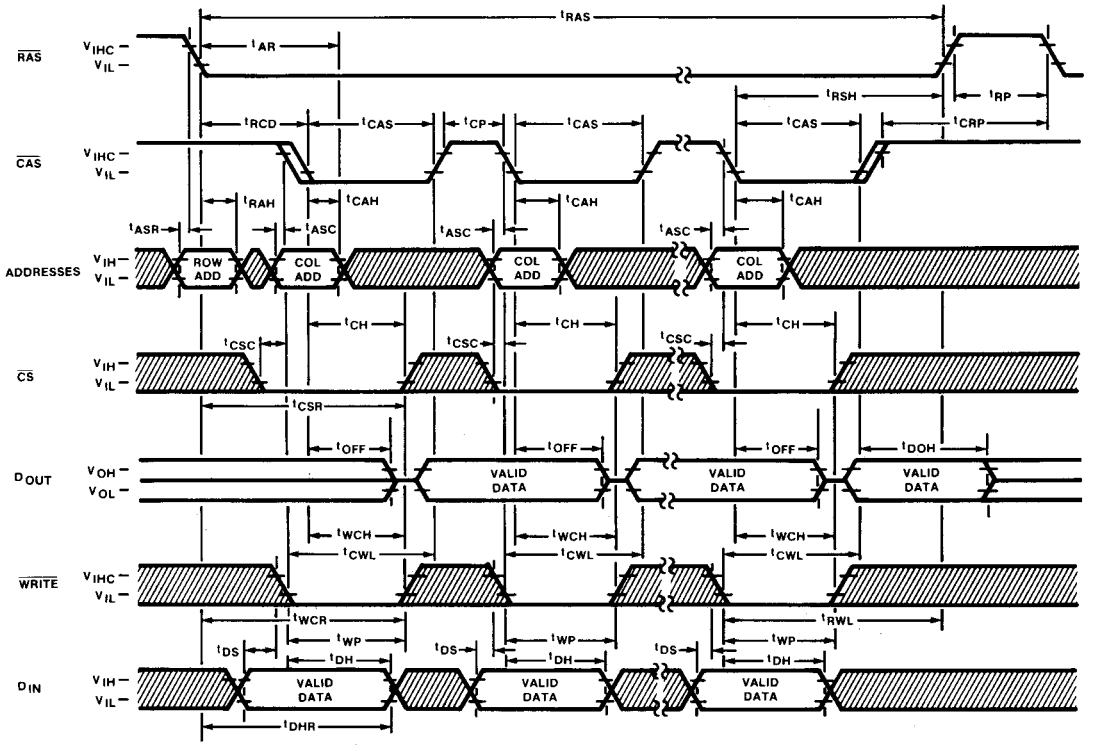
SYMBOL	PARAMETER	TEST CONDITIONS	4027-2		4027-3		4027-4		UNIT
			Min	Max	Min	Max	Min	Max	
	PAGE MODE CYCLES								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[16]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100		135		165		ns
t_{CP}	$\overline{CAS}$ HIGH duration		60		80		110		ns
t_{PC}	Page mode cycle		170		225		275		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CRP}	$\overline{CAS}$ precharge		0		0		0		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CSC}	Chip select set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{CH}	Chip select hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{CSR}	Chip select to $\overline{RAS}$ hold		95		120		160		ns
	PAGE MODE READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
t_{OFF}	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[14,15]	Row access		150		200		250		ns
t_{CAC}[13,14]	Column access		100		135		165		ns
t_{DOH}	Data out hold			10		10		10	µs
	PAGE MODE WRITE CYCLE								
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{CWL}	Write lead		50		70		85		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}	Data set up		0		0		0		ns
t_{DH}	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

TIMING DIAGRAMS (Cont'd)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-55 to 150	
	All input or output voltages with respect to the most negative supply voltage V_{BB}	+20 to -.5	V
	Supply voltage V_{DD}, V_{CC} and V_{SS} with respect to V_{BB}	+20 to -1	V
	V_{BB} - V_{SS} with V_{DD} - V_{SS} > 0	0	V

DC ELECTRICAL CHARACTERISTICS[2,3]

T_A = 0°C to 70°C, V_{DD} + 12V ± 10%, V_{CC}[4] = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage	Any input				V
V_{IL}	Low		-1.0		0.8	
V_{IH}	High		2.4		7.0	
	Output voltage					V
V_{OL}	Low	I_{OL} = 3.2mA	0.0		0.4	
V_{OH}	High	I_{OH} = -5.0mA	2.4		V_{CC}	
	Leakage current	Any input				µA
I_{IL}	Input[5]				10	
I_{OL}	Output[6,7]				10	
	V_{DD} current					mA
I_{DD1}	Average[8]				35	
I_{DD2}	Standby[6]	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}		1	2	
I_{DD3}	Average	$\overline{RAS}$ only cycles			25	
I_{CC}	V_{CC} supply current[9]					mA
I_{BB}	Average V_{BB} current				150	µA
	Capacitance					pF
C_{AD}	Address, D_{IN}, $\overline{CS}$[10]				5	
C_C	$\overline{CAS}$, $\overline{RAS}$,[10] $\overline{WRITE}$				10	
C_{OUT}	Output[6,10]				7	

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}.
3. Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
4. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
5. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
6. Output is disabled (high impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilizations is required prior to measurement of this parameter.
7. $0V \le V_{OUT} \le +10V$.
8. Current is proportioned to cycle rate, I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See Figure 1 for I_{DD1} limits at other cycle rates.
9. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
10. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{\Delta v}$ with Δv = 3 volts.
11. A.C. measurements assume t_T = 5ns.
12. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
13. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
14. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
15. Assumes that $t_{RCD} \le t_{RCD}$ (max).
16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
17. The specifications for t_{RC} (min), t_{RWC} (min), and t_{RMW} (max) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read/modify write cycles.
19. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min), the cycle is a read/write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
20. For t_{RWC} (min), t_{MOD} is -40ns. For t_{RMW} (min), t_{MOD} time available is at least +10ns. There is no restriciton on t_{RMW} (min) but t_{MOD} time available is naturally then affected. For $t_{RMW} < t_{RMW}$ (min) +10ns, cycle then becomes t_{RWC} where $t_{MOD} < 0$ns.