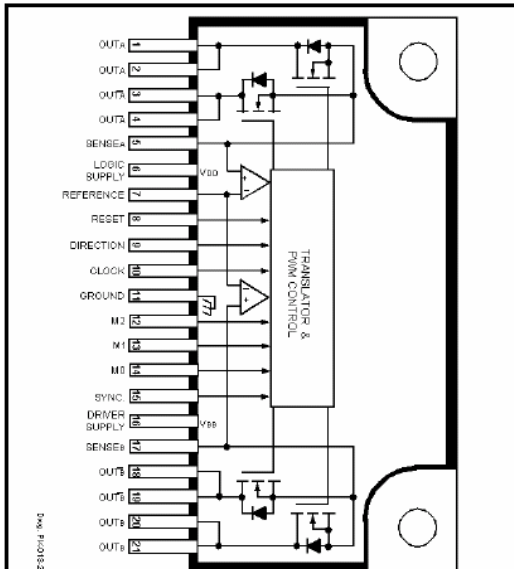


SLA7060M/7061M/7062M

October 2005

UNIPOLAR STEPPER-MOTOR TRANSLATOR/DRIVERS



ABSOLUTE MAXIMUM RATINGS

Driver Supply Voltage, V_{BB}	46 V
Load Supply Voltage, V_M	46 V
Output Current, I_O	
SLA7060M	1.0 A*
SLA7061M	2.0 A*
SLA7062M	3.0 A*
Logic Supply Voltage, V_{DD}	7.0 V
Logic Input Voltage Range,	
V_I	-0.3 V to $V_{DD} + 0.3$ V
Sense Voltage, V_S	± 2.0 V†
Reference Input Voltage Range,	
V_{REF}	-0.3 V to $V_{DD} + 0.3$ V
Package Power Dissipation,	
P_D	See Graph
Junction Temperature, T_J	+150°C
Operating Temperature Range,	
T_A	-20°C to +85°C
Storage Temperature Range,	
T_S	-30°C to +150°C

* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or junction temperature.

† Internal filtering provides protection against transients during the first 1 μ s of the current-sense pulse.

Combining low-power CMOS logic with high-current, high-voltage power FET outputs, the Series SLA7060M translator/drivers provide complete control and drive for a two-phase unipolar stepper motor with internal fixed off time and pulse-width modulation (PWM) control of the output current in a power multi-chip module (PMCM™). There are no phase-sequence tables, high-frequency control lines, or complex interfaces to program.

The CMOS logic section provides the sequencing logic, direction, control, synchronous/asynchronous PWM operation, and a “sleep” function. The minimum CLOCK input is an ideal fit for applications where a complex μ P is unavailable or overburdened. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure a proper input-logic high. For PWM current control, the maximum output current is determined by the user’s selection of a reference voltage and sensing resistor. The NMOS outputs are capable of sinking up to 1, 2, or 3 A (depending on device) and withstanding 46 V in the off state. Clamp diodes provide protection against inductive transients. Special power-up sequencing is not required.

Half-, quarter-, eighth-, and sixteenth-step operation are externally selectable for the SLA7060/61/62M. Half-step excitation alternates between the one-phase and two-phase modes (AB-B-AB-A-AB-B-AB-A), providing an eight-step sequence.

The Series SLA7060M is supplied in a 21-pin single in-line power-tab package with leads formed for vertical mounting (suffix LF2102). The tab is at ground potential and needs no insulation. For high-current or high-frequency applications, external heat sinking may be required. This device is rated for continuous operation between -20°C and +85°C.

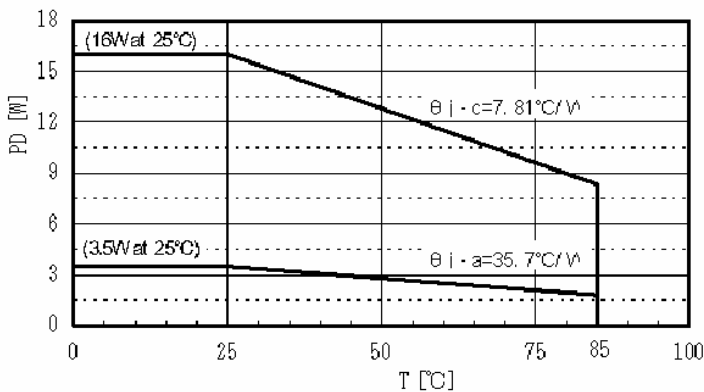
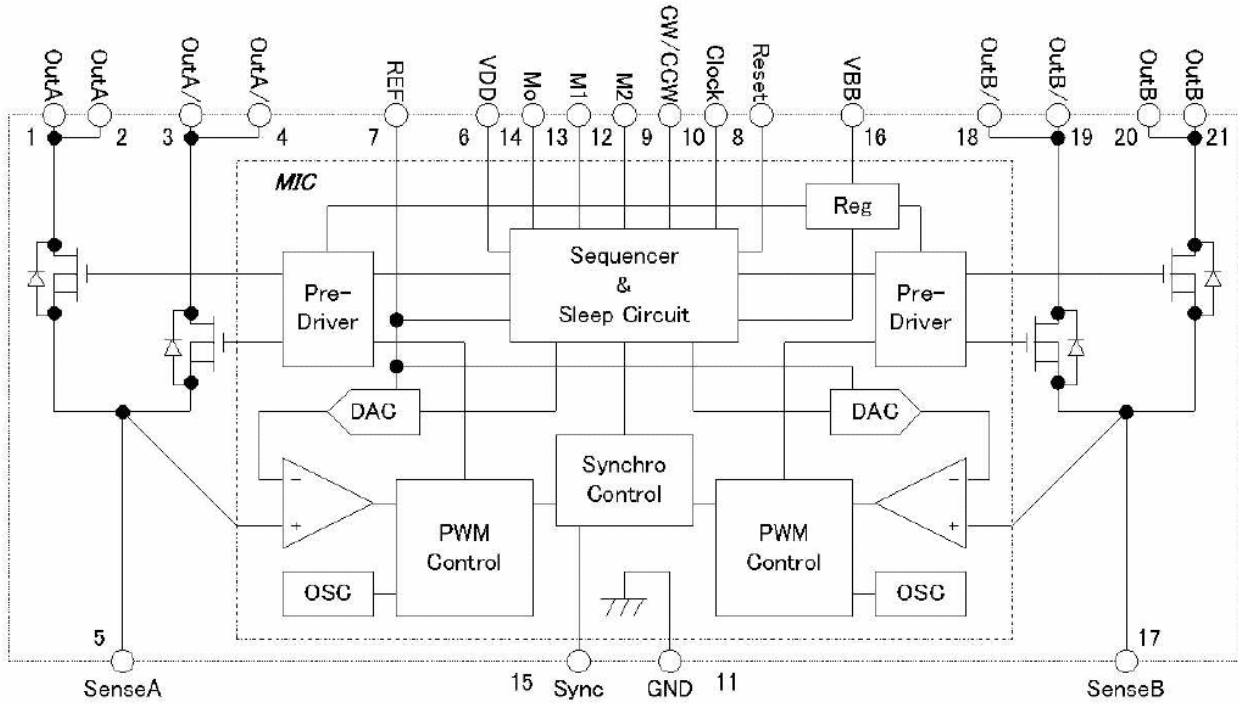
FEATURES

- To 3 A Output Rating
- Internal Sequencer for Microstepping Operation
- PWM Constant-Current Motor Drive
- Cost-Effective, Multi-Chip Solution
- 100 V, Avalanche-Rated NMOS
- Low $r_{DS(on)}$ NMOS Outputs
- Advanced, Improved Body Diodes
- Inputs Compatible with 3.3 V or 5 V Control Signals
- Sleep Mode
- Internal Clamp Diodes

Always order by complete part number, e.g., **SLA7060MLF2102**.

SLA7060M/7061M/7062M

October 2005



Recommended operating conditions

- Load Supply Voltage, V_{BB} 10 to 44 V
- Logic Supply Voltage, V_{DD} 3.0 V to 5.5 V
- Reference Input Voltage, V_{REF} 0.1 V to 1.0 V
- Tab Temperature (no heat sink), T_T <90°C

SLA7060M/7061M/7062M

October 2005

Electrical characteristics: unless otherwise noted at $T_A = +25^\circ\text{C}$, $V_{BB} = 24\text{ V}$, $V_{DD} = 5.0\text{ V}$.

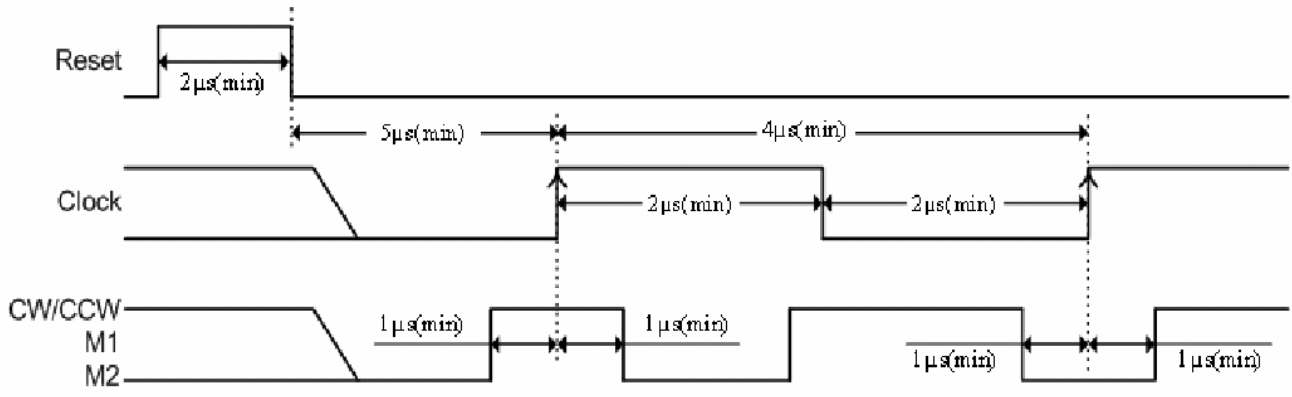
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output drivers						
Driver Supply Volt. Range	V_{BB}	Operating	10	—	44	V
Drain-Source Breakdown	$V_{(BR)DS}$	$V_{BB} = 44\text{ V}$, $I_D = 1\text{ mA}$	100	—	—	V
Output On Resistance	$r_{DS(on)}$	SLA7060M, $I_O = 1.0\text{ A}$	—	700	850	m Ω
		SLA7061M, $I_O = 2.0\text{ A}$	—	250	400	m Ω
		SLA7062M, $I_O = 3.0\text{ A}$	—	180	240	m Ω
Body Diode Forward Volt.	V_F	SLA7060M, $I_F = 1.0\text{ A}$	—	0.85	1.1	V
		SLA7061M, $I_F = 2.0\text{ A}$	—	0.95	1.2	V
		SLA7062M, $I_F = 3.0\text{ A}$	—	0.95	2.1	V
Driver Supply Current	I_{BB}		—	—	15	mA
		$V_{REF} > 2.0\text{ V}$ (sleep mode)	—	—	100	μA
Control logic						
Logic Supply Volt. Range	V_{DD}	Operating	3.0	5.0	5.5	V
Logic Input Voltage	V_{IH}		$0.75V_{DD}$	—	—	V
	V_{IL}		—	—	$0.25V_{DD}$	V
Logic Input Current	I_{IH}		—	± 1.0	—	μA
	I_{IL}	CLOCK, RESET, CW/CCW, and SYNC. M1 and M2	—	± 1.0	—	μA
Max. Clock Frequency	f_{clk}		250*	—	—	kHz
PWM Off Time	t_{off}	70 to 100% $I_{trip,max}$	—	12	—	μs
		38 to 64% $I_{trip,max}$	—	9.0	—	μs
		9 to 30% $I_{trip,max}$	—	7.0	—	μs
PWM Min. On Time	$t_{on(min)}$		—	1.8	—	μs
Ref. Input Voltage Range	V_{REF}	Operating	0	—	1.5	V
		Sleep mode	2.0	—	V_{DD}	V
Ref. Input Current	I_{REF}		—	± 10	—	μA
Monitor Output Voltage	V_{MoH}		$V_{DD} - 1.25$	—	—	V
	V_{MoL}		—	—	1.25	V
Monitor Output Current	I_{Mo}		—	—	± 3.0	mA
Sense Voltage	V_S	Trip point at 100% I_O	$0.95V_{REF}$	V_{REF}	$1.05V_{REF}$	V
Sense Input Current	I_{SENSE}		—	± 10	—	μA
Propagation Delay Time	t_{PLH}	Clock rising edge to output on	—	2.0	—	μs
	t_{PHL}	Clock rising edge to output off	—	1.5	—	μs
Logic Supply Current	I_{DD}		—	—	4.0	mA

Typical values are given for circuit design information only.

*Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

SLA7060M/7061M/7062M

October 2005

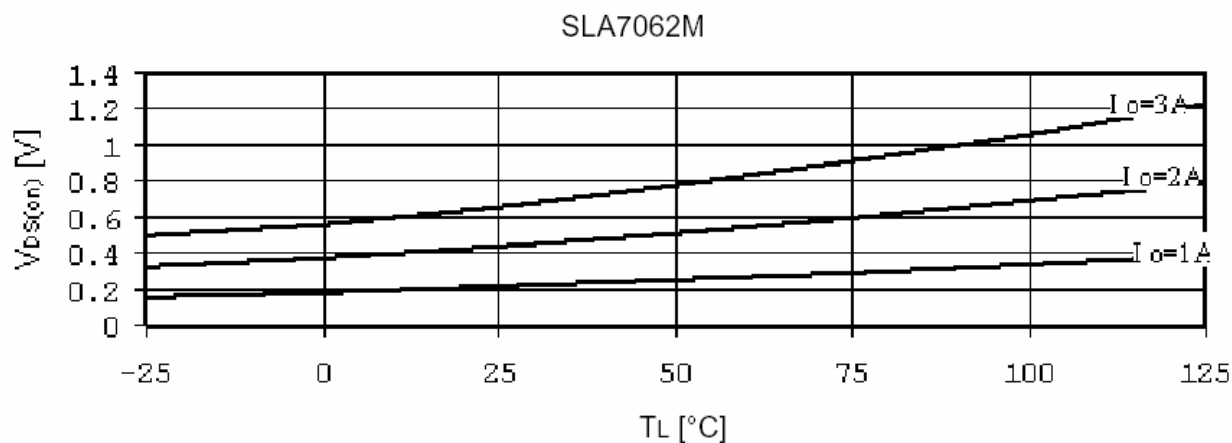
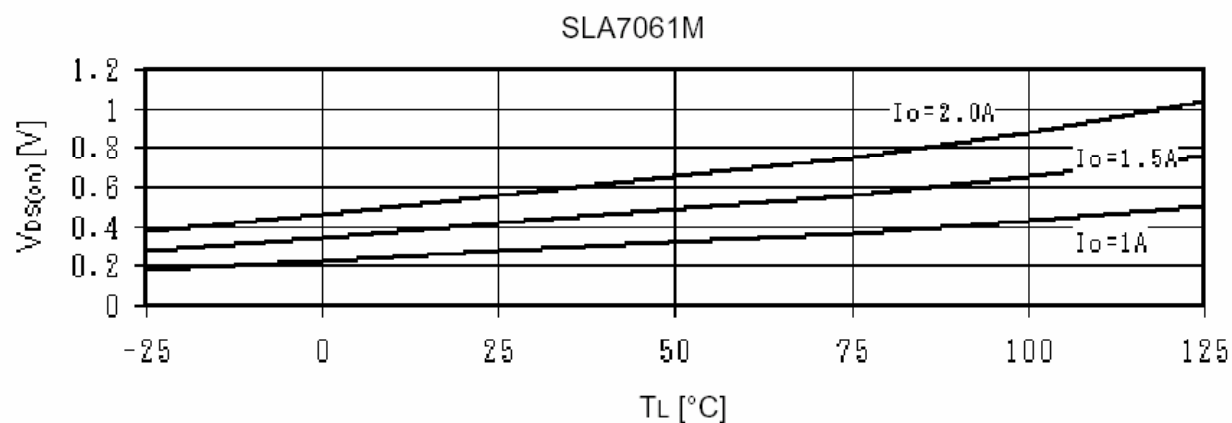
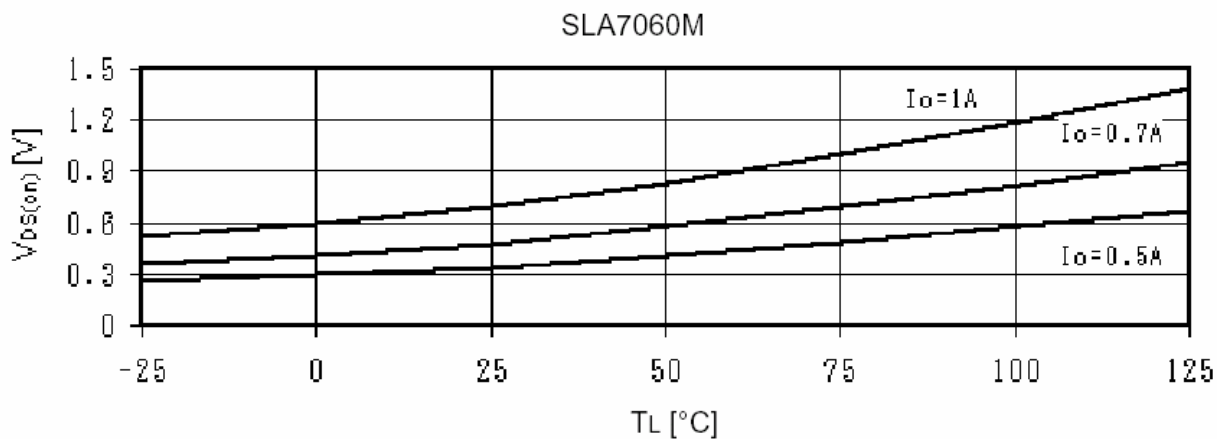


Logic input timing

SLA7060M/7061M/7062M

October 2005

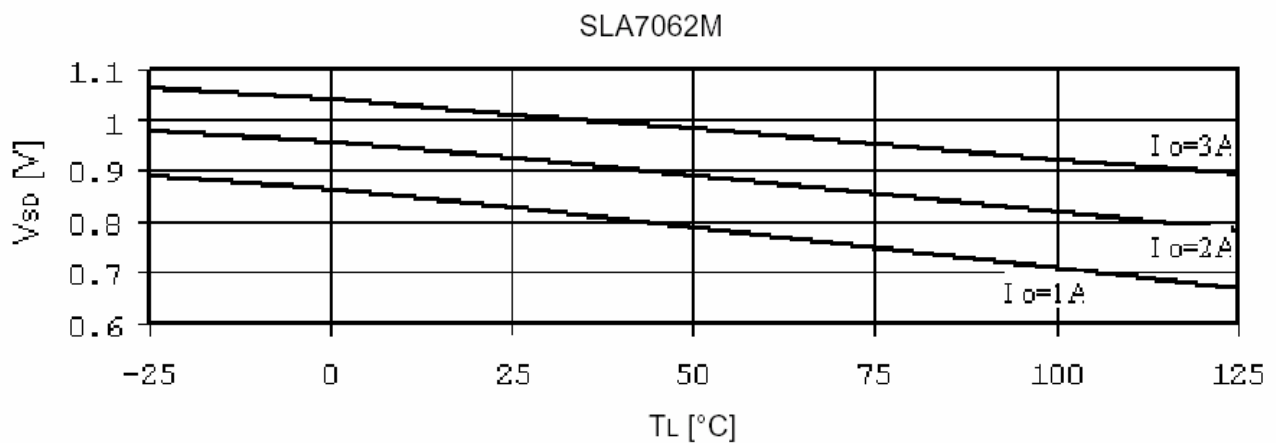
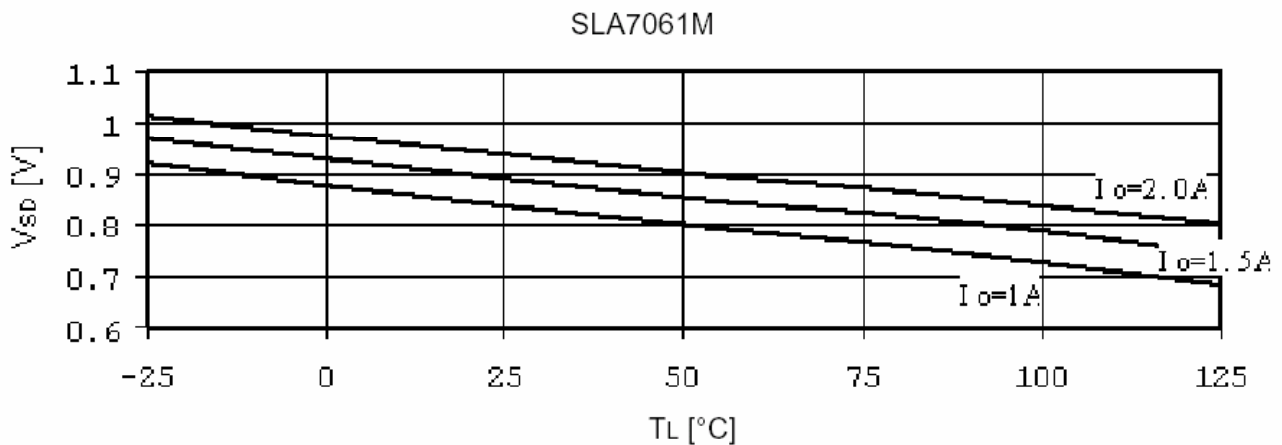
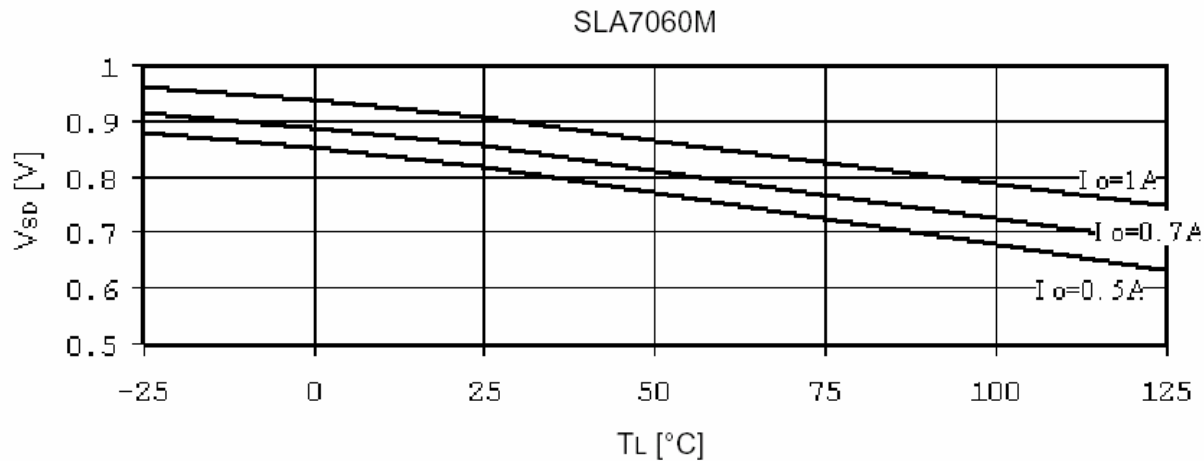
Typical MOSFET characteristics



SLA7060M/7061M/7062M

October 2005

Typical body diode characteristics



SLA7060M/7061M/7062M

October 2005

Functional description

Device operation. These devices are complete microstepping motor drivers with built in translator for easy operation with minimal control lines. They are designed to operate unipolar stepper motors in half-, quarter-, eighth-, and sixteenth-step modes. The current in each of the four outputs, all n-channel DMOS, is regulated with fixed off time pulse-width modulated (PWM) control circuitry. The current at each step is set by the value of an external current-sense resistor (R_S), a reference voltage (V_{REF}), and the DAC's output voltage controlled by the output of the translator.

At V_{DD} power up, or reset, the translator sets the DACs to the home state (see figures for reset conditions). When a step command signal occurs on the CLOCK input the translator automatically sequences the DACs to the next level (see table 2 for the current level sequence). The microstep resolution is set by inputs M1 and M2 as shown in table 1.

RESET input. The RESET input sets the translator to a predefined home state (see table 2); this is not the same as the sleep mode. The monitor output (MO) goes low and all STEP inputs are ignored until the RESET input goes low. A low-pass filter is integrated into the reset circuit; therefore a 5 μ s delay is required between the falling edge of the RESET input and the rising edge of the CLOCK input.

Monitor output (MO). A logic output indicator of the initial/home state of the translator (45°). At power up the translator is reset to the home state (phase A and phase B output currents are both at the half-step position or 70.7%). This output is also high at the 135° , 225° , and 315° positions.

CLOCK (step) input. A low-to-high transition on the clock input sequences the translator, which controls the input to the DACs and advances the motor one increment. The size of the increment is determined by the state of inputs M1 and M2 (see table 1). The hold state is done by stopping the CLOCK input regardless of the input level.

Microstep select (M1 and M2). These logic-level inputs set the translator step mode per table 1. Changes to these inputs do not take effect until the rising edge of the clock input.

Direction (CW/CCW) input. This logic-level input sets the translator step direction. Changes to this input do not take effect until the rising edge of the clock input.

Internal PWM current control. Each pair of outputs is controlled by a fixed off-time (7 to 12 μ s, depending on step) PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, an output is enabled and current flows through the motor winding and R_S . When the voltage across the current-sense resistor equals the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off the driver for the fixed off time during which the load inductance causes the current to recirculate for the off time period. The driver is then re-enabled and the cycle repeats.

Synchronous operation mode. This function prevents occasional motor noise during a "hold" state, which normally results from asynchronous PWM operation of both motor phases. A logic high at the SYNC input is synchronous operation; a logic low is asynchronous operation. The use of synchronous operation during normal stepping is not recommended because it produces less motor torque and can cause motor vibration due to staircase current.

Sleep mode. Applying a voltage greater than 2 V to the REF pin disables the outputs and puts the motor in a free state (coast). This function is used to minimize power consumption when not in use. Although it disables much of the internal circuitry including the output MOSFETs and regulator, the sequencer/translator circuit is active and therefore a microcontroller can set the step starting point for the next operation during the sleep mode. When coming out of sleep mode, wait 100 μ s before issuing a step command to allow the internal circuitry to stabilize.

Table 1. Step Modes

Input M1	Input M2	Step Mode
H	H	Half Step
H	L	Quarter Step
L	H	Eighth Step
L	L	Sixteenth Step

SLA7060M/7061M/7062M

October 2005

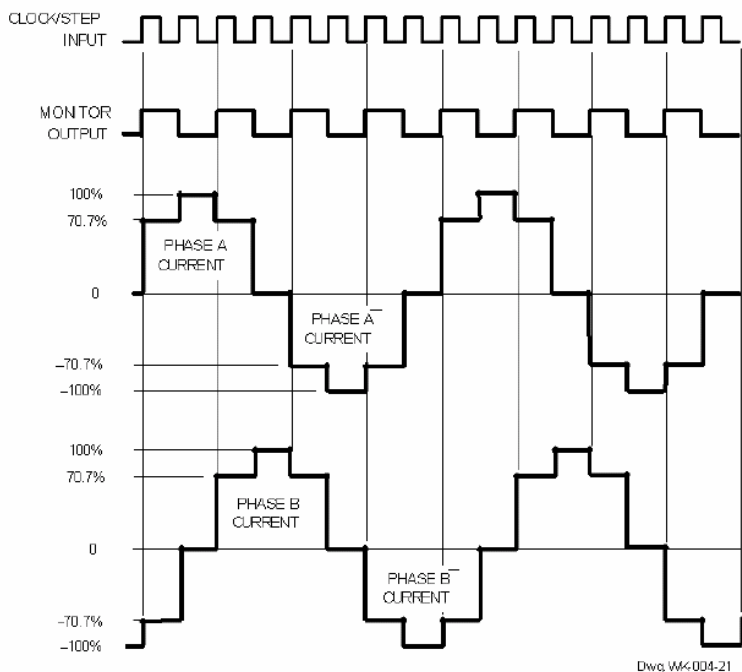
Table 2. Step Sequencing
(CW/CCW = L)

Half Step #	Quarter Step #	Eighth Step #	Sixteenth Step #	Phase A or A\ Current [%I _{tp_max}]	Phase B or B\ Current [%I _{tp_max}]	Step Angle
0	0	0	0	70.7	70.7	45°
		1	1	77.3	63.4	
			2	83.1	55.5	
	1		3	88.2	47.1	
		2	4	92.4	38.2	67.5
			5	95.7	29.0	
		3	6	98.1	19.5	
			7	100	9.8	
1	2	4	8	100	0	90
			9	100	-9.8	
		5	10	98.1	-19.5	
			11	95.7	-29.0	
	3	6	12	92.4	-38.2	102.5
			13	88.2	-47.1	
		7	14	83.1	-55.5	
			15	77.3	-63.4	
2	4	8	16	70.7	-70.7	135†
			17	63.4	-77.3	
		9	18	55.5	-83.1	
			19	47.1	-88.2	
	5	10	20	38.2	-92.4	157.5
			21	29.0	-95.7	
		11	22	19.5	-98.1	
			23	9.8	-100	
3	6	12	24	0	-100	180
			25	-9.8	-100	
		13	26	-19.5	-98.1	
			27	-29.0	-95.7	
	7	14	28	-38.2	-92.4	202.5
			29	-47.1	-88.2	
		15	30	-55.5	-83.1	
			31	-63.4	-77.3	
4	8	16	32	-70.7	-70.7	225†
			33	-77.3	-63.4	
		17	34	-83.1	-55.5	
			35	-88.2	-47.1	
	9	18	36	-92.4	-38.2	247.5
			37	-95.7	-29.0	
		19	38	-98.1	-19.5	
			39	-100	-9.8	
5	10	20	40	-100	0	270
			41	-100	9.8	
		21	42	-98.1	19.5	
			43	-95.7	29.0	
	11	22	44	-92.4	38.2	292.5
			45	-88.2	47.1	
		23	46	-83.1	55.5	
			47	-77.3	63.4	
6	12	24	48	-70.7	70.7	315†
			49	-63.4	77.3	
		25	50	-55.5	83.1	
			51	-47.1	88.2	
	13	26	52	-38.2	92.4	337.5
			53	-29.0	95.7	
		27	54	-19.5	98.1	
			55	-9.8	100	
7	14	28	56	0	100	360
			57	9.8	100	
		29	58	19.5	98.1	
			59	29.0	95.7	
	15	30	60	38.2	92.4	22.5
			61	47.1	88.2	
		31	62	55.5	83.1	
			63	63.4	77.3	
8	16	32	64	70.7	70.7	45°

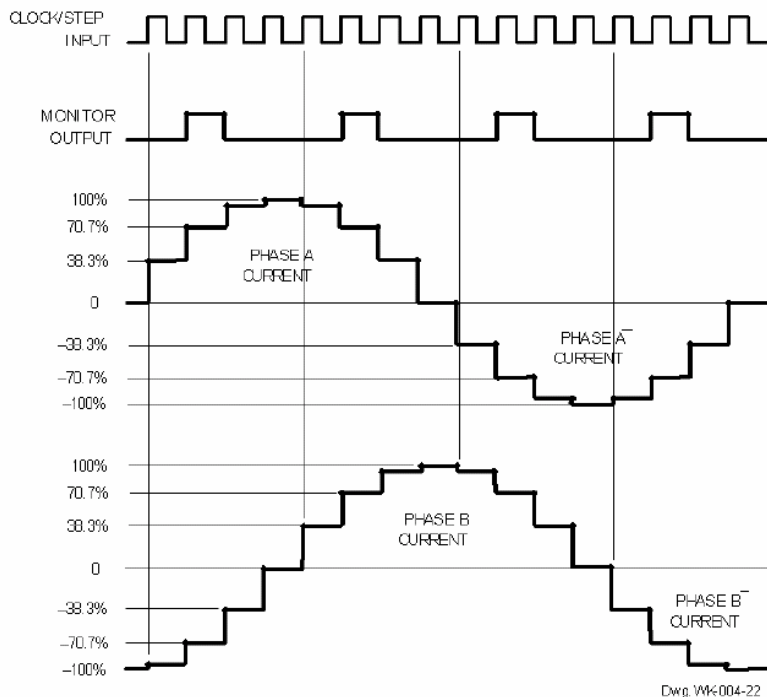
* Home state: MO output high. † MO output high.

SLA7060M/7061M/7062M

October 2005



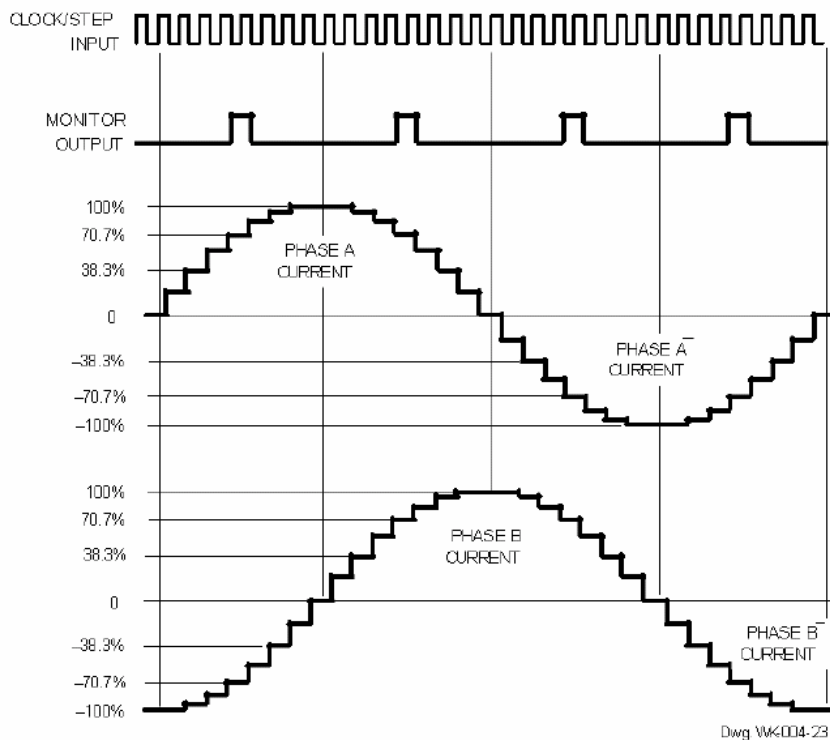
Half-step output current waveshapes. For illustrative purposes, phase A\ or B\ current (unipolar drive) is shown as negative current.



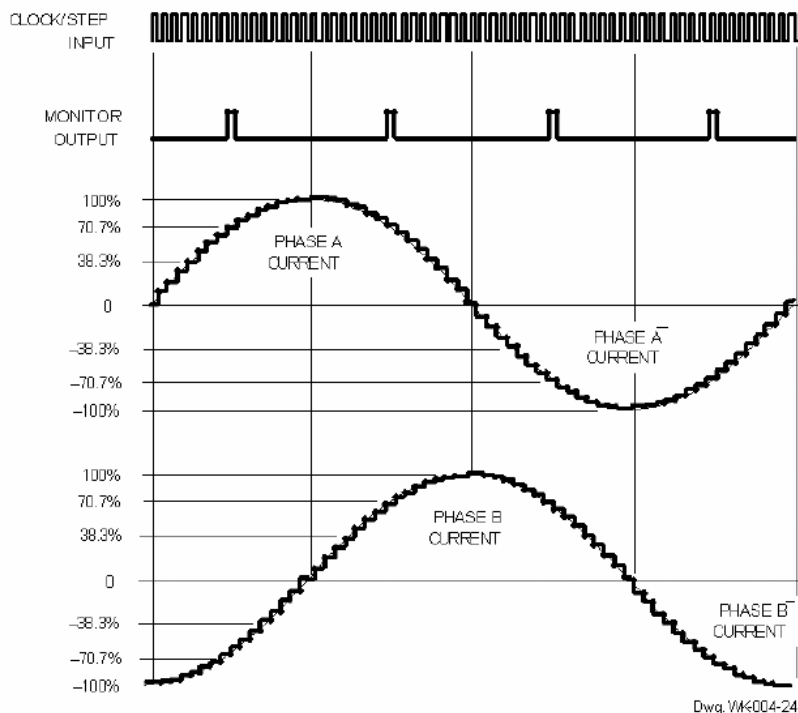
Quarter-step output current waveshapes. For illustrative purposes, phase A\ or B\ current (unipolar drive) is shown as negative current.

SLA7060M/7061M/7062M

October 2005



Eighth-step output current waveshapes. For illustrative purposes, phase A\ or B\ current (unipolar drive) is shown as negative current.



Sixteenth-step output current waveshapes. For illustrative purposes, phase A\ or B\ current (unipolar drive) is shown as negative current.

SLA7060M/7061M/7062M

October 2005

Applications information

Layout.

The printed wiring board should use a heavy ground plane.

For optimum electrical and thermal performance, the driver should be soldered directly into the board.

The driver supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (>47 μF is recommended) placed as close to the device as possible.

To avoid problems due to capacitive coupling of the high dv/dt switching transients, route the high-level, output traces away from the sensitive, low-level logic traces. Always drive the logic inputs with a low source impedance to increase noise immunity.

Grounding. A star ground system located close to the driver is recommended. The logic supply return and the driver supply return should be connected together at only a single point — the star ground.

Logic supply voltage, V_{DD}. Transients at this terminal should be held to less than 0.5 V to avoid malfunctioning operation. Both V_{BB} and V_{DD} may be turned on or off separately.

Logic inputs. Unused logic inputs (CW/CCW, M1, M2, RESET, or SYNC) must be connected to either ground or the logic supply voltage.

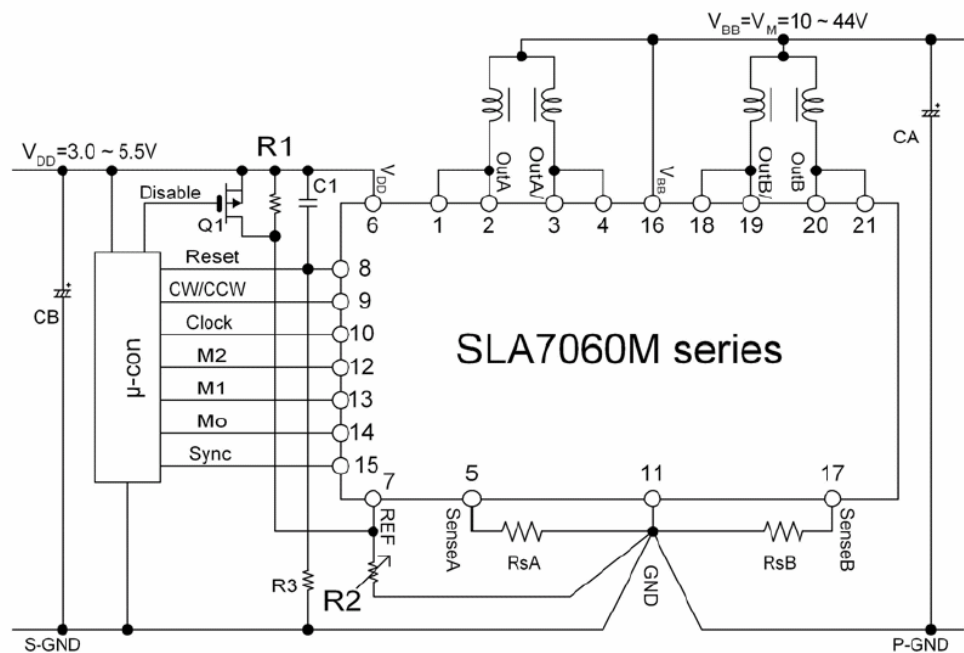
Current sensing. To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistors, R_S, should have an independent ground return to the star ground of the device. This path should be as short as possible. For low-value sense resistors, the IR drops in the printed wiring board sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

PWM current control. The maximum value of current limiting (I_{TRIP}) is set by the selection of R_S and the voltage at the REF input with a transconductance function approximated by:

$$I_{TRIP} = V_{REF} / R_S$$

The required V_{REF} should not be less than 0.1 V. If it is, R_S should be increased for a proportionate increase in V_{REF}.

- RS = 0.1 Ω to 2 Ω
- R1 = 10 kΩ
- R2 = 5.1 kΩ
- R3 = 10 kΩ
- CA = 100 μF, 50 V
- CB = 10 μF, 10 V
- C1 = 0.1 μF



SLA7060M/7061M/7062M

October 2005

Applications Information (cont'd)

Reference voltage. In the Typical Application shown, resistors R_1 and R_2 set the reference voltage as:

$$V_{REF} = (V_{DD} \times R_2) / (R_1 + R_2)$$

The trimming of R_2 allows for the resistor tolerances and REF input current. The sum of $R_1 + R_2$ should be less than 50 k Ω to minimize the effect of I_{REF} . Raising V_{REF} above 2 V by activating Q1 causes the sleep mode.

Minimum output current. The Series SLA7060M uses fixed off-time PWM current control. Due to internal logic and switching delays, the actual load current peak will be slightly higher than the calculated I_{TRIP} value (especially for low-inductance loads). These delays, plus the minimum recommended V_{REF} , limit the minimum value the current-control circuitry can regulate. An application with this device should maintain continuous PWM control in order to obtain optimum torque out of the motor. The boundary of the load current ($I_{O(min)}$) between continuous and discontinuous operation is:

$$I_{O(min)} = [(V_M + V_{SD}) / R_m] \times [(1 / e^{t_{off} / (R_m \times L_m)}) - 1]$$

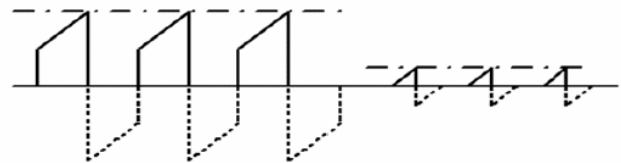
- where V_M = load supply voltage
- V_F = body diode forward voltage
- R_m = motor winding resistance
- t_{off} = PWM off time
- L_m = motor winding inductance

To produce zero current in a motor, the REF input should be pulled above 2 V, turning off all drivers.

Synchronous operation mode. If an external signal is not available to control the synchronous operation mode, a simple circuit can keep the SYNC input low while the CLOCK input is active; the SYNC input will go high (synchronous operation) when the CLOCK input stays low ("hold"). The RC time constant determines the sync transition timing.

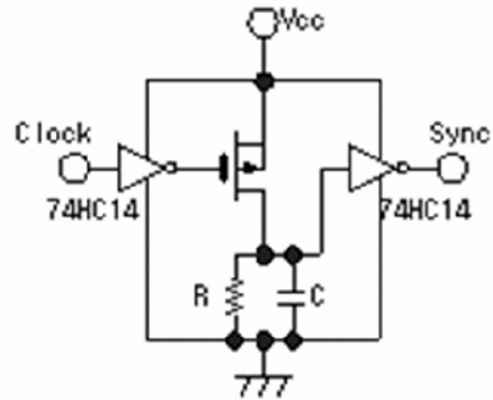
NOTE –The use of this function except at 0, 70.7, or 100% $I_{trip, max}$ (half-step positions 0 through 8) is not recommended.

Temperature effects on FET outputs. Analyzing safe, reliable operation includes a concern for the relationship of NMOS on resistance to junction temperature. Device package power calculations must include the increase in on resistance (producing higher on voltages)

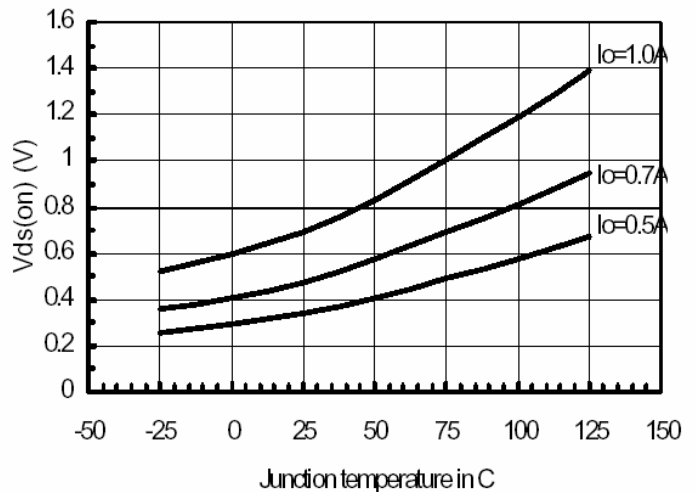


Continuous mode

Discontinuous mode



Sync. signal generator



Normalized FET on resistance

SLA7060M/7061M/7062M

October 2005

Applications Information (cont'd)

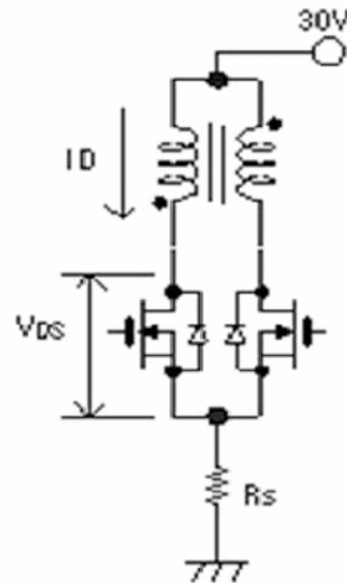
caused by increased operating junction temperatures. The figure provides a normalized on-resistance curve, and all thermal calculations should consider increases from the given +25°C limits, which may be caused by internal heating during normal operation.

These power MOSFET outputs feature an excellent combination of fast switching, ruggedized device design, low on resistance, and cost effectiveness.

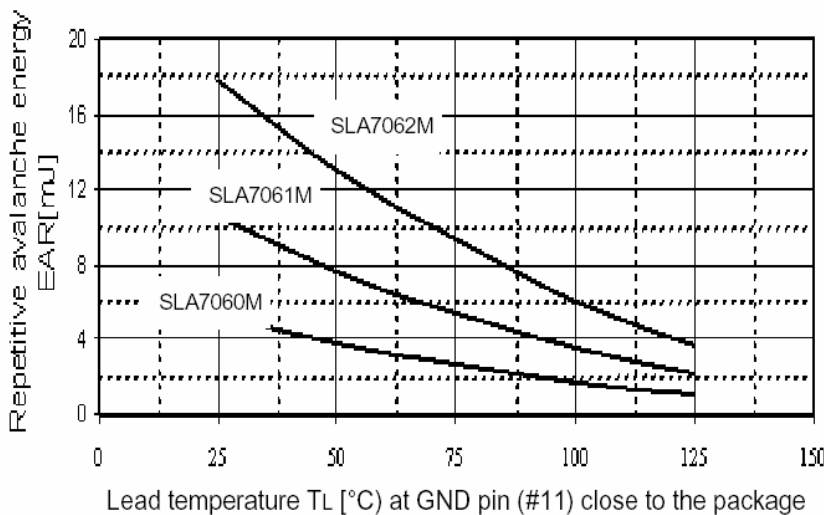
Avalanche energy capability. There is a surge voltage expected when the output MOSFET turns off, and this voltage may exceed the MOSFET breakdown voltage ($V_{(BR)DS}$). However, the MOSFETs are avalanche type and as long as the energy ($E_{(AV)}$), which is imposed on the MOSFET by the surge voltage, is less than the maximum allowable value, it is considered to be within its safe operating area. Note that the maximum allowable avalanche energy is reduced as a function of temperature.

In application, the avalanche energy ($E_{(AV)}$) dissipated by the MOSFET is approximated as

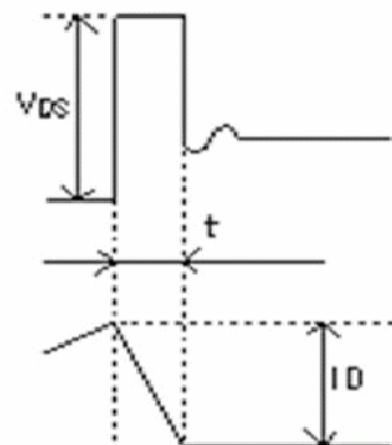
$$E_{(AV)} = V_{DS(AV)} \times 0.5 \times I_D \times t$$



Output circuit for avalanche energy calculations



Allowable avalanche energy



Waveforms during avalanche breakdown

SLA7060M/7061M/7062M

October 2005

Terminal list

Pin	Terminal Name	Terminal Description
1, 2	OUTA	Driver outputs for phase A
3, 4	OUTA\	Driver outputs for phase A\
5	SENSEA	Phase A current sense
6	VDD	Logic power supply, V_{DD}
7	REF	Current set & "sleep" control
8	RESET	Logic control input
9	CW/CCW	Forward/reverse logic control input
10	CLOCK	Step clock input
11	GND	Supply negative return
12	M2	Step mode logic control input
13	M1	Step mode logic control input
14	MO	Monitor logic output
15	SYNC	Synchronous PWM control input
16	VBB	Driver power supply, V_{BB}
17	SENSEB	Phase B current sense
18, 19	OUTB\	Driver outputs for phase B\
20, 21	OUTB	Driver outputs for phase B

The products described herein are manufactured in Japan by SanKen Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

Sanken and Allegro reserve the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Therefore, the user is cautioned to verify that the information in this publication is current before placing any order.

When using the products described herein, the applicability and suitability of such products for the intended purpose shall be reviewed at the users responsibility.

Although Sanken undertakes to enhance the quality and reliability of its products, the occurrence of failure and defect of semiconductor products at a certain rate is inevitable.

Users of Sanken products are requested to take, at their own risk, preventative measures including safety design of the equipment or systems against any possible injury, death, fires or damages to society due to device failure or malfunction.

Sanken products listed in this publication are designed and intended for use as components in general-purpose electronic equipment or apparatus (home appliances, office equipment, telecommunication equipment, measuring equipment, etc.). Their use in any application requiring radiation hardness assurance (e.g., aerospace equipment) is not supported.

When considering the use of Sanken products in applications where higher reliability is required (transportation equipment and its control systems or equipment, fire- or burglar-alarm systems, various safety devices, etc.), contact a sales representative to discuss and obtain written confirmation of your specifications.

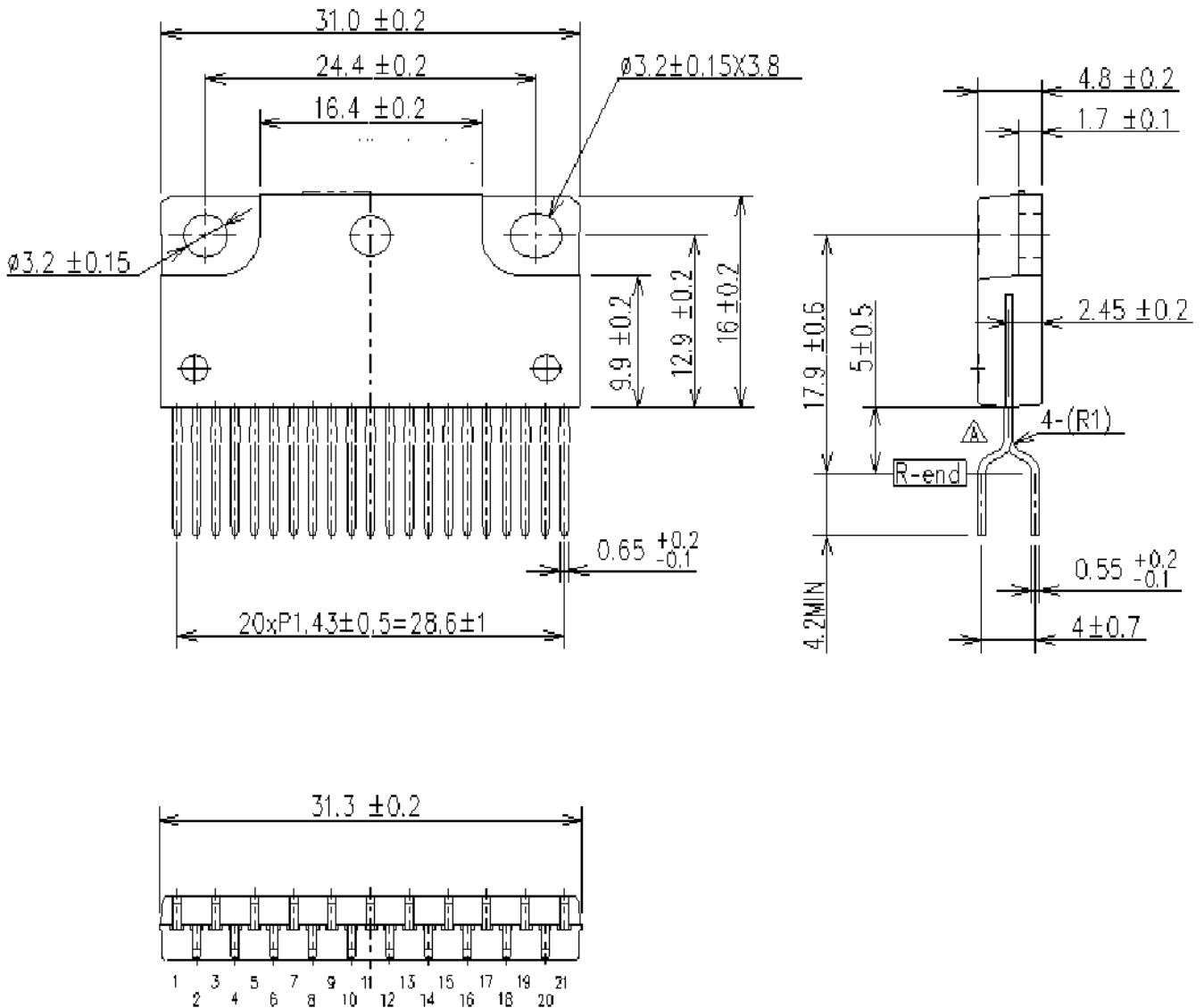
The use of Sanken products without the written consent of Sanken in applications where extremely high reliability is required (aerospace equipment, nuclear power-control stations, life-support systems, etc.) is strictly prohibited.

The information included herein is believed to be accurate and reliable. Application and operation examples described in this publication are given for reference only and Sanken and Allegro assume no responsibility for any infringement of industrial property rights, intellectual property rights, or any other rights of Sanken or Allegro or any third party that may result from its use.

SLA7060M/7061M/7062M

October 2005

SLA706xMLF2102
Dimensions in millimeters

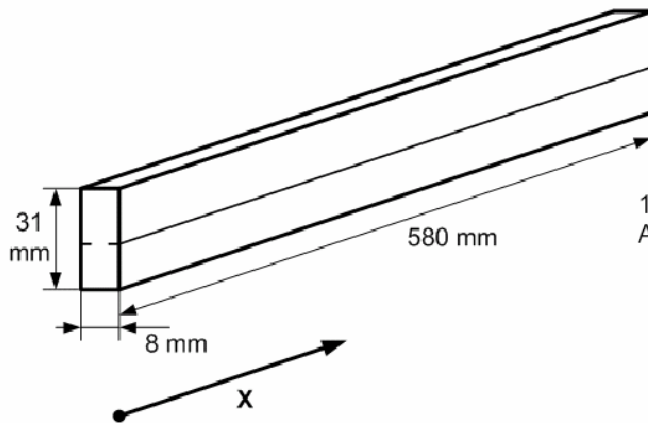


- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative.
 3. Recommended mounting hardware torque: 0.490 - 0.822 Nm.
 4. Recommended use of metal-oxide-filled, alkyl-degenerated oil-base silicone grease: Dow Corning SC102, Toshiba YG6260, Shin-Etsu G746, or equivalent.

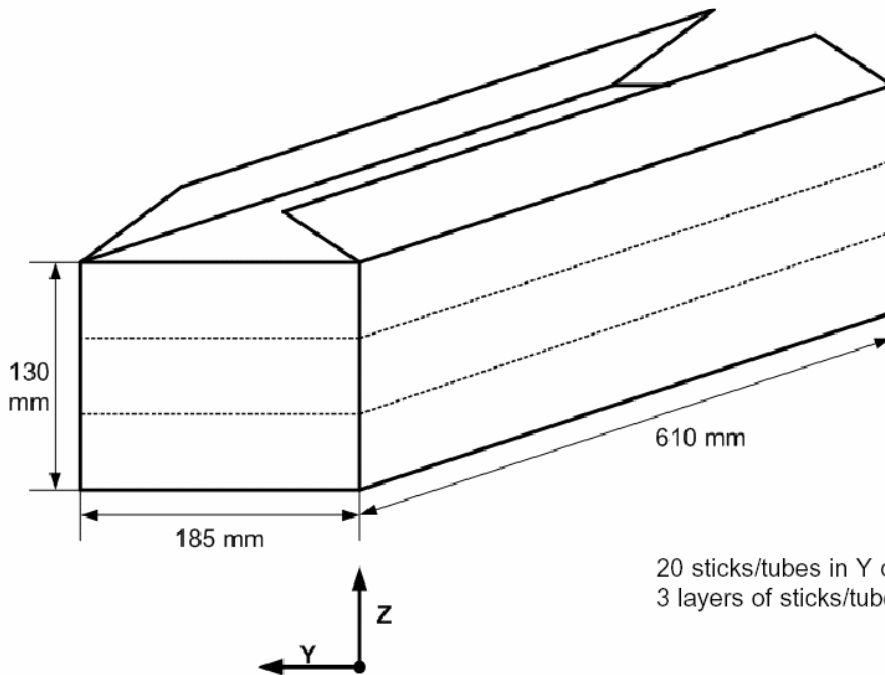
SLA7060M/7061M/7062M

October 2005

Packing information



18 devices per stick/tube.
A rubber stopper is provided at each end of the stick/tube.



20 sticks/tubes in Y direction;
3 layers of sticks/tubes in Z direction = 1080 devices per box.

SLA7060M/7061M/7062M

October 2005

<Worldwide Contacts>

Asia Pacific

China

Sanken Electric Hong Kong Co., Ltd.

Suite 1026 Ocean Centre, Canton Road, Tsimshatsui, Kowloon, Hong Kong

Tel: 852-2735-5262

Fax: 852-2735-5494

Sanken Electric (Shanghai) Co., Ltd.

Room3202, Maxdo Centre, Xingyi Road 8, Changning district, Shanghai, China

Tel: 86-21-5208-1177

Fax: 86-21-5208-1757

India

Saket Devices Pvt. Ltd.

Office No.25, 2nd Floor, Bandal - Dhankude Plaza, Near PMT Depot, Paud Road, Kothrud, Pune - 411 038, India

Tel: 91-20-5621-2340

Fax: 91-20-2528-5459

Japan

Sanken Electric Co., Ltd. Overseas Sales Headquarters

Metropolitan Plaza Bldg. 1-11-1 Nishi-Ikebukuro, Toshima-ku, Tokyo 171-0021, Japan

Tel: 81-3-3986-6164

Fax: 81-3-3986-8637

Korea

Sanken Electric Korea Co., Ltd.

Mirae Asset Life Bldg. 6F, 168 Kongduk-dong, Mapo-ku, Seoul, 121-705, Korea

Tel: 82-2-714-3700

Fax: 82-2-3272-2145

Singapore

Sanken Electric Singapore Pte. Ltd.

150 Beach Road, #14-03 The Gateway West, Singapore 189720

Tel: 65-6291-4755

Fax: 65-6297-1744

Taiwan

Taiwan Sanken Electric Co., Ltd.

Room 1801, 18th Floor, 88 Jung Shiau East Road, Sec. 2, Taipei 100, Taiwan R.O.C.

Tel: 886-2-2356-8161

Fax: 886-2-2356-8261

SLA7060M/7061M/7062M

October 2005

Europe

France

Allegro MicroSystems Europe

Les Pleiades, Park Nord Annecy, 74370 Metz-Tessy, France

Tel: 33-450512359

Fax: 33-450512083

United Kingdom

Allegro MicroSystems Europe Limited

Balfour House, Churchfield Road, Walton-on-Thames, Surrey KT12 2TD, U.K.

Tel: 44-1932-253355

Fax: 44-1932-246622

North America

United States

Allegro MicroSystems, Inc.

115 Northeast Cutoff, Worcester, Massachusetts 01606, U.S.A.

Tel: 1-508-853-5000

Fax: 1-508-853-3353

Allegro MicroSystems, Inc. (Southern California)

14 Hughes Street, Suite B105, Irvine, CA 92618

Tel: 1-949-460-2003

Fax: 1-949-460-7837