IMI4345

PHASE DETECTOR

INTERNATIONAL MICROCIRCUITS INC

PRODUCT FEATURES

- >40 MHz typical operating frequency
- 7 ns typical pulse width
- TTL level compatibility
- Linear digital phase detection
- Two error output options:
  Single-ended or Double-ended
- Lock detect signal
- Suitable for systems requiring ZERO phase-frequency difference at lock
- Low power consumption
- Packaging options include:
  – Plastic and Ceramic Dual-in-line
  – SOIC
  – Die for hydrid applications
- Grades available include: commercial, military operating range, and military screening

PRODUCT DESCRIPTION

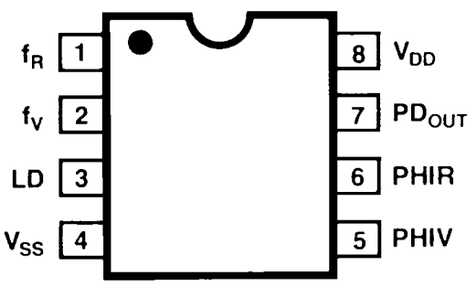
The IMI4345 is one of the family of LSI PLL frequency synthesizers offered by International Microcircuits. The device is a very fast CMOS digital phase detector, it compares phases of two input frequencies and output error signals which are linearly proportional to the phase difference. When used with prescalers, a loop filter and a VCO, the IMI4345 provides a very broad bandwidth frequency synthesizer.

APPLICATIONS

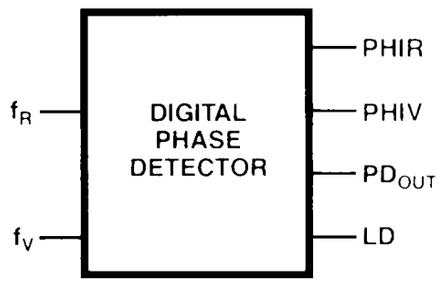
The phase detector can be used in general applications which require high performance phase detection such as: CATV, AM/FM Radio, TV Tuning and Scanning Receivers.

With its exceptional bandwidth it can also be used in Radar and Video applications.

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS

- DC Supply Voltage V_{DD} = −0.5 to +10V
- Input Voltage V_{IN} = −0.5 to V_{DD} +0.5V
- Input Current per pin I_{IN} = ±10 mA
- Storage Temperature T_{STG} = −65 to 150 °C

Maximum ratings are conditions beyond which damage to the device may occur (voltage referenced to V_{SS}).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range:

$$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic level (either V_{SS} or V_{DD}).

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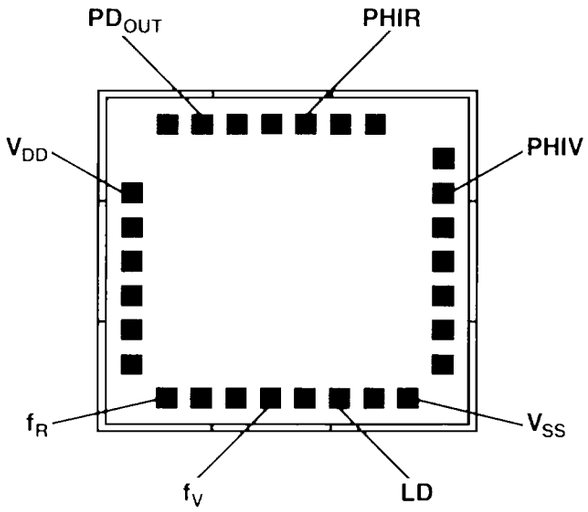
BONDING DIAGRAM



SWITCHING CHARACTERISTICS

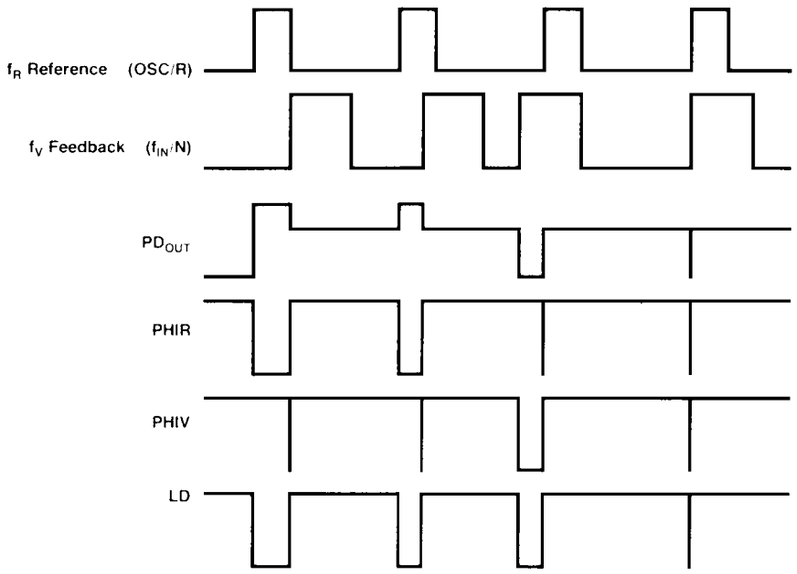
T_A = −55 to +125 °C
V_{DD} = 4.5 to 5.5V
C_L = 50pF

Characteristics	Symbol	Min.	Typ.	Max.	Units
Output Rise and Fall Time	t_R, t_F	—	10	20	nS
Output Pulse Width PHIR, PHIV with f_R in phase with f_V	t_{WO}	0	15	25	nS
Positive Clock Pulse Width	t_{WP}	25	15	—	nS
Negative Clock Pulse Width	t_{WN}	25	15	—	nS
Maximum Frequency	f_{MAX}	—	30	15	MHz

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	−55 to 125°C 4.5 to 5.5V		−40 to 85°C 4.75 to 5.25V		25°C 5V	Units
		Min.	Max.	Min.	Max.	Typ.	
Input Voltage	V_{IL}		0.8		0.8	1.2	V_{dc}
V_O = 0.4 or 2.4V	V_{IH}	2.2		2.0		1.6	
Output Current PHIR and PHIV only V_{OH} 2.4V	I_{OH}	6.0		7		8	mA
V_{OL} 0.4V	I_{OL}	6.0		7		8	
PD_{OUT} and LD only V_{OH} 2.4V	I_{OH}	3.0		3.5		4	
V_{OL} 0.4V	I_{OL}	3.0		3.5		4	
Input Current	I_{IN}		±10		±10	±0.1	μA
Input Capacitance	C_{IN}		10		10	6	pF
Output Capacitance	C_{OUT}		10		10	6	pF
3-State Leakage	I_L		±10		±3	±0.1	μA
Quiescent Current	IDD_{st}		10		10	1	μA
Dynamic Current at 20 MHz	IDD_{dyn}		50		50	30	mA

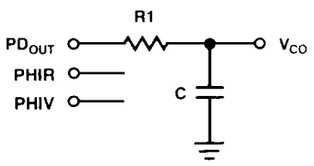
PHASE DETECTOR OUTPUT WAVEFORMS



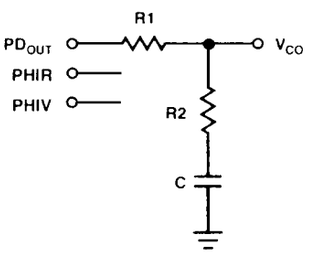
NOTE: The PD_{OUT} state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

PHASE LOCKED LOOP – LOW PASS FILTER DESIGN

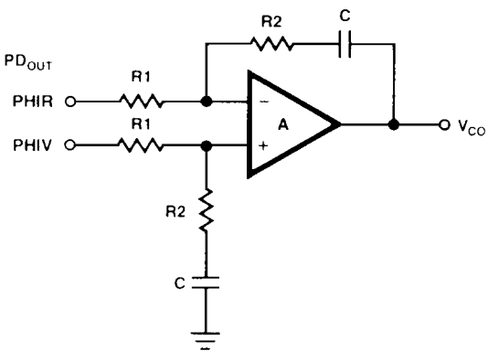
A)



B)



C)



$$\omega_N = \sqrt{\frac{K\phi K_{VCO}}{NR_1C}} \qquad \omega_N = \sqrt{\frac{K\phi K_{VCO}}{NC(R_1+R_2)}} \qquad \omega_N = \sqrt{\frac{K\phi K_{VCO}}{NCR_1}}$$

$$\xi = 1/2\omega_N(N/K\phi K_{VCO}) \qquad \xi = 1/2\omega_N(R_2C + N/K\phi K_{VCO}) \qquad \xi = \frac{\omega_N R_2C}{2}$$

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PHASE LOCKED LOOP – LOW PASS FILTER DESIGN

Continued from page 3

$$F(S) = \frac{1}{R_1CS+1} \qquad F(S) = \frac{R_2CS + 1}{S(R_1C+R_2C)+1}$$

Assuming gain A is very large, then:

$$F(S) = \frac{R_2CS + 1}{2}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor Cc is then placed from the midpoint to ground to further ϕV and ϕR. The value of Cc should be such that the corner frequency of this network does not significantly affect ω_N.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K\phi = V_{DD}/4\pi$ for PD_{OUT}

$K\phi = V_{DD}/2\pi$ for ϕV and ϕR

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_N \cong (2\pi/10)f_r$ (at phase detector input)

$\xi \cong 1$

ORDERING INFORMATION

Products are available from International Microcircuits in several packages and screening options. The Order Number is formed by a combination of device number, package pins, package style, and screening, as shown below.

IMI4345 008 P B CMOS DIGITAL PHASE DETECTOR

Grade

B = Commercial, −40° to +85° C
T = Military Operating Range, −55° to +125° C
K = Military Screening, −55° to +125° C
G = Commercial Visual (Die)
Q = Military Visual (Die)

Package

P = Plastic DIP
Q = Plastic J-Leaded Chip Carrier
X = Small Outline
S = Ceramic Side-Brazed Dual-In-Line
L = Ceramic Leadless Chip Carrier
D = Die

Package Pins

IMI Device Number