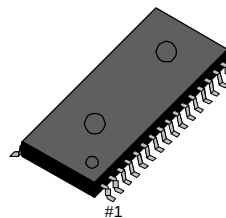


GENERAL DESCRIPTION

The S1A0501X01 is an audio processor for volume/tone/fader control, which is suitable for car radios or Hi-Fi system. It has a built-in trimmer for user to set a source level. R/L rear output is changable to input in the case of a home audio system for user conveniency, an external equalizer or a noise reduction circuit is selectable.

When the S1A0501X01 is used with some sound-effect equipment such as graphic equalizer, the internal tone control block of S1A0501X01 can be bypassed for decreasing redundancy. All selections and function controls are designed to be controlled by an I²C-bus protocol or a general microprocessor interface protocol.

32-SOP-450B



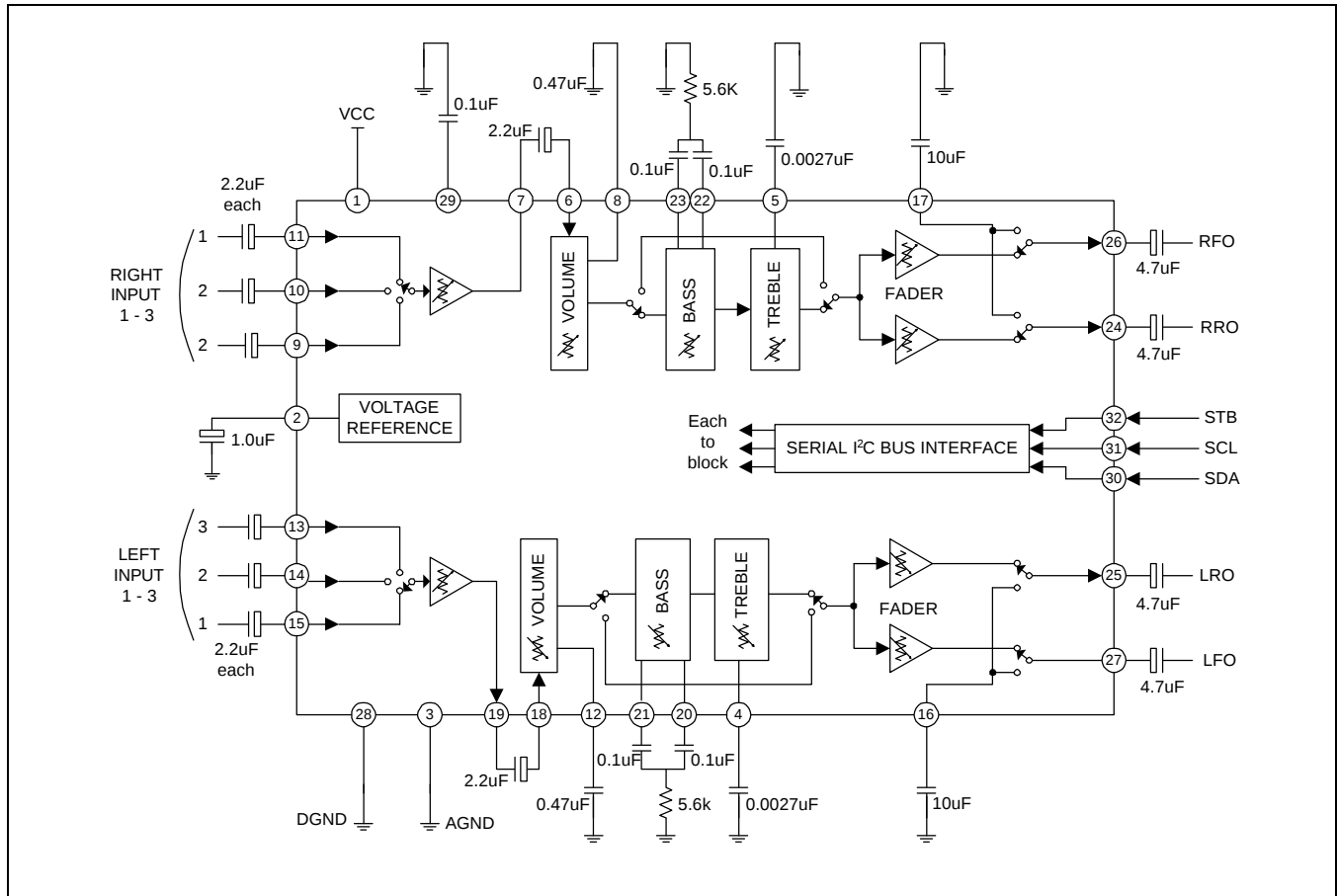
FEATURES

- 3-Input multiplexing
- Source Level trimmer (selectable input level)
- Volume control in 0.6dB step
- Tone control (internal bass/treble function block with external components)
- Source out / volume in (enable ext.graphic eq./ noise reduction equipment)
- Loudness / mute
- Fader control (separated for balance)
- All functions are programmable / controllable via serial I²C bus or general Micom interface protocol.

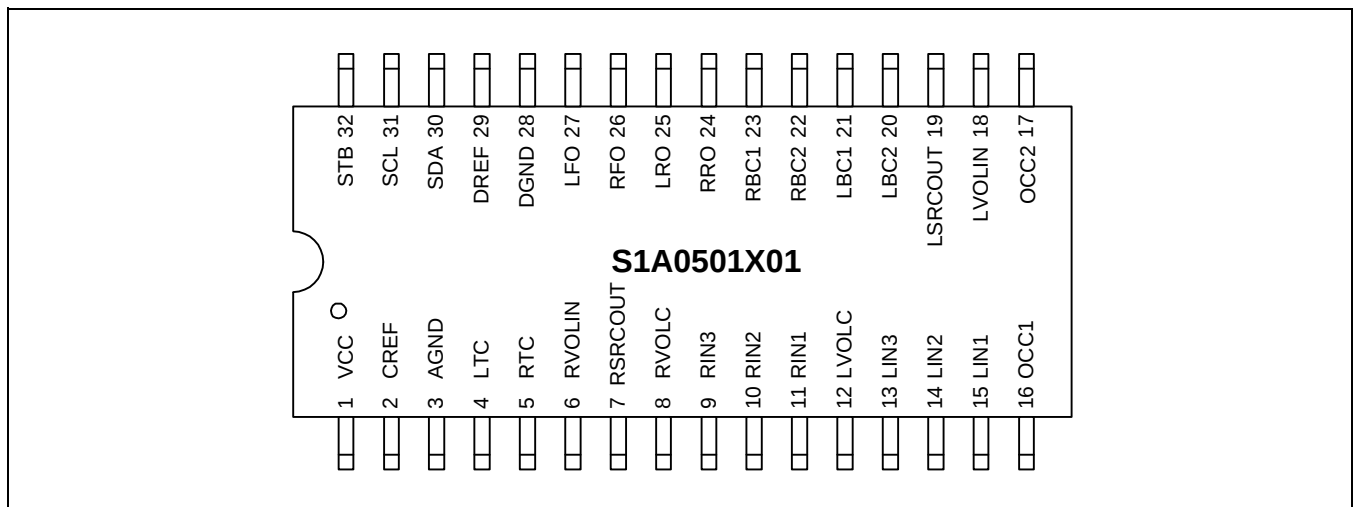
ORDERING INFORMATION

Device	Package	Operating Temperature
S1A0501X01-S0B0	32-SOP-450B	-25°C - +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbols	Description
1	VCC	Power Supply
2	CREF	Reference Voltage Ripple Rejection Capacitor Tab
3	AGND	Analog Ground (0V)
4	LTC	Left Treble Capacitor Tab
5	RTC	Right Treble Capacitor Tab
6	RVOLIN	Right Volume In / External Equalizer For Right Channel
7	RSRCOUT	Right Source Out / External Equalizer For Right Channel
8	RVOLC	Right Volume Loudness Capacitor Tab
9	RIN3	Right Audio Input3
10	RIN2	Right Audio Input2
11	RIN1	Right Audio Input1
12	LVOLC	Left Volume Loudness Capacitor Tab
13	LIN3	Left Audio Input3
14	LIN2	Left Audio Input2
15	LIN1	Left Audio Input1
16	OCC1	Offset Cancelling Capacitor Tab1
17	OCC2	Offset Cancelling Capacitor Tab2
18	LVOLIN	Left Volume In / External Equalizer For Left Channel
19	LSRCOUT	Left Source Out / External Equalizer For Left Channel
20	LBC2	Left Bass Capacitor Tab2
21	LBC1	Left Bass Capacitor Tab1
22	RBC2	Right Bass Capacitor Tab2
23	RBC1	Right Bass Capacitor Tab1
24	RRO	Right Rear Audio Output
25	LRO	Left Rear Audio Output
26	RFO	Right Front Audio Output
27	LFO	Left Front Audio Output
28	DGND	Digital Ground (0V)
29	DREF	Internally-generated Digital Power Stabilization Capacitor Tab
30	SDA	Data Signal Input Of I ² C Bus
31	SCL	Clock Signal Input Of I ² C Bus
32	STB	Strobe Signal Input

ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Value	Unit
Supply Voltage	VCCmax	15.0	V
Max.Power Dissipation	Pdmax	1000	mW
Max.Operating Temperature	Topr	-25 to +75	
Max.Storage Temperature	Tstg	- 40 to +125	

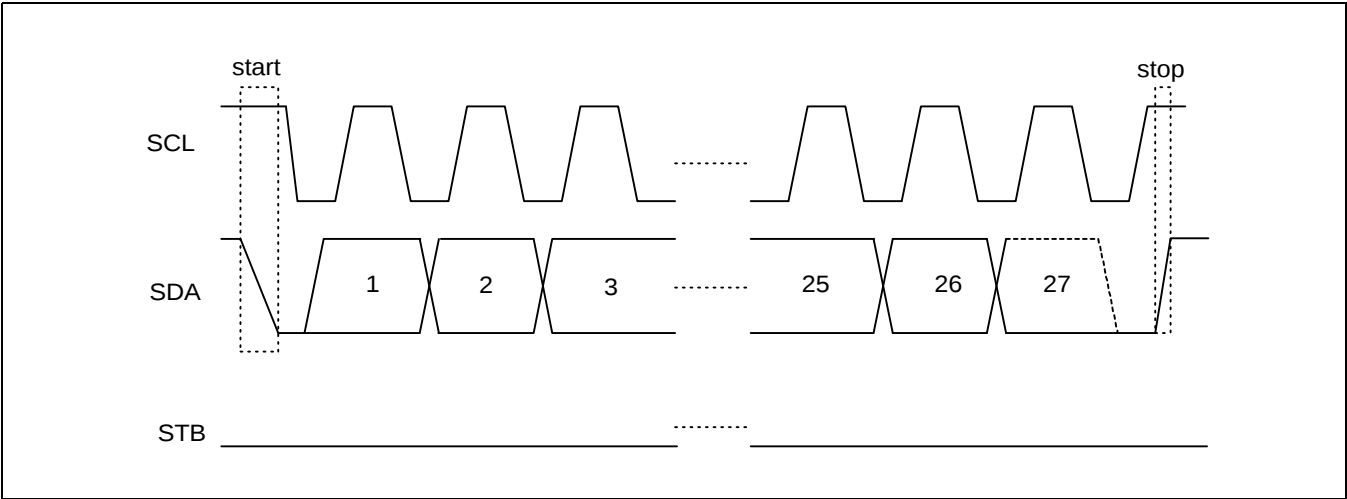
ELECTRICAL CHARACTERISTICS

Electrical Characteristics (Vi = 1Vrms/1kHz, Ta=25°C, VCC=13.2V TYP)

Parameters	Test Conditions	Specifications			Unit
		Min	Typ	Max	
Operating Voltage	-	6.0	-	15.0	V
Supply Current	Vi=0	6.0	10.0	14.0	mA
Input Dynamic	VCC=13.2V, Output T.H.D.=0.1%	6.0	-	-	Vp-p
Input Crosstalk	Vi=1Vrms,1kHz, 20Hz-20kHz BPF	-	-	-89.0	dB
Trimming Range	-	-5.4	-6.0	-	dB
Channel Crosstalk	Vi=1Vrms,1kHz, 20Hz-20kHz BPF	-	-	-89.0	dB
Channel Balance	Vi=1Vrms,1kHz	-2.0	-	2.0	dB
Voltage Gain	Vi=1Vrms,1kHz, Volume=Max	-2.0	0.0	2.0	dB
S/N Ratio	Vi=1Vrms,1kHz, 20Hz-20kHz BPF		-	92	dB
T.H.D.	Vi=1Vrms,1kHz, Volume=Max	-	0.005	0.01	%
Loudness Boost	Vi=1Vrms,100Hz	0.2	-	10.5	dB
Max.Volume attenuation	Vi=1Vrms,1kHz, Volume=Min		-76.2	-74.2	dB
Bass Control Range	Vi=1Vrms,100Hz, Bass= Min/Max	-14	-	14	dB
Treble Control Range	Vi=1Vrms,10kHz, Treble= Min/Max	-12	-	12	dB
Front/Rear Balance	Vi=1Vrms,1kHz, Fader= Middle	-	-	1.0	dB
Front/Rear Control Range	Vi=1Vrms,1kHz, Fader= Min	-	-	-38.75	dB
Frequency Response	-3dB	20	-	20000	Hz
Mute Attenuation	Vi=1Vrms,1kHz, 20Hz-20kHz BPF	-100	-	-90	dB

SERIAL BUS INTERFACE PROTOCOL - THE I²C BUS

Timing Diagram of I²C Bus Protocol



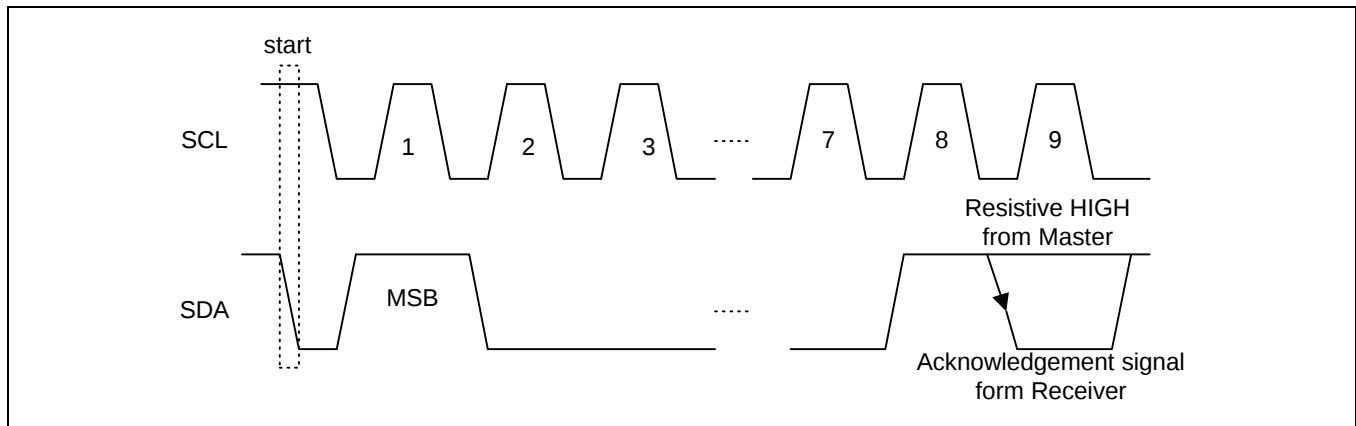
I²C Bus Byte Format of S1A0501X01

Start	1 - 8	9	10 - 17	18	19 - 26	27	Stop
S	Slave Address	ACK	Sub Address	ACK	DATA	ACK	P

- S = A start Condition
- Slave Address = Chip Address (10000000B)
- ACK = Acknowledge (from Slave)
- Sub Address = Transferred Data1 (assigning Function)
- DATA = Transferred Data2 (assigning Operation)
- P = A Stop Condition

STB Signal 'LOW' '= Always 'LOW' when I²C Bus protocol (tied to 'GND').

♣ Max.SCL Frequency 200kHz

Acknowledge on the I²C Bus Interface Protocol

Software Specification of S1A0501X01

<< Byte Organization - I²C Bus Transmission >>

FUNCTIONS		SUB Address	DATA BYTE								REMARKS	
			MSB	B6	B5	B4	B3	B2	B1	LSB		
Input Control	Select	0 0 0 X X X X X	SSEL SSEL X X X 1 0									
	Trimmer Set		STS1 STS0 X X X									
	Loudness		SLD X X X									
Volume Control	Fine	0 0 1 X X X X X	SVF3 SVF2 SVF1 SVF0 X									
	Coarse		SVC2 SVC1 SVC0 X									
Tone Control	Bass	0 1 0 X X X X X	SB3 SB2 SB1 SB0								SB3 , ST3 : OOST / CUT	
	Treble		ST3 ST2 ST1 ST0									
Fader Control	Left Front	0 1 1 X X X X X										
	Left Rear	1 0 0 X X X X X										
	Right Front	1 0 1 X X X X X	SF4	SF3	SF2	SF1	SF0	X	X	X		
	Right Rear	1 1 0 X X X X X										
Misc. Control	Rearin Con	1 1 1 X X X X X	SRIC				X	X	X	X	SET 'HIGH'	
	MUTE		SMUT E				X	X	X	X		X
	EXT.EQ		SEQ				X	X	X	X		X

cf> 'Rearin Control' of MISC.CONTROL is a **NOT-supported** function in present version of S1A0501X01.

So this bit should be always **'HIGH'** when transferring control data.

SOFTWARE SPECIFICATION

— Input Select / Trimmer Setting / Loudness Control

FUNCTION	SUBADDRESS	DATA BYTE									VALUE	REMARK	
Input Select	BYTE FORMAT									INPUT1 INPUT2 INPUT3 *INPUT4	Not Used		
	b7	b6	b5	b7	b6	b5	b4	b3	b2			b1	b0
	0 0 0			0 0 X X X									
				0 1 X X X									
				1 0 X X X									
				1 1 X X X									
Trimmer Setting				0 0 X X X						0 dB	2 dB STEP (4)		
				0 1 X X X						- 2 dB			
				1 0 X X X						- 4 dB			
				1 1 X X X						- 6 dB			
Loudness				0 X X X						ON			
				1 X X X						OFF			

SOFTWARE SPECIFICATION - Tone Control : Bass boost/cut1

FUNCTION	SUBADDRESS	DATA BYTE								VALUE	REMARK
Bass Control	0 1 0	BYTE FORMAT									2 dB STEP
		b7	b6	b5	b4	b3	b2	b1	b0		
						0	0	0	0		
						0	0	0	1		
						0	0	1	0		
						0	0	1	1		
						0	1	0	0		
						0	1	0	1		
						0	1	1	0		
						0	1	1	1		
						1	1	1	1		
						1	1	1	0		
						1	1	0	1		
						1	1	0	0		
						1	0	1	1		
						1	0	1	0		
						1	0	0	1		
						1	0	0	0		

SOFTWARE SPECIFICATION - Tone Control : Treble boost/cut

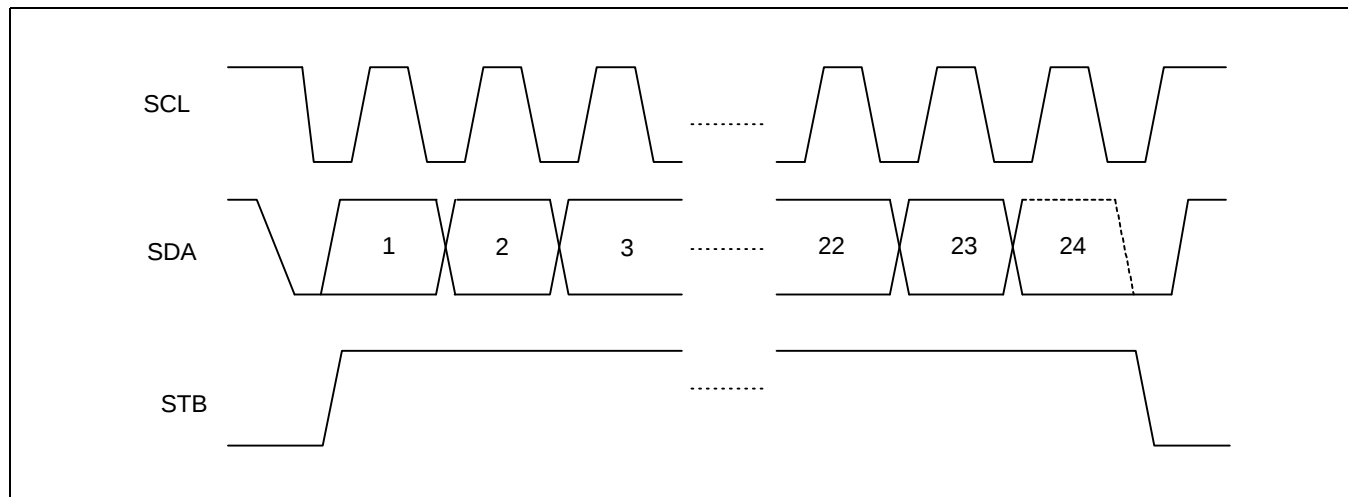
FUNCTION	SUBADDRESS	DATA BYTE								VALUE	REMARK
Treble Control	0 1 0	BYTE FORMAT									1.7 dB STEP
		b7	b6	b5	b4	b3	b2	b1	b0		
		0	0	0	0						
		0	0	0	1						
		0	0	1	0						
		0	0	1	1						
		0	1	0	0						
		0	1	0	1						
		0	1	1	0						
		0	1	1	1						
		1	1	1	1						
		1	1	1	0						
		1	1	0	1						
		1	1	0	0						
		1	0	1	1						
		1	0	1	0						
		1	0	0	1						
		1	0	0	0						

SOFTWARE SPECIFICATION - Fader / Miscellaneous Control DATA BYTE BYTE FORMAT

FUNCTION	SUBADDRESS	DATA BYTE								VALUE	REMARK
Fader Control	b7 b6 b5 0 1 1 1 0 0 1 0 1 1 1 0	BYTE FORMAT								Left Front Left Rear Right front Right Rear	
		b7	b6	b5	b4	b3	b2	b1	b0		
				0	0	0	X	X	X	0 dB	
				0	0	1	X	X	X	- 1.25 dB	
				0	1	0	X	X	X	- 2.5 dB	
				0	1	1	X	X	X	- 3.75 dB	
				1	0	0	X	X	X	- 5.0 dB	
				1	0	1	X	X	X	- 6.25 dB	
				1	1	0	X	X	X	- 7.5 dB	
				1	1	1	X	X	X	- 8.75 dB	
		0	0				X	X	X	0 dB	
		0	1				X	X	X	- 10 dB	
		1	0				X	X	X	- 20 dB	
		1	1				X	X	X	- 30 dB	
Rear-in Control	1 1 1			0	X	X	X	X	X	ENABLE	Should Be 'DISABLE'
				1	X	X	X	X	X	DISABLE	
Mute			0		X	X	X	X	X	ON	
			1		X	X	X	X	X	OFF	
External Equalizer		0			X	X	X	X	X	ENABLE	
		1			X	X	X	X	X	DISABLE	

SERIAL BUS INTERFACE PROTOCOL - THE GENERAL CASE

Timing Diagram of General MICOM Interface Bus Protocol



General MICOM Interface Bus Byte Format Of S1A0501X01

Bit Stream	1 - 7	8	9 - 16	17 - 24
Meanings	Chip Select Code		Function Code	DATA

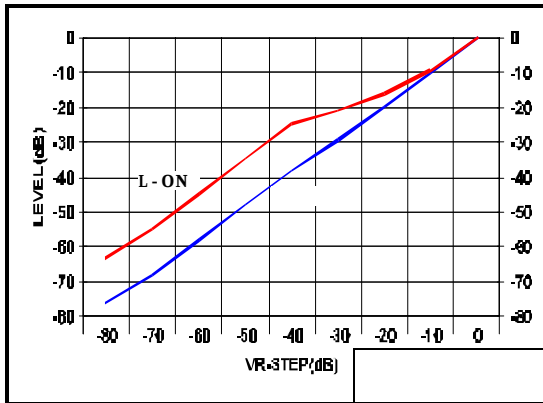
Chip Select Code = Same As I²C Bus Slave Address (1000000 × B)
 X = Don't Care Bit (Not Used Bit)
 Function Code = Transferred Data1 (assigning Function)
 DATA = Transferred Data2 (assigning Operation)
 STB Signal 'LOW' = Chip Not Selected.
 STB Signal 'HIGH' = Chip Selected.

♣ Allowed Strobe Pulse Width (Maximum) ≤ 6.0ms

Volume Step vs output Level

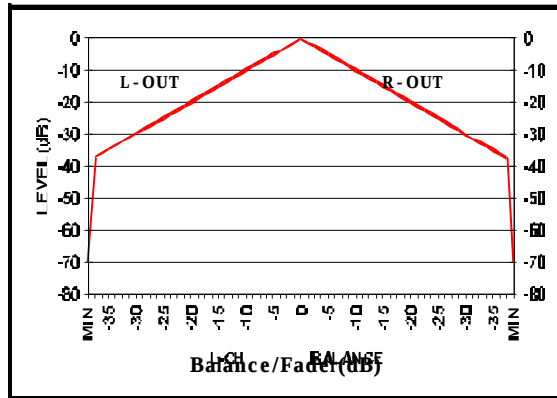
Input :1Vrms

Vcc=12V

**Balance & Fader Step vs output Level**

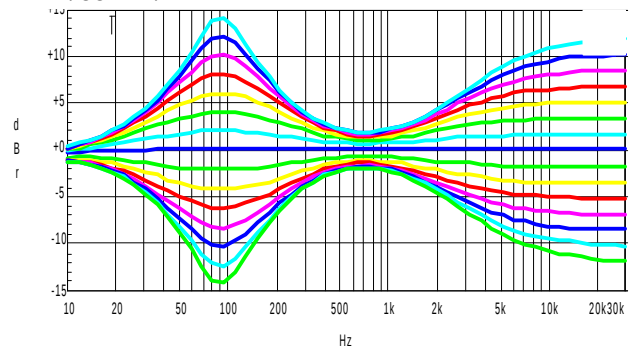
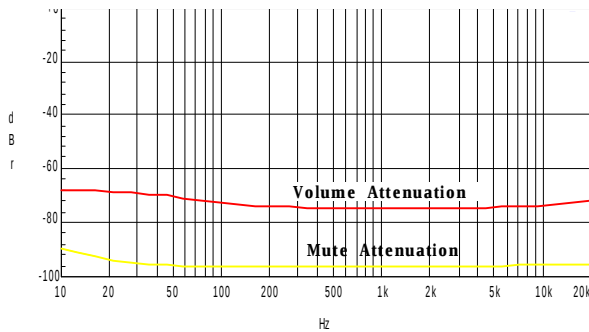
Input :1Vrms

Vcc=12V

**Bass & Treble Boost / Cut**

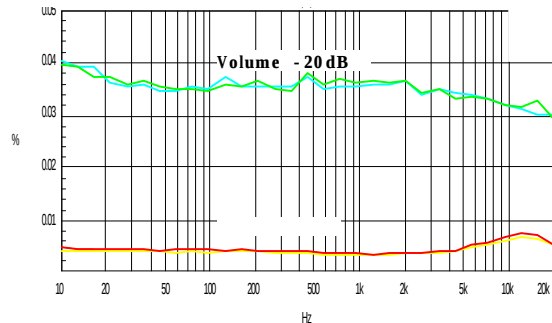
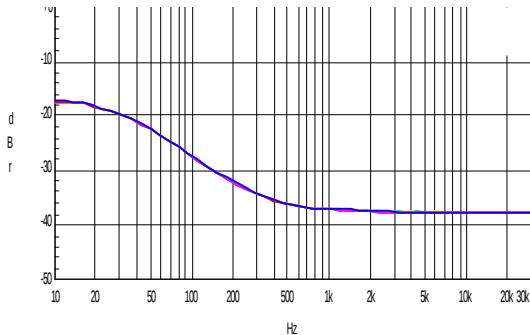
Input : 300mVrms, Volume=Max

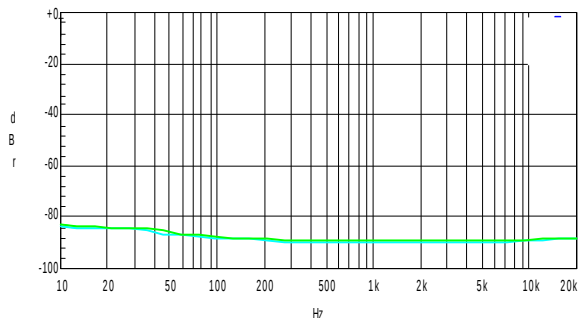
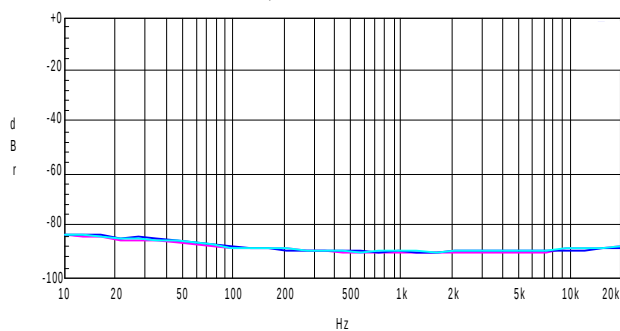
Vcc=12V

**Loudness Boost**

Input : 300mVrms, Volume=-37.8dB

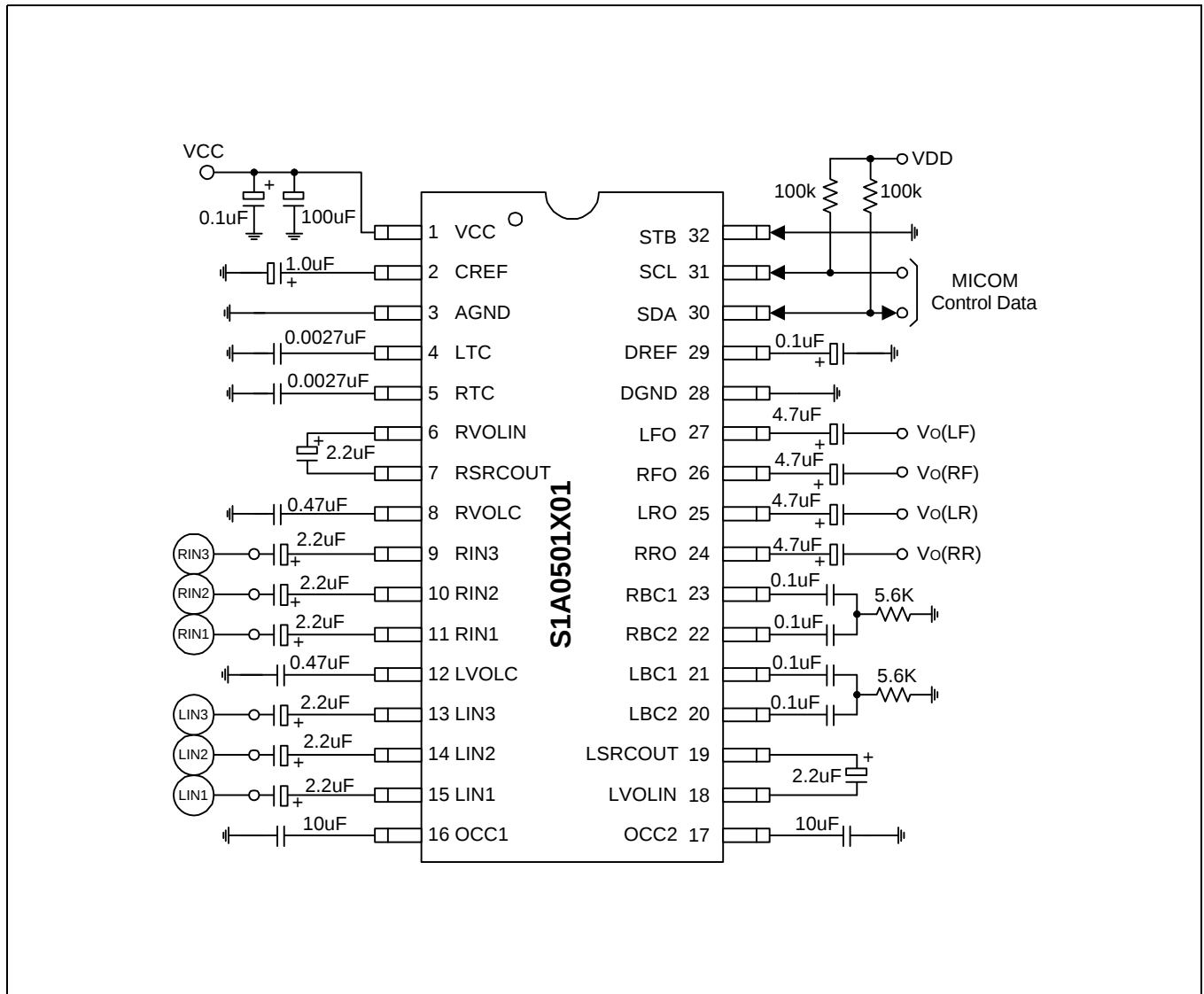
Vcc=12V



Input CrossTalk**Selected Input : 1Vrms, Otherwise : Short****Vcc=12V****L/R Channel Separation****Selected Channel Input :1Vrms****The Other : Short, Vcc=12V**

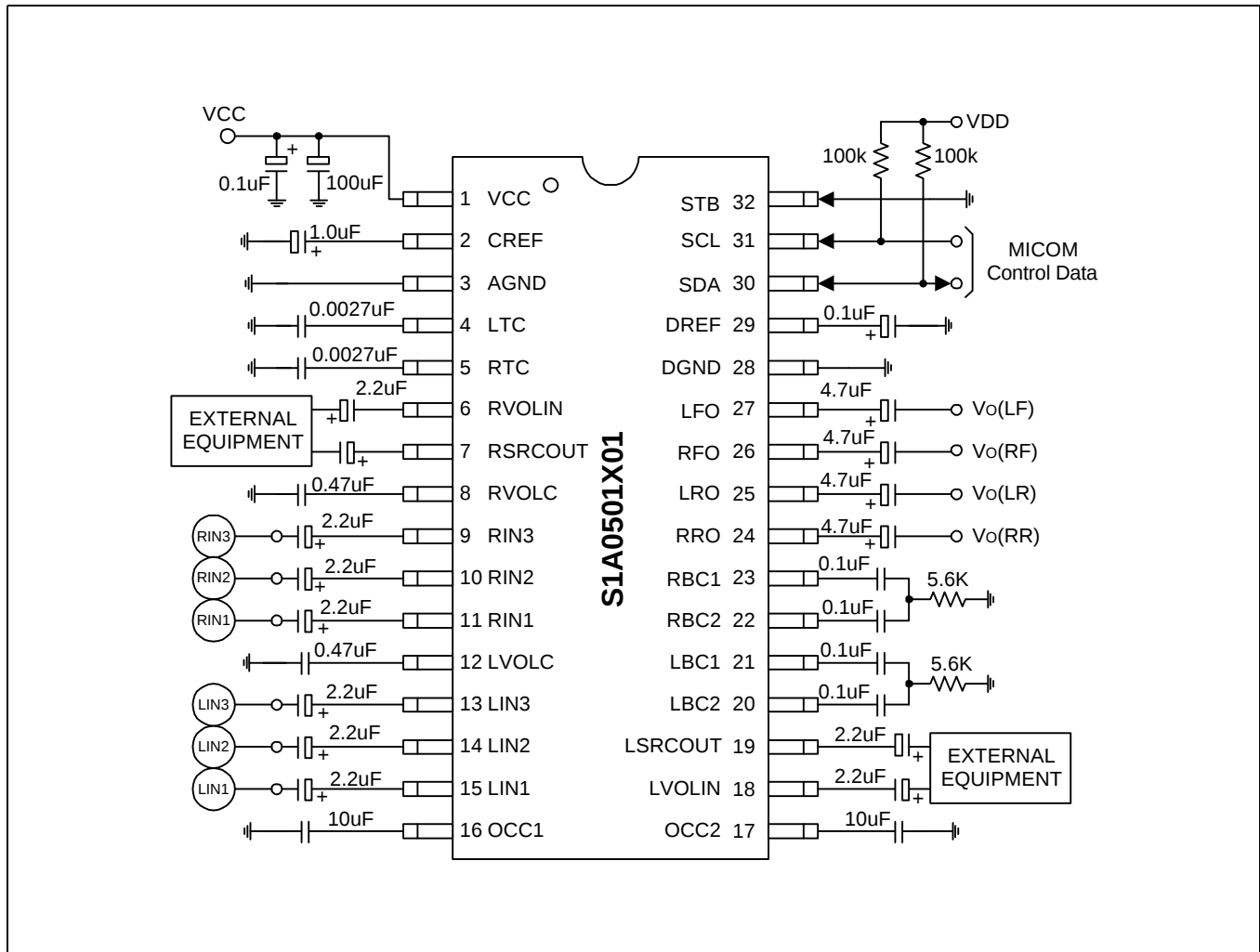
APPLICATION CIRCUIT 1

MODE I : 3 INPUTS - 1 OUTPUT



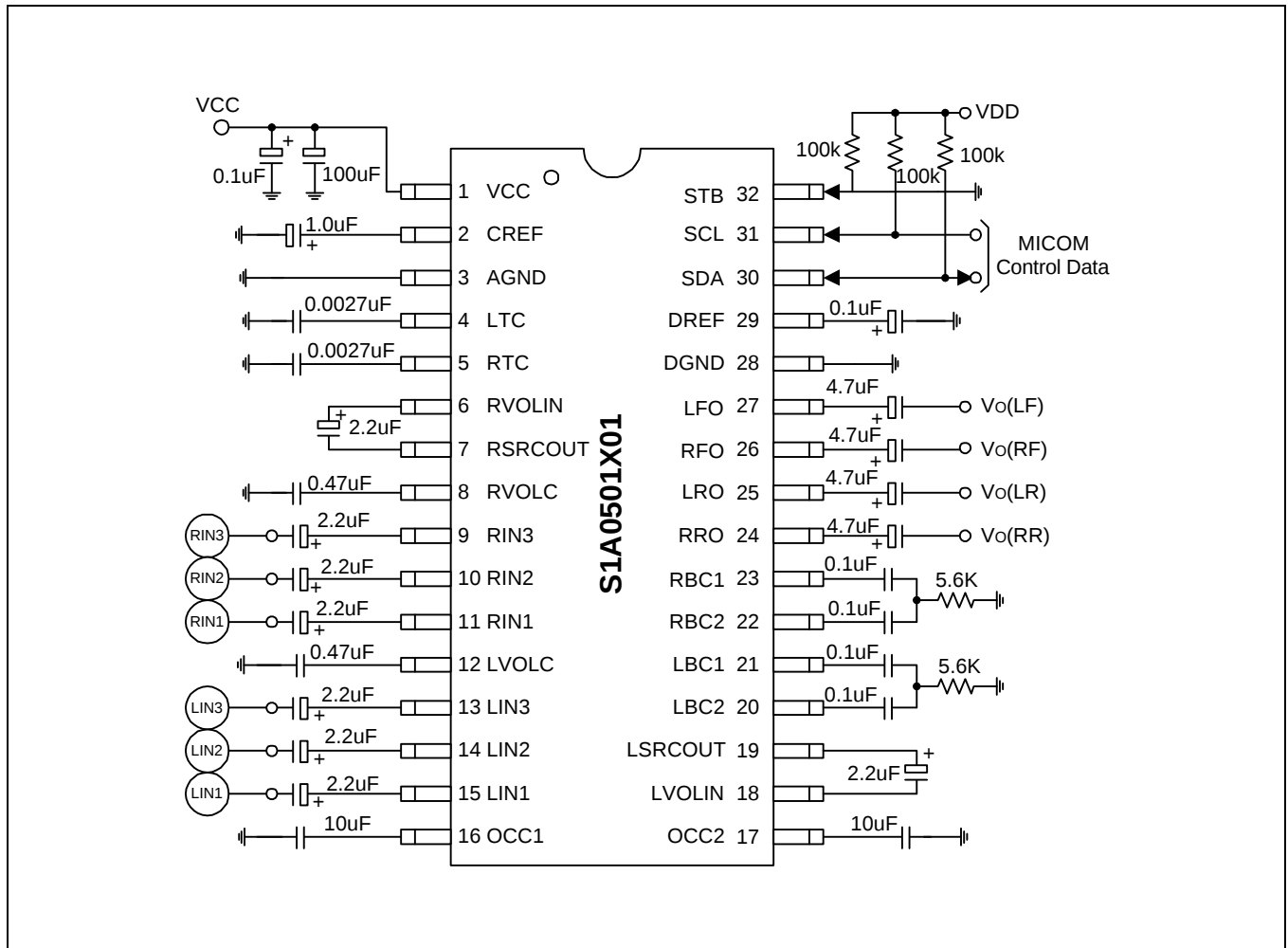
APPLICATION CIRCUIT 2

MODE II : 3 INPUTS - 1 OUTPUT W/ EXT.EQUIPMENT



Cf> Let the microprocessor set 'SEQ' signal to 0, if an external device is an audio-signal controlled processor such as a graphic equalizer.

APPLICATION CIRCUIT 3

MODE III : 3 INPUTS - 1 OUTPUT (NOT I²C BUS PROTOCOL)

NOTES