



Integrated Device Technology Inc.

# FAST CMOS EEPROM 16K (2K x 8-BIT)

IDT78C16A

### FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 75ns (max.)
  - Commercial: 70ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- DATA Polling – detection of write cycle completion
- Low-power CEMOS™ technology
  - 125mA active current
  - 0.9mA standby current (full CMOS)
- Data protection circuitry (V<sub>CC</sub> lockout for V<sub>CC</sub> < 3.8V) provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- JEDEC approved byte-wide pinout
- 24-pin THINDIP (300 mil.), 24-pin DIP (600 mil.) and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

### DESCRIPTION:

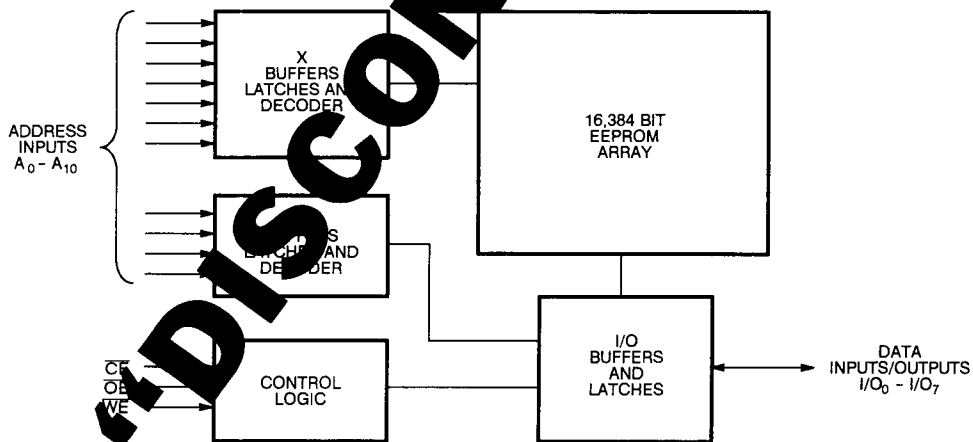
The IDT78C16A is a 5 volt only 2K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM). This high-speed CEMOS™ EEPROM is written on a byte basis and provides 16,384 bits of non-volatile data storage (data retention in excess of 100 years). Its fast read access time allows zero wait state read cycles with high-performance microprocessors.

Writing is simplified using internal charge-pump and timer circuit which eliminates the need for special external programming voltage and write pulse shaping circuits. Byte erase before write occurs automatically and input buffers, latches and internal timer free the host system of most tasks during the write cycle. A DATA Polling mode provides a method for determining write cycle completion. The IDT78C16A also contains a dual voltage detection logic circuit which allows the device to be used in older applications which do not require external programming circuits.

The IDT78C16A is function- and pinout-compatible with the IDT6116, a 2K x 8 static RAM. It is ideal for systems requiring non-volatile system data modifications.

This military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B, making it ideally suited to high temperature applications demanding the highest level of performance and reliability.

### FUNCTIONAL BLOCK DIAGRAM



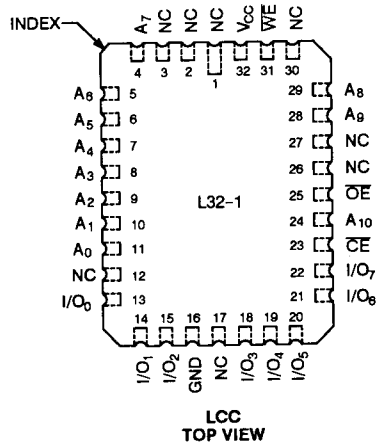
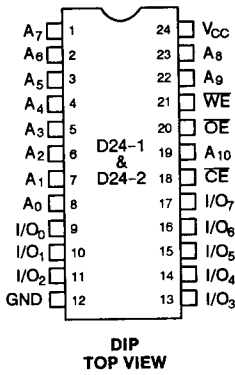
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

DECEMBER 1987

**PIN CONFIGURATIONS**



**PIN NAMES**

A <sub>0</sub> - A <sub>3</sub>	Addresses-Column
A <sub>4</sub> - A <sub>10</sub>	Addresses-Row
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O <sub>0</sub> - I/O <sub>7</sub>	Data Input (I <sub>0</sub> - I <sub>7</sub> ) during write; Data Output (O <sub>0</sub> - O <sub>7</sub> ) during read
V <sub>CC</sub>	Power
GND	Ground

## DEVICE OPERATIONAL MODE <sup>(1)</sup>

MODE	PIN			I/O <sub>0</sub> - I/O <sub>7</sub>
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Data <sub>OUT</sub> (O <sub>0</sub> - O <sub>7</sub> )
Byte Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Data <sub>IN</sub> (I <sub>0</sub> - I <sub>7</sub> )
Standby	V <sub>IH</sub>	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V <sub>IL</sub>	Don't Care	High Z
	Don't Care	Don't Care	V <sub>IH</sub>	High Z

### NOTE:

- All control inputs are TTL-compatible.

## READ MODE

Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) must be logically active in order for data to be available at the outputs. After a selected byte address is stable,  $\overline{CE}$  is taken to a TTL LOW (enabling chip). The Write Enable ( $\overline{WE}$ ) pin should remain deselected (TTL HIGH) during the entire read cycle. Data is gated from the device outputs by selecting the  $\overline{OE}$  pin (TTL LOW).

## WRITE MODE

The IDT78C16A is programmed electrically in-circuit and does not require any external latching, erasing or timing. Writing to the IDT78C16A is as easy as writing to a static RAM. When a write cycle is initiated, the device automatically latches the address, data and control signals as it begins its write operation.

A write cycle is initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The IDT78C16A supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. All inputs, except for data, are latched on the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Data is then latched in by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurred first. An automatic byte erase of the existing data at the addressed location is performed before the new data byte is written. Once initiated, a byte write operation will automatically proceed to completion within 10ms.

## STANDBY MODE

The IDT78C16A features a standby mode which reduces the maximum active current from 125mA to 20mA for TTL levels and to 0.9mA for CMOS levels. With  $\overline{CE} \geq V_{IH}$  all outputs are in the high impedance state.

## DATA PROTECTION

Nonvolatile data is protected from inadvertent writes in the following manner:

### Power Up/Down

On-chip circuitry provides protection against false write during V<sub>CC</sub> power up/down. The IDT78C16A features an internal sensing circuit that disables the internal programming circuit if V<sub>CC</sub> < 3.8V. This prevents input signals at  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{OE}$  from triggering a write cycle during a V<sub>CC</sub> power up/down event.

## Noise Protection

The IDT78C16A will typically reject write pulses that are less than 15ns. This prevents spurious noise from initiating a write cycle.

## Write Inhibit

Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH or  $\overline{CE}$  HIGH during a power-on and power-off, will inhibit inadvertent writes.

## DATA Polling

The IDT78C16A has a maximum write cycle time of 10ms; a write will always be completed in less than the maximum cycle time. Write cycle completion is readily determined via a simple software routine (DATA Polling) that performs a read operation while the device is in an automatic write mode. If a read command (addressed to the last byte written) is given while the IDT78C16A is still writing, the inverse of the most significant bit (I/O<sub>7</sub> pin) of the last byte written will be present. True data is not released until the write cycle is completed. Thus, a  $\overline{DATA}$  polling monitor of the output (or periodic read of the last written byte) for true data can be used to detect early completion of a write cycle.

## ENDURANCE

IDT's EEPROM technology employs the Fowler-Nordheim method of tunneling across a thin oxide. IDT78C16A EEPROMs are designed and tested for applications requiring extended endurance.

The endurance failure mechanism associated with EEPROMs results from the charge trapping in the thin tunneling dielectric. This failure is a function of the number of write cycles that each byte in the part has experienced. Trapped charges accumulate slowly with each write cycle, eventually becoming large enough to prevent reliable writing to the bit cell. Since some bits may be more sensitive than others, an endurance failure is typically a single bit failure (i.e. a failure of a single bit to properly write or retain data).

To test for endurance, sample devices are written 10,000 times at every byte location and checked for data retention capability. IDT's tests ensure that shipped devices will write a minimum of 10,000 times (at every byte location) with a maximum failure rate of 1%. This means that up to 1% of a sample of devices will fail to write or retain data after being written to 10,000 times. Those devices that do fail typically have a single bit(s) that fails to retain data after being written.

For more detailed information please refer to the *IDT Reliability Report on Endurance*.

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ENDURANCE**

PARAMETER	VALUE	UNIT
Minimum Endurance	10,000	Cycles/Byte

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

GRADE	AMBIENT TEMPERATURE	GND	V <sub>CC</sub>
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

**RECOMMENDED DC OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	3.5	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	0.4	0.8	V
V <sub>WI</sub>	Write Inhibit	3.8	-	-	V

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0MHz, V<sub>CC</sub> = 5.0V)

SYMBOL	PARAMETER <sup>(1)</sup>	CONDITIONS	TYP.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**NOTE:**

- This parameter is sampled and not 100% tested.

**DC ELECTRICAL CHARACTERISTICS**

Following Conditions Apply Unless Otherwise Specified

- T<sub>A</sub> = 0°C to +70°C                      V<sub>CC</sub> = 5.0V ± 10% (Commercial)  
 T<sub>A</sub> = -55°C to +125°C                  V<sub>CC</sub> = 5.0V ± 10% (Military)  
 V<sub>LC</sub> = 0.2V                                  V<sub>HC</sub> = V<sub>CC</sub> - 0.2V  
 C<sub>L</sub> = 30pF

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
I <sub>I1</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	-	10	µA
I <sub>LO</sub>	Output Leakage Current	CE = V <sub>IH</sub> or OE = V <sub>IH</sub> , V <sub>I/O</sub> = GND to V <sub>CC</sub>	-	10	µA
I <sub>CC1</sub>	Operating Power Supply Current V <sub>CC</sub> = Max., f = 0	CE = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	125	mA
I <sub>CC2</sub>	Dynamic Operating Current V <sub>CC</sub> = Max., f = f <sub>MAX</sub>	CE = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	125	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL Level)	CE ≥ V <sub>IH</sub> , V <sub>CC</sub> = Max., I <sub>I/O</sub> = 0mA V <sub>IN</sub> ≥ V <sub>IH</sub> or 0 ≤ V <sub>IN</sub> ≤ V <sub>IL</sub>	-	20	mA
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level)	CE ≥ V <sub>HC</sub> , V <sub>CC</sub> = Max., I <sub>I/O</sub> = 0mA V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or 0 ≤ V <sub>IN</sub> ≤ 0.2V	-	0.9	mA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8mA	-	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2mA	2.4	-	V

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ ,  $C_L = 30pF$ ,  $0^\circ C$  to  $+70^\circ C$ )

SYMBOL	PARAMETER	COMMERCIAL $0^\circ C$ to $+70^\circ C$								UNIT		
		78C16A70		78C16A90/100		78C16A120		78C16A150			78C16A200	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
<b>READ CYCLE</b>												
$t_{CE}$	Chip Enable Access Time	—	70	—	90/100	—	120	—	150	—	200	ns
$t_{AA}$	Address Access Time	—	70	—	90/100	—	120	—	150	—	200	ns
$t_{OE}$	Output Enable to Output Valid	—	50	—	60/65	—	70	—	70	—	70	ns
$t_{CLZ}$	Chip Enable to Output in Low Z <sup>(1)</sup>	5	—	5	—	5	—	5	—	5	—	ns
$t_{OLZ}$	Output Enable to Output in Low Z <sup>(1)</sup>	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ}$	Chip Disable to Output in High Z <sup>(1)</sup>	0	20	0	20	0	20	0	20	0	20	ns
$t_{OHZ}$	Output Disable to Output in High Z <sup>(1)</sup>	0	20	0	20	0	20	0	20	0	20	ns
$t_{OH}$	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns

**NOTE:**

1. This parameter is guaranteed but not tested.

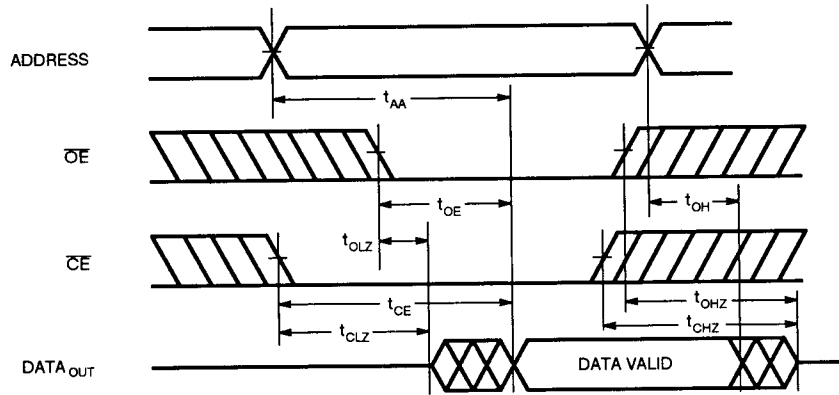
**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ ,  $C_L = 30pF$ ,  $-55^\circ C$  to  $+125^\circ C$ )

SYMBOL	PARAMETER	MILITARY $-55^\circ C$ to $+125^\circ C$										UNIT
		78C16A75		78C16A90/100		78C16A120/150		78C16A200/250		78C16A300/350		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
<b>READ CYCLE</b>												
$t_{CE}$	Chip Enable Access Time	—	75	—	90/100	—	120/150	—	200/250	—	300/350	ns
$t_{AA}$	Address Access Time	—	75	—	90/100	—	120/50	—	200/250	—	300/350	ns
$t_{OE}$	Output Enable to Output Valid	—	50	—	60/65	—	70	—	70	—	70	ns
$t_{CLZ}$	Chip Enable to Output in Low Z <sup>(1)</sup>	5	—	5	—	5	—	5	—	5	—	ns
$t_{OLZ}$	Output Enable to Output in Low Z <sup>(1)</sup>	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ}$	Chip Disable to Output in High Z <sup>(1)</sup>	0	30	0	30	0	30	0	30	0	30	ns
$t_{OHZ}$	Output Disable to Output in High Z <sup>(1)</sup>	0	30	0	30	0	30	0	30	0	30	ns
$t_{OH}$	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns

**NOTE:**

1. This parameter is guaranteed but not tested.

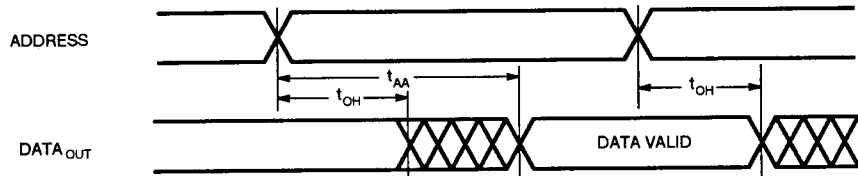
**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



**NOTE:**

1.  $\overline{WE}$  is HIGH for Read Cycle.

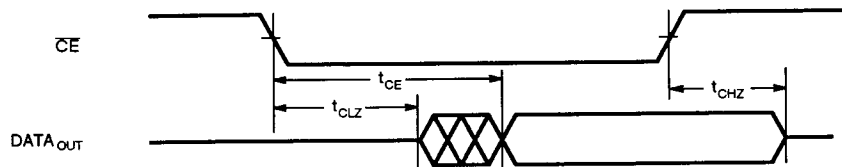
**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1)</sup>**



**NOTE:**

1.  $\overline{WE}$  is HIGH;  $\overline{CE} = V_{IL}$ ;  $\overline{OE} = V_{IL}$

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1)</sup>**



**NOTE:**

1.  $\overline{WE}$  is HIGH;  $\overline{OE} = V_{IL}$ ; address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ , All Temperature Ranges;  $C_L = 30pF$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
<b>WRITE CYCLE</b>				
$t_{AS}$	Address Set-up Time	5	—	ns
$t_{AH}$	Address Hold Time	50	—	ns
$t_{DS}$	Data Set-up Time	20	—	ns
$t_{DH}$	Data Hold from Write Time	15	—	ns
$t_{OES}$	Output Enable Set-up Time	5	—	ns
$t_{OEH}$	Chip Enable Hold from Write Time	15	—	ns
$t_{CES}$	Chip Enable Set-up Time	—	—	ns
$t_{CEH}$	Chip Enable Hold Time	0	—	ns
$t_{WP}$	Write Pulse Width	—	—	ns
$t_{WB}$	Byte Write Cycle	—	10	ms
$t_{DBV}$	DATA Polling to DATA Valid	—	$t_{OE}$	
$t_{WH}$	Write Hold Time	15	—	ns
$t_{DP}$	End of Write Pulse to $\overline{DATA}$ Polling	15	—	ns
$t_{WES}$	Write Enable Set-up Time	0	—	ns
$t_{WEH}$	Write Enable Hold Time	0	—	ns
$t_{DV}$	Data Valid Time (1, 2)	—	1	$\mu s$

**NOTES:**

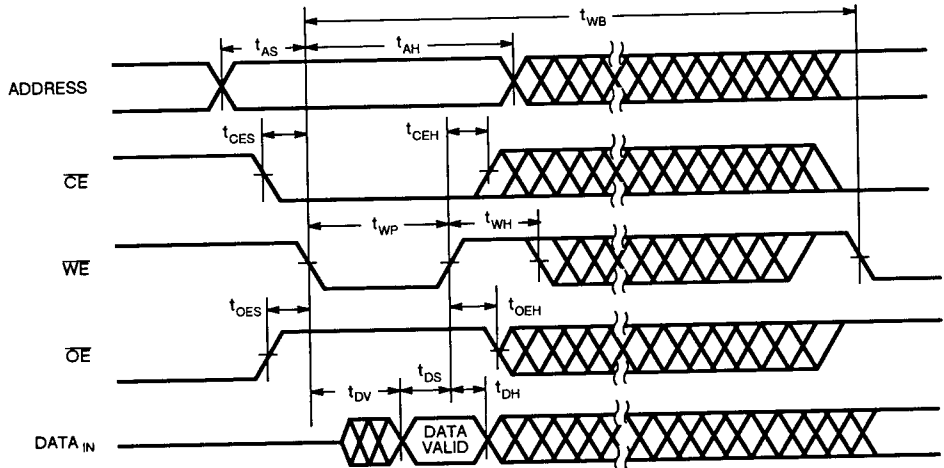
1. Data must be valid within 1 $\mu s$  maximum and must remain valid if  $t_{WP}$  is longer than 1 $\mu s$ .
2. This parameter is guaranteed but not tested

**AC TEST CONDITIONS**

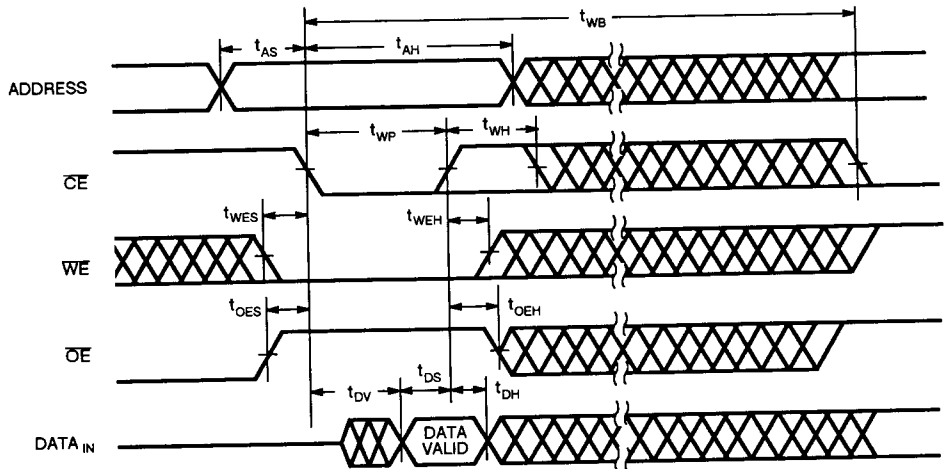
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

"DISCONTINUED"

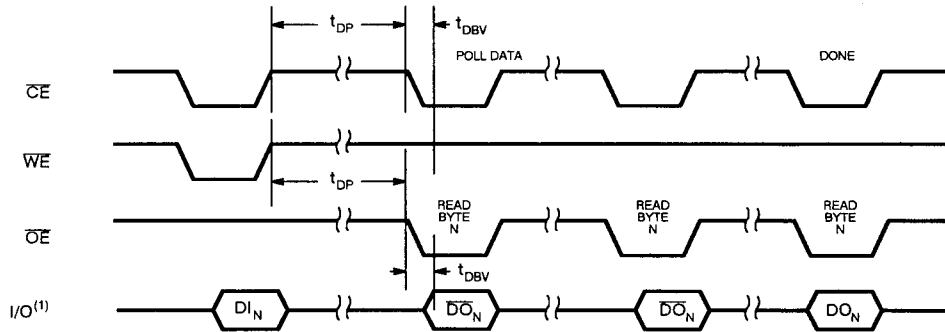
**TIMING WAVEFORM OF WRITE CYCLE NO. 1,  $\overline{WE}$  CONTROLLED**



**TIMING WAVEFORM OF WRITE CYCLE NO. 2,  $\overline{CE}$  CONTROLLED**



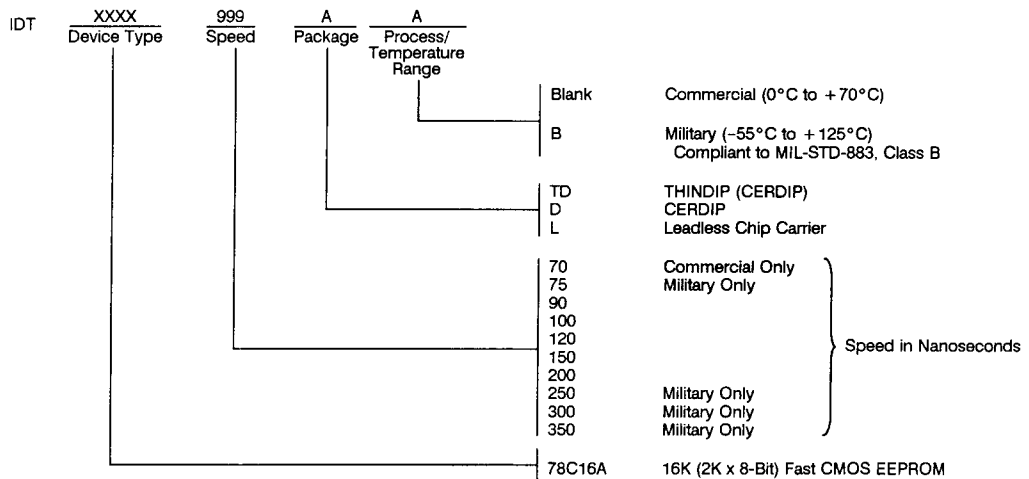
**DATA POLLING**



**NOTE:**

1. Most significant bit of the byte being written is inverted and available at I/O<sub>7</sub> if a Read command is issued. All other outputs are high impedance at this time. True data will not be released until the Write cycle is completed.

**ORDERING INFORMATION**



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