Le77D21

Voice Over Subscriber Line Interface Circuit with Auto Battery Switch
VoiceChip™ Family 770 Series

APPLICATIONS

- **Short/Medium Loop: approximately 2000 ft. of 26 AWG, and 5 REN loads**
- **Voice over IP/DSL – Integrated Access Devices, Smart Residential Gateways, Home Gateway/Router**
- **Cable Telephony – NIU, Set-Top Box, Home Side Box, Cable Modem, Cable PC**
- **Fiber–Fiber In The Loop (FITL), Fiber To The Home (FTTH)**
- **Wireless Local Loop, Intelligent PBX, ISDN NT1/TA**

FEATURES

- **Integrated Dual-Channel Chip set**
  - — Auto Battery Switch for low power consumption
  - — 3.3 V Logic Operation, 5-V tolerant
  - — Test Load Switch
  - — eTQFP Package (44-pin)
  - — Minimum Discretes
- **Ringing**
  - — 5REN
  - — up to 90 Vpk, Balanced
  - — Sinusoidal or trapezoidal with programmable DC offset
- **Subscriber Loop Test/Self-Test**
  - — GR-909 compliant drop test capability in both measurements and pass/fail
    - – Hazardous Potential
    - – Foreign Electromotive Force
    - – Resistive Faults
    - – Receive off-hook
    - – Ringers Test
    - – Loop length
    - – Power Supply, Feed, Ringing, AC Transmission
- **World Wide programmability:**
  - — Two-wire AC impedance
  - — Dual Current Limit
  - — Metering
  - — Loop closure and ringtrip thresholds
- **Eight SLIC Device States, including:**
  - — Low power Standby state
  - — On-hook transmission
  - — Reverse Polarity
  - — Ringing and Active with Test Load Switch

ORDERING INFORMATION

An Le78D11 codec/filter must be used with this part.

Device	Package
Le77D212TC	44-pin eTQFP

DESCRIPTION

Legerity's new solutions have enhanced and optimized features to directly address the requirements of voice over broadband applications. Their common goal is to reduce system level costs, space, and power through higher levels of integration, and to reduce the total cost of ownership by offering better quality of service. The Le78D11/Le77D21 chip set includes on-chip battery and bi-directional test load switches, providing a totally software configurable solution to the BORSCHT functions for two lines. The resulting system is not only very cost-effective, but is less complex, smaller and denser with minimal external components. Eight programmable states are available: Low Power Standby, Disconnect, Normal Active, Reverse Polarity, Ringing, Line Test, and two test load states— Active and Ringing. Binary fault detection is provided upon application of fault conditions or thermal overload.

RELATED LITERATURE

- **080697 Le78D11 Codec/Filter Data Sheet**
- **080716 VoiceChip™ Family 770 Series Chip Set Users Guide**
- **081013 Layout Considerations for the Le77D112 and Le9502 Devices Application Note**

BLOCK DIAGRAM

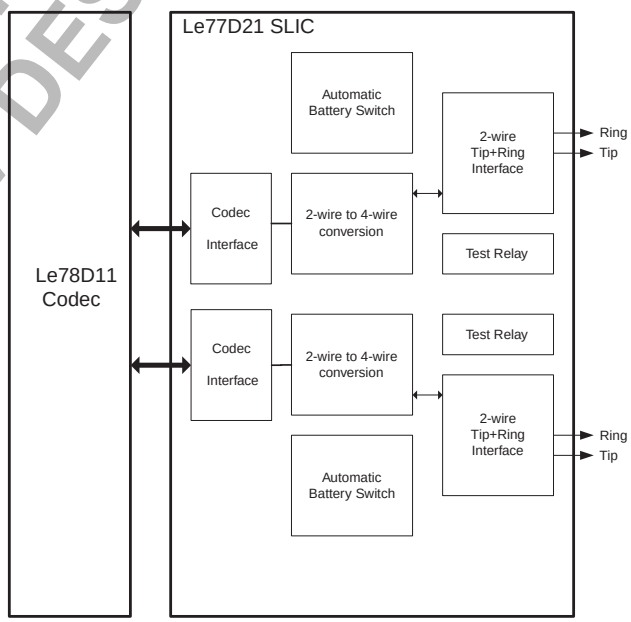

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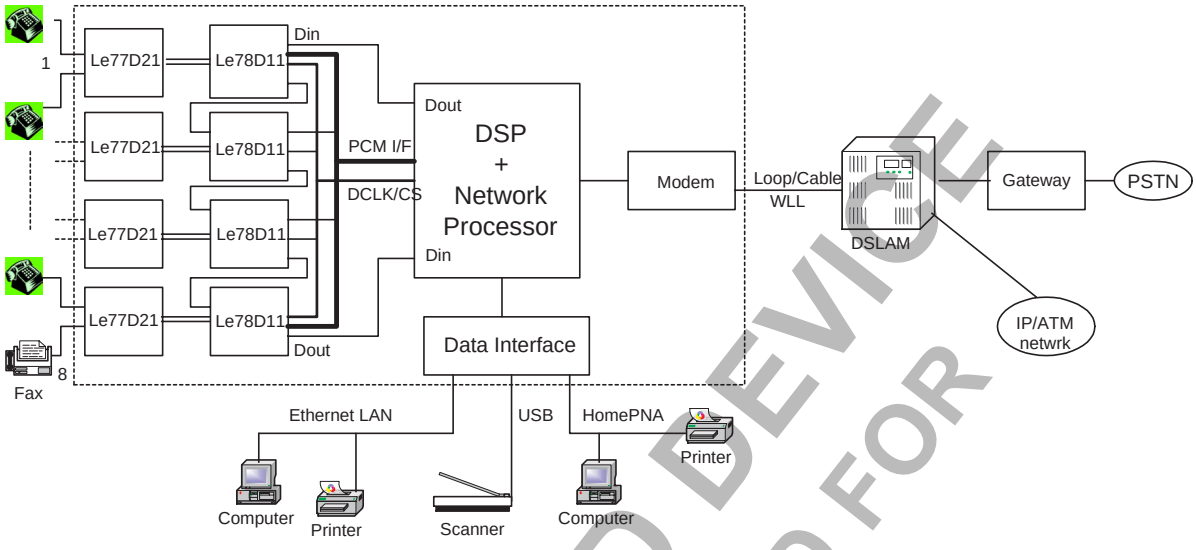
TABLE OF CONTENTS

PRODUCT DESCRIPTION

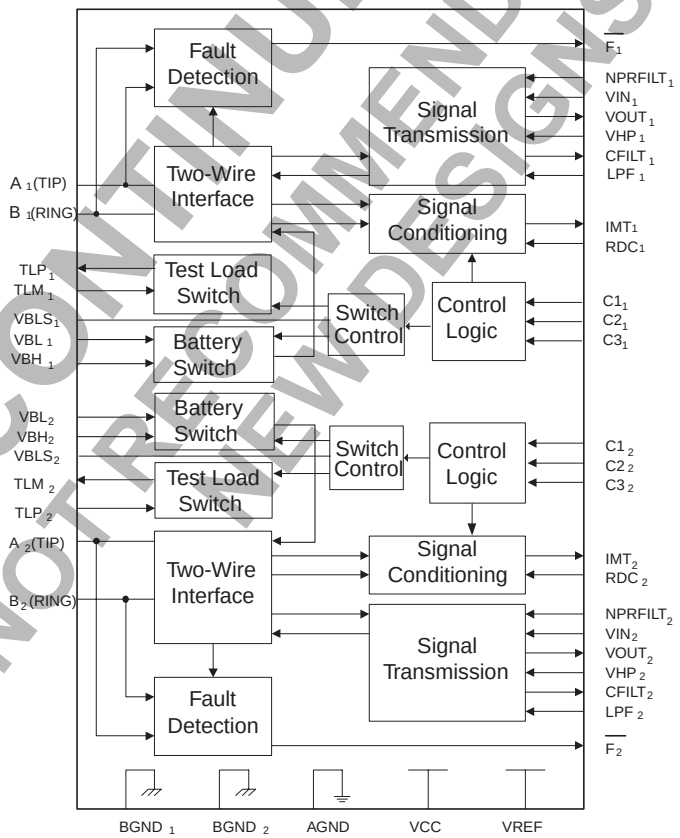
The dual-channel Le77D21 SLIC device uses reliable, dielectrically isolated, fully complementary bipolar technology to implement BORSCHT functions for short loop applications. Internal power dissipation is minimized through automatic battery switching to a lower battery voltage in Off-hook mode. Three power supplies—3.3 V, a negative High battery and a negative Low battery—are required for operation. Eight programmable states control loop signaling, transmission, ringing and loop testing functions. The Le77D21 SLIC device DC current feed limit (I_{SC})is programmable from 15 to 45 mA. Binary fault indication is provided on application of foreign voltages, longitudinal faults, or thermal overloads. This device is used in conjunction with the Le78D11 codec/filter for voice over broadband and other applications, such as the one shown in Figure 1 below.

Figure 1. Typical Le77D21/Le78D11 Chip Set
Application in an 8-Port Integrated Access Device in Customer Premises



BLOCK DESCRIPTIONS

Figure 2. Le77D21 SLIC device Block Diagram



Two-Wire Interface

The two-wire interface block provides DC current and sends/receives voice signals to a telephone connected via the A_i (TIP) and B_i (RING) pins. The A_i(Tip) and B_i(Ring) pins are also used to send the ringing signal to the telephone. The Le77D21 SLIC device can also be programmed in the Disconnect* state to place the A and B pins at high impedance.

Note:

**Devices may have up to 1 mA of leakage to VBH in the Disconnect state. This can cause either Tip or Ring to pull to VBH. To implement a service denial state and ensure compliance with UL 60950, use the Low Power Standby state instead of the Disconnect state. Program V_{DC} = 0 V to minimize loop current and mask the hook detect status.*

DC Feed

DC feed control in the Le78D11/Le77D21 chip set is implemented in the Le77D21 SLIC device. The current limit threshold (I_{LTH}) can be programmed up to 30 mA via the MPI interface of the Le78D11 codec/filter using the recommended R_{DC} value.

Referring to Figure 3, the DC feed curve consists of two distinct regions. The first region is a flat anti-sat region that supplies a constant Tip-Ring voltage (V_{AB} open). The second region is a constant current region that begins when the loop current reaches the programmed current limit threshold (I_{LTH}). This region looks like a constant current source with a 3.2 kΩ shunt resistor. The short circuit current is nominally 14.4 mA greater than I_{LTH}.

A block diagram of the DC feed control circuit is shown in Figure 4. In the anti-sat region, current source CS1 creates a constant reference current, which is limited to sub-voice frequencies by C_{LPFi}. This filtered current is then steered by the Polarity Control, depending on whether the SLIC mode is Standby, Normal Active, or Reverse Polarity. The steered current then takes one of two paths to the Level Shift block, where it is used to set A (TIP) and B (RING) voltage.

When I_{loop}/500 becomes greater than I_{LTH}/500, the difference is subtracted from CS1, and again filtered by C_{LPF}. This reduced current causes a reduced DC feed voltage. In Standby and Normal Active, A(TIP) is held constant, while B(RING) is changed to reduce the feed voltage. In Reverse Polarity, A (TIP) and B (RING) are swapped. When (I_{loop}-I_{LTH})/500 = CS1, all of the current from CS1 is subtracted, making the TIP-RING voltage = 0 V. This is the short circuit condition. At least 200-Ω loop and fuse resistance are required to ensure stability of the A (TIP) and B (RING) output amplifiers.

The capacitor C_{LPF}, in conjunction with an internal 25 kΩ resistor (not shown), is used to create a low pass filter for the DC feed loop. This capacitor should nominally be 4.7 µF, setting a 1.4 Hz pole. The purpose of this filter is to separate the operation of the DC feed from voice signal frequencies, preventing distortion and idle-channel noise, and improper operation of the battery switch during voice transmission.

Normal or Reverse Polarity is controlled by the Le78D11 codec/filter through the C3-1 state control pins. Some applications require slew rate control of the transition between these feed states. The capacitor, C_{NPRi}, may be used to increase the transition time and create a quiet polarity change. In the Normal Active state, the $NPRFILT_i$ pin is driven up to V_{CC}.

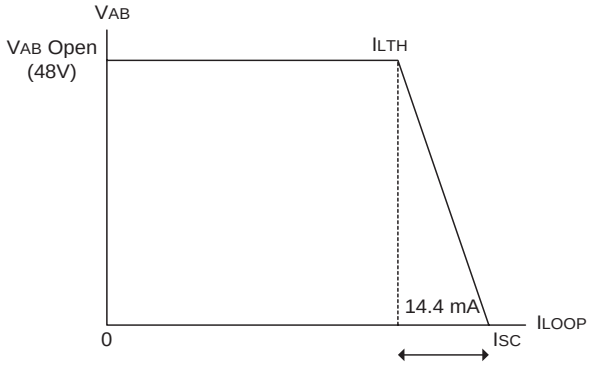
When Reverse Polarity is selected, C_{NPRi} is discharged by current I_{NPR}, and the transition time is:

$$\Delta t = \frac{(V_{CC} - V_{REF}) \bullet C_{NPRi}}{I_{NPR}}$$

In the Reverse Polarity state, the $NPRFILT_i$ pin is discharged near ground. When Normal Active is selected, C_{NPRi} is charged by current I_{NPR}, and the transition time is: $\Delta t = \frac{V_{REF} \bullet C_{NPRi}}{I_{NPR}}$

A 100-nF capacitor provides a nominal Normal Active to Reverse Polarity transition time of about 5 ms and a Reverse Polarity to Normal Active transition time of 3 ms.

Figure 3. DC Feed Curve



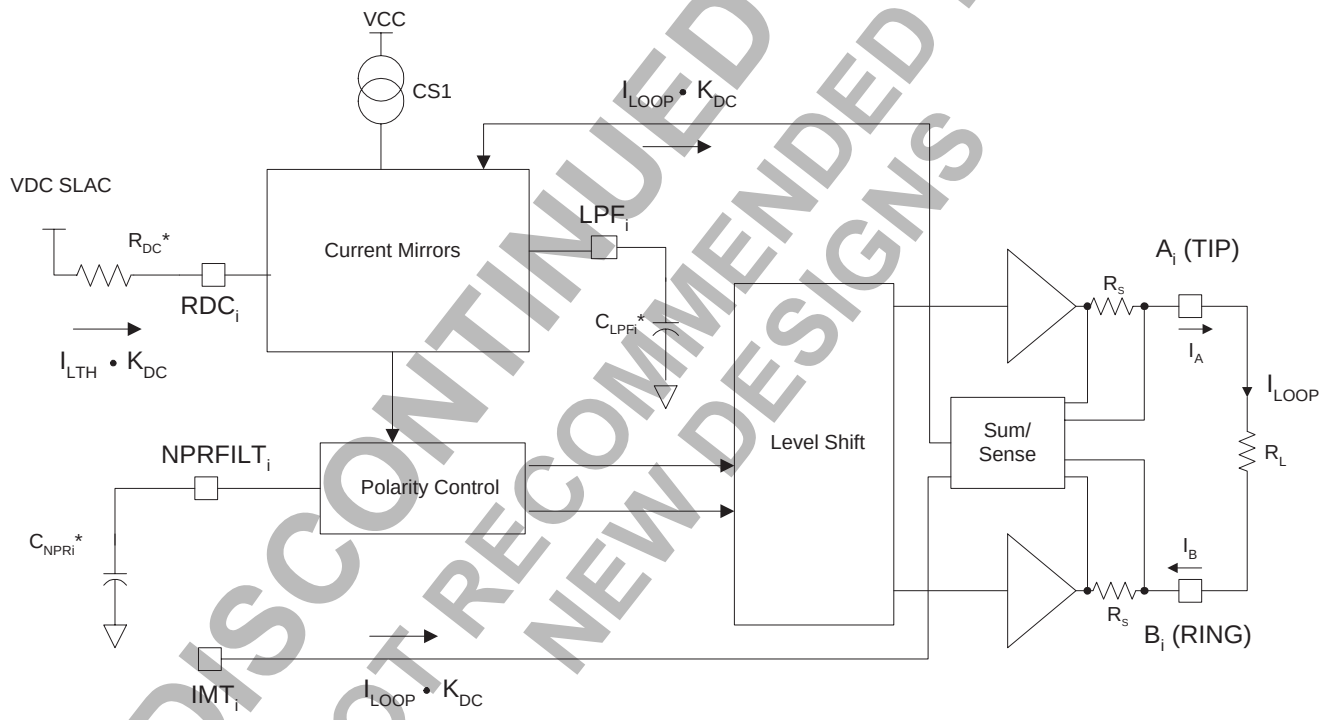
$$I_{SC} = I_{LTH} + 14.4\,mA$$

$$I_{LTH} = \frac{|V_{DC}|}{R_{DC}K_{DC}} = \frac{|V_{DC}|}{40}$$

Note:

1. *V_{DC} is programmable via Le78D11 codec/filter. (V_{DC} = 0.00 V to -1.20 V relative to V_{REF})*
2. *V_{REF} = 1.4 V nominal*
3. *K_{DC} = Le77D21 SLIC device DC current gain.* $K_{DC} = \frac{I_{MT}}{I_{LOOP}}$.
4. *R_{DC} = external resistor 20 kΩ nominal*
5. *$V_{AB} = V_{Ai} – V_{Bi}$ Tip-Ring differential voltage*
6. *I_{SC} = Loop short circuit current limit.*
7. *I_{LTH} = Loop current limit threshold. I_{LTH} should be programmed to 15 mA or less when in the Standby State.*
8. *14.4mA is a nominal value. See Device Specifications, on page 15 for expected variation.*

Figure 4. DC Feed Block Diagram, Active and Standby Modes



Note:

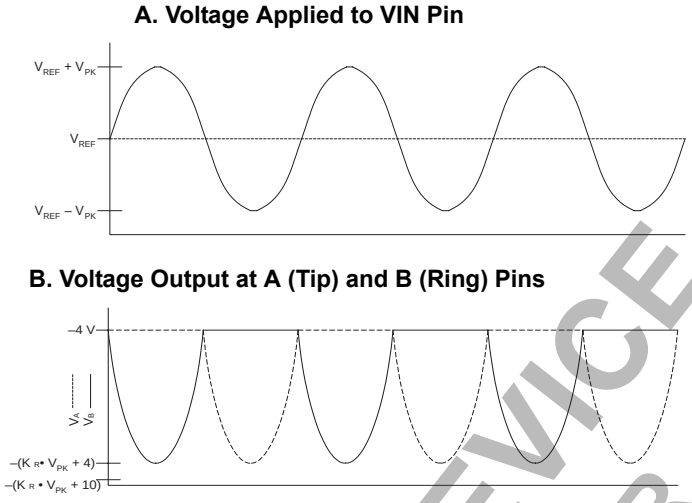
** denotes external components*

Ringing

Ringing is accomplished by placing the Le77D21 SLIC device into the Ringing state via the Le78D11 codec/filter's MPI interface. Placing the Le77D21 SLIC device into the Ringing state automatically enables signal generator A in the Le78D11 codec/filter which puts the ringing signal on the receive signal path (pin VIN). (For information on programming the Le78D11 codec/filter's signal generators, please refer to the *VoiceChip™ Family 770 Series Chip Set User's Guide*, document ID# 080716). When the

Le77D21 SLIC device is in the Ringing state, the gain from the Le77D21 SLIC device's input pin, VIN, to the output is K_R, the ringing voltage gain. The output is a quasi-balanced waveform, as shown in Figure 5. On the positive half cycle of the input waveform, when ($V_{IN} – V_{REF}$) is positive, V_{AB} is positive with $V_{A(TIP)}$ near –4 V and $V_{B(RING)}$ brought negative. When ($V_{IN} – V_{REF}$) is negative, $V_{B(RING)}$ is held near –4 V and $V_{A(TIP)}$ is brought more negative. The waveform can be either sinusoidal or trapezoidal under the control of the Le78D11 codec/filter.

Figure 5. Ringing Waveforms



SIGNAL TRANSMISSION

In Normal Active and Reverse Polarity states, the AC line current is sensed across the internal resistors, R_S (see Figure 1, on page 7), summed, attenuated and converted to voltage at the CFILT pin. This voltage then goes through a high pass filter (with a nominal 13 Hz corner frequency), implemented using an on-chip 8-kΩ nominal resistor and an external C_{HP} capacitor, amplified, and finally sent to the Le78D11 codec/filter at the VOUT pin. The output is proportional to the AC metallic component of the line voltage. Additionally, the signal transmission block receives the analog signal from the Le78D11 codec/filter. The analog signal is amplified and sent to the line.A proportion of the signal at V_{OUT} is also fed back to the line.

There are three parameters which define the AC characteristics of the Le77D21 SLIC device: (1) the input impedance presented to the line or 2-wire side (Z_{2WIN}), (2) the gain from the 4-wire (V_{IN}) to the 2-wire (V_{AB}) side (G_{42}), and (3) the gain from the 2-wire side to the 4-wire (V_{out}) side (G_{24}).

Input Impedance (Z_{2WIN})

Z_{2WIN} is the impedance presented to the line at the 2-wire side, and is defined by:

$$Z_{2WIN} = 2R_F + K_V K_{OUT} R_{IMT}$$

where 2 • R_F is the total resistance of the external fuse resistors in the circuit, R_{IMT} is the impedance setting resistor, K_{OUT} is the gain from V_{OUT} to V_{AB}, and K_V is the voice current gain defined in the Transmission Specifications Table. Note that the equation reveals that Z_{2WIN} is a function of the selectable resistors, R_{IMT} and R_F. For example, if R_F = 0 Ω and R_{IMT} is 100 k, the terminating impedance is 600 Ω. This is the configuration used in this data sheet for defining the device specifications. However, in a real application, R_F = 50 Ω is recommended, producing a total input impedance of 700 Ω which is a good starting point for meeting worldwide requirements using the programmable filters of the Le78D11 codec/filter.

2-Wire to 4-Wire Gain (G_{24})

The 2-wire to 4-wire gain is the gain from the phone line to the V_{OUT} output of the Le77D21 SLIC device. To solve for G_{24}, the VIN pin is grounded (see Figure 1).

$$\frac{V_{OUT}}{V_{AB}} = G_{24} = \frac{1}{\frac{2R_F}{K_V R_{IMT}} + K_{OUT}}$$

or

$$G_{24} = -20\log\left(K_{OUT} + \frac{2R_F}{K_V R_{IMT}}\right) \text{ in dB}$$

Using the values of R_{IMT} and R_F from the application example, G_{24} for this circuit is –10.9 dB.

4-Wire to 2-Wire Gain (G_{42})

G_{42} is the gain from the VIN input to the line. This gain is defined as V_{AB}/V_{IN}.

$$\frac{V_{AB}}{V_{IN}} = G_{42} = \frac{K_{IN}\left(\frac{R_L}{R_L + 2R_F}\right)}{\left(1 + \frac{K_{OUT}R_{IMT}K_V}{R_L + 2R_F}\right)}$$

or

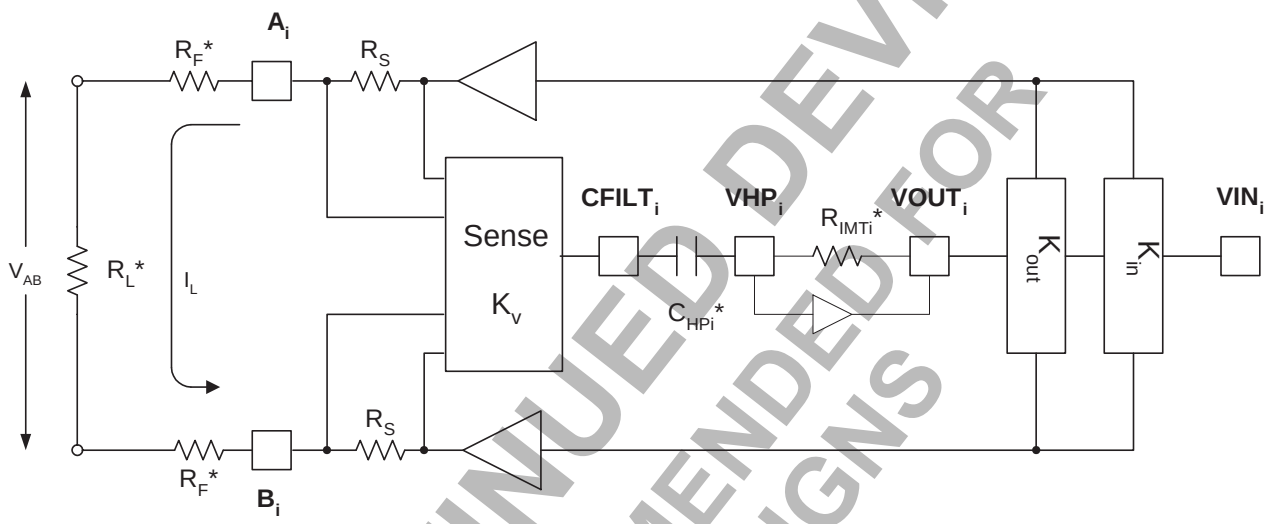
$$G_{42} = -20\log\left[\frac{K_{IN}\left(\frac{R_L}{R_L + 2R_F}\right)}{\left(1 + \frac{K_{OUT}R_{IMT}K_V}{R_L + 2R_F}\right)}\right] \text{ in dB}$$

where K_{IN} is the gain from VIN to V_{AB}. Using the values of R_{IMT} and R_F from the application example and R_L = 600 Ω, G_{42} for this circuit is 7.3 dB.

Note:

Equation derivations can be found in the Legerity VoiceChip™ Family 770 Series Chip Set User's Guide (document ID# 080716).

Figure 1. Transmission Block Diagram



Note:

** denotes external components.*

FAULT DETECTION

Each channel of the VoSLIC device has a fault detection pin, $\overline{F}_1$ or $\overline{F}_2$. These pins are driven Low when a longitudinal current fault or foreign voltage fault occurs (see Figure 4). When not in Disconnect state, there are three conditions that will cause the $\overline{F}_i$ pin to indicate a fault condition:

- $|I_A - I_B| > I_{LONG}$
- In Normal Active and Standby state, a foreign voltage fault occurs in which V_A is above ground or V_B is close to V_{BH}.
- In Reverse Polarity state, a foreign voltage fault occurs in which V_B is above ground or V_A is close to V_{BH}.

In the Disconnect state, fault detection is not supported; however, fault conditions can be monitored by the Le78D11 device.

For more details on AC, DC fault detection, loss of power, or clock-failure alarm, please refer to the *VoiceChip™ Family 770 Series Chip Set User's Guide*.

Signal Conditioning

The RDC_i pin is used to set the DC feed current limit, as described in the DC feed section.The IMT_i pin provides K_{DC} times the loop current to the Le78D11 codec/filter. The Le78D11 codec/filter implements all loop supervision and ring trip processing on this signal.

$$I_{IMT} = \frac{I_A + I_B}{2} \bullet K_{DC}$$

Thermal Overload

When the die temperature around the power amplifier of an Le77D21 SLIC device channel reaches approximately 160°C, the IMT pin of that channel is pulled high. At the same time, all the blocks controlling that channel of the device are shut off, except for the logic interface block. The Le77D21 SLIC device channel goes into a state similar to Disconnect, making the line current zero. When the temperature drops below 145°C, the Le77D21 SLIC device channel returns to its previous state. It is important to recognize that even while a channel experiences thermal overload, the state of the device can be modified.

Battery Switch and Control

To control power dissipation under normal operating conditions, a battery switch is provided to enable use of a low voltage battery. Two battery supplies are needed to provide high voltage ringing, on-hook idle loop condition requirements and active voice transactions.The decision to switch battery is based upon the operating modes, loop voltage, and the low battery voltage. Care should be taken to select the appropriate low battery (V_{BL}) voltage using the equations below to avoid operation near the threshold.

High Battery Voltage

The High Battery Voltage (VBH) is used to supply the Idle Loop Voltage in the standby (on-hook) state and the high amplitude ringing signal during Ringing state.

Low Power Standby:

min $V_{BH} = V_{AB} + V_{OH}$ (tip) + V_{OH} (ring)

Where V_{AB} = Tip to Ring open circuit voltage, V_{OH} (tip)=1 V and V_{OH} (ring) = 4 V are the overhead voltages. For V_{AB} = 51 V max

min V_{BH} = 51 + 5 = –56 V

For Normal Active, Reverse Polarity, and Active with Test Load, on hook:

min $V_{BH} = V_{AB} + 2\ V_{OH}$ = 51 V + 10V = –61 V (in all states except Standby, V_{OH} (tip) = V_{OH} (ring) = V_{OH}= 5 V)

For Ringing, Line Test, Ringing with Test Load:

$$V_{BH} = V_{rms} CF \left[\frac{Zr + R_{loop} + 2R_F}{Zr}\right] + 2V_{OH}$$

Where V_{rms} is the required voltage across the ringer load (REN), Z_r= ringer impedance, CF= crest factor , and V_{OH} = overhead voltage as shown in Figure 2, on page 9.

Example 1.

For a typical 500 ft. loop application with desired ringing voltage of 40 mVrms across the load and trapezoidal ringing waveform:

R_{loop}(26 AWG wire) = 42.5 Ω and CF=1.25

For a 5 REN ringer load (1380 Ω+ 40 µF), $|Z_r|$ @ 20 Hz = |(1380 Ω + 40 µF)| ~ 1382 Ω, V_{OH} = 5.0 V (max.); R_F = 50 Ω

V_{BH} = 40 • 1.25 • 1.10 + 10 = 65 V

Example 2.

For a typical 2000 ft. loop application with trapezoidal ringing waveform R_{loop}(26 AWG wire) = 170 Ω and CF=1.25

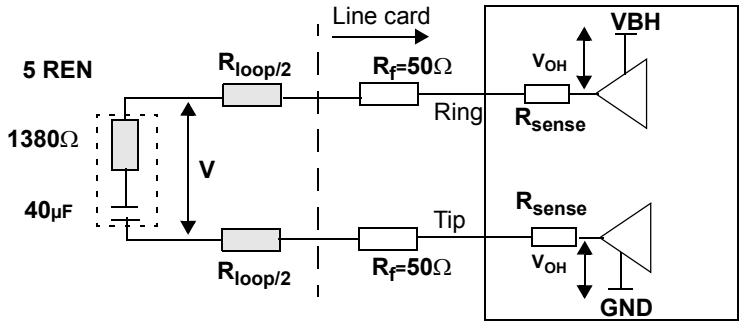
For a 3 REN ringer load (2300 Ω+24uF), $|Z_r|$ =@ 20Hz = 2320 Ω, V_{OH} = 5.0 V (max.); R_F = 50 Ω

V_{BH} = 40 • 1.25 • 1.12 + 10 = 66 V

All States: max V_{BH} = –100 V.

Therefore, to meet all of the above requirements, the minimum |VBH| should be 66 V.

Figure 2. High Battery Calculation



Low Battery Voltage

The Low Battery Voltage (VBL) is used to supply the current during the Active (off-hook) state. The minimum VBL required is provided by the following formula.

$$V_{BL_{(min)}} = \frac{V_{AB}open + [DC_{Slope} \cdot ILTH]}{1 + \frac{DC_{Slope}}{2 \cdot (R_f + R_{sense}) + R_{loop} + R_{Set}}} + 2V_{OH}(max) + V_{DIODE}$$

Where I_{LTH} = loop current limit threshold, R_{loop}, R_f, R_{sense} are the loop resistance, fuse and sense resistance respectively (see Figure 3), V_{AB} = tip to ring open circuit voltage, V_{OH} = overhead voltage, DC_{Slope} = the DC feed slope and V_{DIODE}= voltage across the V_{BL}diode.

Example 1:

For a typical 500 ft loop, R_{loop} = 42.5 Ω, R_{Set} = 430 Ω, and with I_{LTH} = 20 mA, I_{LTH} tol = 2 mA, R_f = 50 Ω, R_{sense} = 20 Ω, V_{OH}(max) = 5.0 V, V_{AB} open (max) = 51 V and DC_{Slope} (worse)= 2.2 kΩ

$$V_{BL_{(min)}} = \frac{51V + [2.2k\Omega(22mA)]}{1 + \frac{2.2k\Omega}{2(50\Omega + 20\Omega) + 42.5\Omega + 430\Omega}} + 2(5.0V) + 0.7V = 32.34V$$

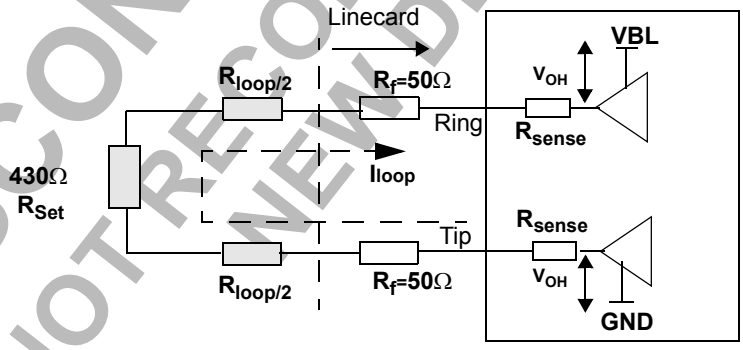
Example 2:

For a typical 2000 ft loop, R_{loop} = 170 Ω, R_{Set} = 430 Ω, and with I_{LTH} = 20 mA, I_{LTH} tol = 2 mA, R_f = 50 Ω, R_{sense} = 20 Ω, V_{OH}(max) = 5.0 V, V_{AB} open (max) = 51 V and DC_{Slope}(worst)= 2.2 kΩ

$$V_{BL_{(min)}} = \frac{51V + [2.2k\Omega(22mA)]}{1 + \frac{2.2k\Omega}{2(50\Omega + 20\Omega) + 170\Omega + 430\Omega}} + 2(5.0V) + 0.5V = 35.5V$$

Therefore, the minimum V_{BL} should be 35.5 V.

Figure 3. Low Battery Calculation



Test Load Switch

The test load switch is a low impedance bi-directional on/off switch to facilitate Active mode and Ring mode tests to be performed with an external test load connected across the tip and ring leads. There are two modes, Active+Test Load and Ringing + Test load which activate this switch

Test Load Selection

To meet the 50 mA peak current requirement and assuming maximum ringing of 90 V peak, the R_{test} (min.) = (90-4)/0.05=1.72 kΩ.

The maximum value should be defined to still operate with the programmed off-hook threshold. With a standard 800-Ω feed, this is typically 10 mA/ 4000 Ω. Limits are 30%, giving R_{test} (max) = 2.9 kΩ (2.7 kΩ recommended)

Off-Hook Tests

These tests can be performed by switching from standby to active+test load state. The normal off-hook threshold can be used and AC transmission tests can be performed into the test load. With the recommended load value, the DC loop voltage does not change significantly and is unlikely to cause problems with an attached phone. The V_A, V_B, and V_{AB} voltages and the I_{MT} loop current can be read directly from the Le78D11 codec/filter.

Ringing Tests

These tests can be performed by switching from standby to ringing+test load enabled state. To minimize risk of bell tinkle, these tests are best performed with a DC voltage rather than the AC produced by signal generator A in the Le78D11 codec/filter. To minimize transients, a nominal DC voltage of –48V should be established.

This test requires modified ring trip threshold to be used. Once normal polarity has been tested, the signal can be slowly ramped to +48V and tested again in the reverse polarity, to confirm current feeding in both polarities. Finally, ramp back to –48V and return to Standby state.

Control Logic

Each channel of the Le77D21 SLIC device has three input pins from the Le78D11 codec/filter (C3, C2, and C1). The inputs set the operational state of each channel. There are eight operational SLIC states (See Table 1): Low Power Standby, Disconnect, Normal Active, Reverse Polarity, Ringing, Line Test, Active with test load and Ringing with test load

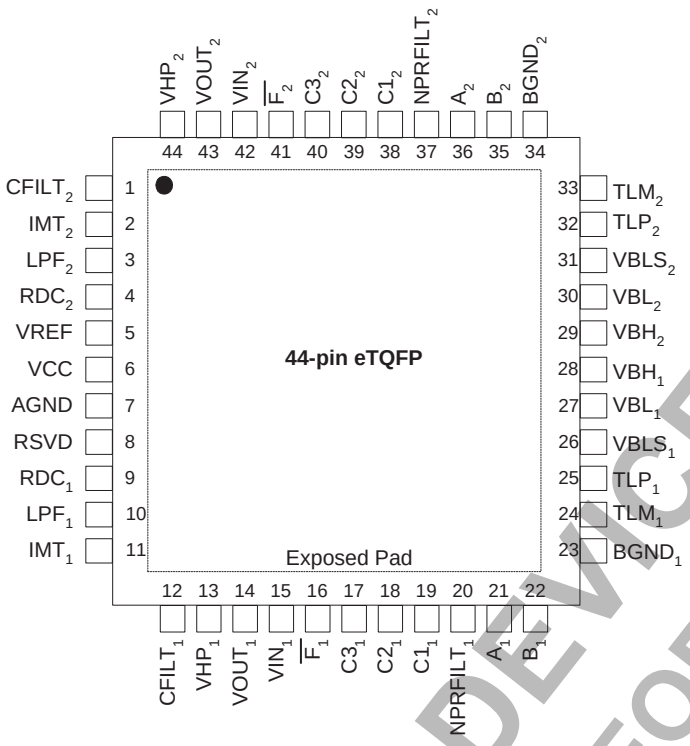
Table 1. Device Operating States

C3	C2	C1	Operating Mode	Description
0	0	0	Low Power Standby	Voice transmission disabled. Maximum loop current capability is reduced.
0	0	1	Disconnect*	Le77D21 SLIC device channel is shut down and presents a high impedance to the line.
0	1	0	Normal Active	Le77D21 SLIC device channel fully operational. A (TIP) is more positive than B (RING). Also used for on-hook transmission.
0	1	1	Reverse Polarity	Similar to normal active, but DC polarity is reversed so that the B (RING) lead is more positive than the A (TIP) lead. Also used for on-hook transmission.
1	0	0	Ringing	Ringing state with V_{AB} set to $K_R \cdot V_{IN}$. The switching supply maintains minimum headroom for the sourcing and sinking amplifiers in order to maximize power efficiency.
1	0	1	Line Test State	Similar to ringing state with reduced bias currents for lower noise. Loop current sensing range is limited. See IMT pin specifications.
1	1	0	Active + Test Load	Normal Active with test switch enabled.
1	1	1	Ringing + Test Load	Ringing with test switch enabled.

Note:

**During line testing, wait more than 3 seconds before proceeding with a line measurement.*

CONNECTION DIAGRAM



Note:

1. *Pin 1 is marked for orientation.*
2. *Both VBLS pins must be connected together.*

PIN DESCRIPTIONS

Pin Name	Type	Description
AGND	Ground	Analog and digital ground return for VCC circuitry (common to both channels)
$A_{1,2}$ (TIP)	Output	A (Tip lead) power amplifier output for channels 1 and 2
$BGND_{1,2}$	Ground	Battery ground return for power amplifiers on channels 1 and 2
$B_{1,2}$ (RING)	Output	B (Ring lead) power amplifier output for channels 1 and 2
$C1_1$, $C2_1$, $C3_1$	Input	Logic control inputs to control channel 1 state
$C1_2$, $C2_2$, $C3_2$	Input	Logic control inputs to control channel 2 state
$CFILT_{1,2}$	Output	AC coupling pin for 4-wire amplifier
$\overline{F}_{1,2}$	Output	Fault detect pins for channels 1 and 2. A low indicates a fault for the respective channel, which can be triggered by large longitudinal voltages, or ground key
$IMT_{1,2}$	Output	Current output equal to the loop current divided by 500. During thermal overload, IMT is forced to V_{CC}
RSVD	Input	Reserved
$LPF_{1,2}$	Output	A capacitor tied to from this pin to AGND stabilizes the DC feed loop, and lowers Idle Channel Noise
$NPRFILT_{1,2}$	Output	An optional capacitor tied from these pins to AGND controls the reverse polarity slew rate of channels 1 and 2
$RDC_{1,2}$	Input	Resistor connection to programmable VDC of the Le78D11 codec/filter to set DC feed current limit (I_{LTH})
$TLP_{1,2}$	Input	Test Load Switch input, a test load is connected from this pin to the tip lead
$TLM_{1,2}$	Input	Test Load Switch input, a test load is connected from this pin to then ring lead
$VBL_{1,2}$	Supply	Low Battery Voltage power to each channel through an external diode
$VBH_{1,2}$	Supply	High Battery Voltage power supply (tie pins together)
$VBLS_{1,2}$	Supply	Low battery sense pin for battery switch control
VCC	Supply	A nominal 3.3 V power supply for internal VCC circuitry (common to both channels)
$VHP_{1,2}$	Output	High pass invert summing node of the VOUT amplifier driven by the AC current coming from CFILT1 and CFILT2
$VOUT_{1,2}$	Output	Analog (4-wire side) VOUT amplifier transmit output
$VIN_{1,2}$	Input	Analog (4-wire side) voice or ringing signal input. This pin multiplexes between 4-wire voice input and ringing input depending on the SLIC device programmed state
VREF	Supply	A nominal 1.4 V reference supplied by the Le78D11 codec/filter for internal use (common to both channels)
Exposed Pad	Isolated	Exposed pad on underside of device must be connected to a heat spreading area. The AGND plane is recommended

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage temperature	–55 to +150°C
Ambient temperature, under bias	-40° to 85°C
V_{CC} with respect to AGND	–0.4 to +6.5 V
VBLS to BGND	+0.4 to –104 V
VBH to GND	+0.4 to -104 V
BGND with respect to AGND	–100 mV to 100 mV
A (TIP) or B (RING) to BGND:	
Continuous	V_{BH} –1 to BGND +1
10 ms (F = 0.1 Hz)	V_{BH} –5 to BGND +5
1 µs (F = 0.1 Hz)	V_{BH} –10 to BGND +10
250 ns (F = 0.1 Hz)	V_{BH} –15 to BGND +15
Current from A (TIP) or B (RING)	±150 mA
C1, C2, C3 to AGND	–0.4 to VCC + 0.4 V
VREF	AGND to VCC
Maximum power dissipation	1.8 W
Thermal Data: In 44-pin eTQFP package	θ_{JA} 32° C/W
Thermal Data: In 44-pin eTQFP package	θ_{JC} 9.2° C/W
ESD Immunity (Human Body Model)	±800 V minimum
CDM Immunity (Charge Device Model)	±600 V minimum

Notes:

Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165ºC. Continuous operation above 145ºC junction temperature may degrade device reliability.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through 16 0.3 mm diameter vias on a 1.27 mm pitch to a large (> 500 mm^2) internal copper plane. (Refer to Legerity application note Layout Considerations for the Le77D112 and Le9502 Devices, document ID# 081013).

OPERATING RANGES

Legerity guarantees the performance of this device over commercial (0º C to 70º C) and industrial (–40º C to 85º C) temperature range by conducting electrical characterization and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40° to 85° C

Electrical Ranges

VCC	3.3 V ± 5%
VBH	– 56* to -100 V
VREF	1.40 V ± 50 mV
VBL	– 20* to VBH

Note:

**See Battery Switch and Control, on page 8 for voltage requirements for specific applications.*

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, test conditions are: V_{CC} = 3.3 V, V_{REF} = 1.4 V, BATH = -80.0 V, BATL= –32 V, AGND = BGND

For Active, Reverse Polarity, Line Test, Disconnect, Ringing+Test Load, Active+Test load and Line Test modes, V_{DC} = 0.6 V (I_{LTH} = 15 mA); for Standby V_{DC}=0.4 V (I_{LTH} = 10 mA)

There are no fuse resistors, R_L=600 Ω. Ringing configuration is $V_{IN} - V_{REF}$ = 0.7 Vpk., 20 Hz sinusoidal.

Refer to *Test Circuit*, on page 18 for all other component values

DC Supply Currents and Power Dissipation

Operation States	Condition	V_{CC} Supply Current Icc			VBL Supply Current I_{VBL} mA			VBH Supply Current I_{VBH} mA			Total Power Dissipation mW			SLIC Device Power mW			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Note
Standby	R_L = open		4.0	7.0		0	0.25		1.6	3.0		150	300		150	300	
Disconnect	R_L = open		3.0	4.5		0	0.25		0.5	0.9		50	90		50	90	1
Active	R_L = open		6.5	10.0		0	0.25		3.0	7.0		260	400		260	400	
	R_L = 600 Ω		6.6	10.0		35.0	41.0		0	0.25		1140	1350		500	650	1,2
	R_L = 300 Ω		6.6	10.0		36.0	43.0		0	0.25		1200	1417		825	975	1
Reverse Polarity	R_L = open		6.5	10.0		0	0.25		3.0	7.0		260	400		260	400	
	R_L = 600 Ω		6.6	10.0		35.0	41.0		0	0.25		1120	1350		500	650	1,2
	R_L = 300 Ω		6.6	10.0		36.0	43.0		0	0.25		1120	1417		825	975	1
Ringing	R_L = open		5.6	9.0		0	0.25		3.0	7.0		266	400		260	400	1,2
Ringing	R_L = 1400Ω		6.4	10.0		0	0.25		37.0 rms	43.0 rms		3020	3500		1230	1350	1
Line Test	R_L = open		5.0	8.0		0	0.25		0.2	4.5		230	390		230	350	
Active + Test Load	R_L = open		6.5	10.0		0	0.25		24.0	31.0		2140	2500		1000	1250	1
Ringing + Test Load	R_L = open Vin=0.5 Vdc		6.5	10.0		0	0.25		26.5	33.0		2140	2500		1000	1250	

Note:

1. *Current and Power numbers shown are for one channel only but are tested with both channels in the same state*
2. *Not tested in production. parameter is guaranteed by characterization or correlation to other tests*

System Specifications

The performance targets defined in this section are for a system using the Le78D11/Le77D21 chip set. Specifications for the Le78D11 codec/filter are published separately.

Item	Condition	Min	Typ	Max	Unit	Note
Peak Ringing Voltage	Ringing mode, R_{LOAD} = 1500 Ω,		70	90	V	4.
Output Impedance during internal ringing	Ringing mode, Le78D11 codec/filter generating internal ringing		2 • RF		Ω	4.
Sinusoidal Ringing THD	Ringing mode, R_{LOAD} = 1500 Ω generating internal sinusoidal ringing		2		%	4.
Signaling Performance Limits						
Hook switch threshold	ITH = 10 mA	7		13	mA	4.
Hook switch hysteresis	All ITH settings		10		%	3.
Internal Ring-trip Accuracy	RTSL= 2.2 W (07h)	–20		+20	%	4.
Test Switch Limits	Continuous switch turn on		2		s	4.

Device Specifications

Specification	Condition	Min	Typ	Max	Unit	Note
Line Characteristics						
V_A active V_B Reverse Polarity	R_L = open		–4		V	
V_A open	Standby		–1		V	
V_{AB} open	Active or Reverse Polarity	44	48	52	V	1.
V_{AB} open	Standby	44	48	53	V	1.
DC Feed Slope (DC_{slope})	V_{AB} open 45 Vo 51 V		3.2		kΩ	4.
Loop Current, I_L accuracy	Active or Reverse Polarity, R_L = 600 Ω; I_{LTH} = 15 mA	I_{LTH} + 6	I_{LTH} + 11.3	I_{LTH} + 20		
	Standby R_L = 600 Ω; I_{LTH} = 10 mA	I_{LTH} + 6	I_{LTH} + 11.5	I_{LTH} + 20		
Short circuit loop current, I_{SC}	Active or Reverse Polarity, R_L = 100 Ω; I_{LTH} = 15 mA	I_{LTH} + 10	I_{LTH} + 13.5	I_{LTH} + 29		
	Standby R_L = 100 Ω; I_{LTH} = 10 mA	I_{LTH} + 10	I_{LTH} + 13.7	I_{LTH} + 29		4.
LPF_i	Output impedance		25		kΩ	3.
	Bias voltage with respect to GND		2.2		V	
	Leakage current for capacitor value of 4.7 µF ± 20%			0.1	µA	
$NPRFILT_i$ drive capability	$\|I_{NPRi}\|$	30		130	µA	
Fault Detection						
Longitudinal Fault Threshold I_{LONG}		18	25	37	mA	8.
Ringing and Line Test State						
V_A, V_B	V_{IN} = V_{REF} R_L = 1400 Ω		–4		V	3.
V_{AB} offset	V_{IN} = V_{REF}	–2		+2	V	
Voltage gain, K_R	R_L=1400Ω, $K_R = \frac{V_{AB}}{V_{IN}} \bullet V_{IN}$ = 0.7Vpk	95	100	106	V/V	1.
Ringing distortion	R_L = 1400 Ω, V_{IN} = 0.7 V_{PK}		0.5	3.5	%	
Ringing current limit	R_L = 100 Ω	90	120	200	mApk	3.
	R_L = 300 Ω		145			

Specification	Condition	Min	Typ	Max	Unit	Note
Battery Switch Performance Characteristics						
Battery Switch Threshold	VBH to VBL		VBL+10		V	4.
Battery Threshold Hysteresis	VBL to VBH after switch to VBL		1.0			3.
Test Load Switch Characteristics and Limits						
Polarity	Bi-Directional					3.
Voltage drop	25 mA		2.6		V	
	50 mA		4.0			4.
External Test Load	Resistive, Between Tip and Ring	1.7		2.7	kΩ	4.
TLP, TLM	Leakage to ground (switch open)			10	µA	4.
	Input Current capability			50	mA	4.
Power Supply Rejection Ratio at the 2-wire interface						
V_{CC} to V_{AB}	200 to 4000 Hz	25	45		dB	
	4 to 20 kHz, 50 mV_{RMS}	20	40			4.
V_{BH}	200 to 4000 Hz, 100 mV_{RMS}	28	50			
V_{BL}	200 to 4000 Hz, 100 mV_{RMS}	35	50			
Longitudinal Capability						
Longitudinal balance	R_L = 600 Ω, 300 to 3400 Hz, 0 dBm, Active and Reverse Polarity	46	60		dB	
T-L balance	1 kHz, 0 dBm	40	50			
Longitudinal current per pin	A(TIP) or B(RING)	25	30		mA	4.
Longitudinal impedance	A(TIP) or B(RING), 0 to 100 Hz		1	5	Ω/pin	4.
Transmission Performance						
2WRL	300 Hz to 3400 Hz	18			dB	4.
K_{DC} DC current gain (IMT accuracy)	$K_{DC} = \frac{I_{IMT}}{I_{LOOP}}$, R_L = 600 Ω, Active, Standby and Rev. Pol.	$-\frac{1}{525}$	$-\frac{1}{500}$	$-\frac{1}{475}$	A/A	6.
K_V Voice Current gain	Line Test, Standby I_L < |20 mA| Active or Rev. Pol. I_L < |80 mA| Ringing I_L < |100 mA|	$\frac{1}{520}$	$\frac{1}{500}$	$\frac{1}{480}$		4.
V_{IN} to V_{AB} (K_{IN})	R_L = open, 0dBm on 2W side	13.7	14	14.3	dB	
V_{OUT} to V_{AB} (K_{OUT})		9.74	9.54	9.34		4.
Gain accuracy 2- to 4-Wire	0 dBm, 1 kHz on 2W side	-9.74	-9.54	-9.34		
Gain accuracy 4- to 2-Wire	0 dBm, 1 kHz on 2W side	7.76	7.96	8.16		
Gain accuracy 4- to 4-Wire	0 dBm, 1 kHz on 2W side	–1.98	–1.58	–1.18		
Gain accuracy over frequency	300 to 3400 Hz, Relative to 1 kHz	–0.1		+0.1		
Gain tracking at 1kHz, relative to 0 dBm	–30 dBm to +3 dBm, 2-Wire	–0.1		+0.1		
	–55 dBm to –30 dBm, 2-Wire	–0.1		+0.1		4.
Gain tracking On Hook	0 dBm to –30 dBm	-0.15		0.15		4., 7.
	+3 dBm to 0 dBm	-0.35		0.35		4., 7.
THD (Total Harmonic Distortion)	0 dBm, 2-wire, 1 kHz		–64	–50		
	+7 dBm, 2-wire, 1 kHz		–55	–40		
THD, On Hook	0 dBm, 2-wire, 1kHz			–36		7.
Overload Level, 2-Wire	Active or Reverse Polarity, 1kHz	2.5			Vpk	2.
Idle Channel Noise	C-message		12	15	dBrnC	4.
Idle Channel Noise	Psophometric		-78	-75	dBmP	
$CFILT_i$	Output impedance		8000		Ω	3., 5.
	Drive capability, Active State	–150		+150	µA	
VHP_i	Input impedance		5		Ω	
	Offset voltage with respect to V_{REF}	–20		+20	mV	

Specification	Condition	Min	Typ	Max	Unit	Note
$VOUT_i$	Output impedance		1		Ω	3.
	Offset voltage with respect to V_{REF}	–50		+50	mV	
	Drive capability, R_L = 20 kΩ	$\frac{V_{REF} - 1}{20\ k}$		$\frac{V_{REF} + 1}{20\ k}$	µA	
VIN_i	Input impedance	200			kΩ	3.
	Offset voltage voice	–20		+20	mV	
	Ringing and Line Test	–20		+20		
V_{REF}	Bias current	0		+200	µA	
Metering gain R_L = 300 Ω,	Frequency = 12 kHz	4.2	4.4	4.7	dB	4.
	Frequency = 16 kHz					
Metering distortion, R_L = 300 Ω, V_{AB} = 1.5 V_{pk}	Frequency = 12 kHz		–55	–40	dB	4.
	Frequency = 16 kHz					
Logic Interface						
Inputs (C1, C2, C3, CHCLK)						
V_{IL}				0.8	V	
V_{IH}		2.0				
I_{IL}	V_{IN} = 0.4 V	–150		+150	µA	
I_{IH}	V_{IN} = 2.4 V	–100		+100		
Outputs ($\overline{F}$)						
V_{OH}	I_{OUT} = –25 µA	2.4	2.8		V	
V_{OL}	I_{OUT} = 25 µA		0.2	0.4		
IMT Pin Characteristics						
IMT_i	Output impedance		1		MΩ	3.
	Offset current I_{LOOP} = 0 mA, V_{IMT} = V_{REF}	–5		+5	µA	11.
	Drive Capability					
	Ringing	–240		240		3.
	Active and Reverse Polarity	–160		160		
	Standby and Line Test	–80		80		
Ringing |IMT| current limit	V_{IN} = 0.7V, R_L = 100 Ω	180		240		4.
Line Test State |IMT| current limit	V_{IN} = 0.7V, R_L = 100 Ω	80		120		
V_{IMT} Thermal Shutdown	I_{IMT} = 1mA	2.3			V	4., 10.

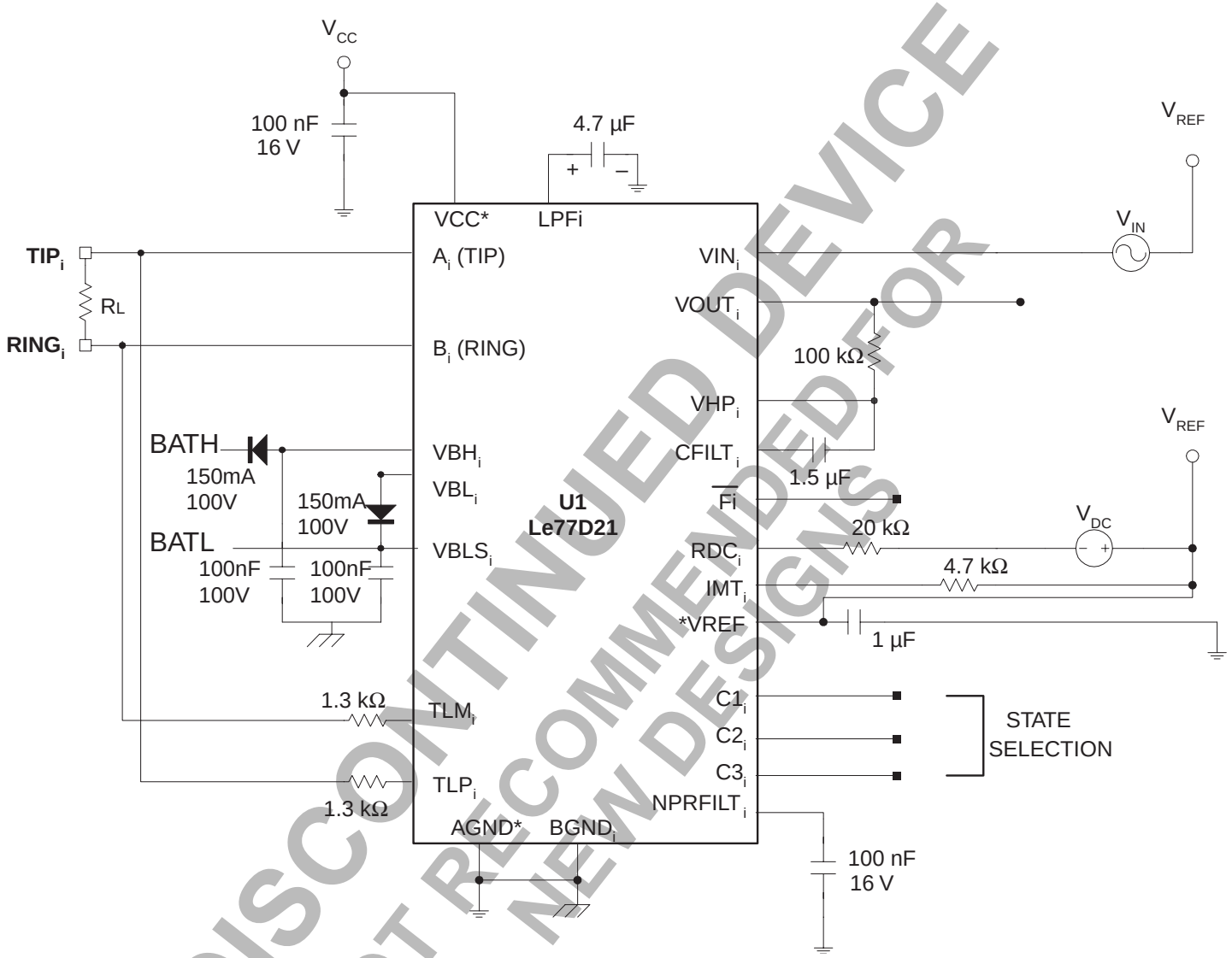
Notes:

1. *V_{AB} = Voltage between the A_i (TIP) and B_i (RING) pins.*
2. *Overload level is defined when THD = 1%.*
3. *Guaranteed by design.*
4. *Not tested in production. Parameter is guaranteed by characterization or correlation to other tests.*
5. *Layout should have less than 10 pF from pin to ground.*
6. *I_{IMT} = current coming out from IMT pin.*
7. *When On-Hook, R_{Lac} = 600 Ω*
8. *$I_{LONG} = |I_A - I_B|$.*
9. *R_L is the resistance seen between A (TIP) and B (RING) pins of the device.*
10. *The Le78D11 device cannot detect this level. Indication of Thermal Shutdown will not generate an interrupt.*
11. *For applications requiring operation below 0°C, the IMT offset current in Standby can shift up to 25 µA below -20°C with Reopen. This could result in a false off hook indication.*

    To work around this issue, increase the hook threshold on the Le78D11 device to 15 mA to avoid this off-hook detector behavior at low temperature.

TEST CIRCUIT

Per Channel



Note:

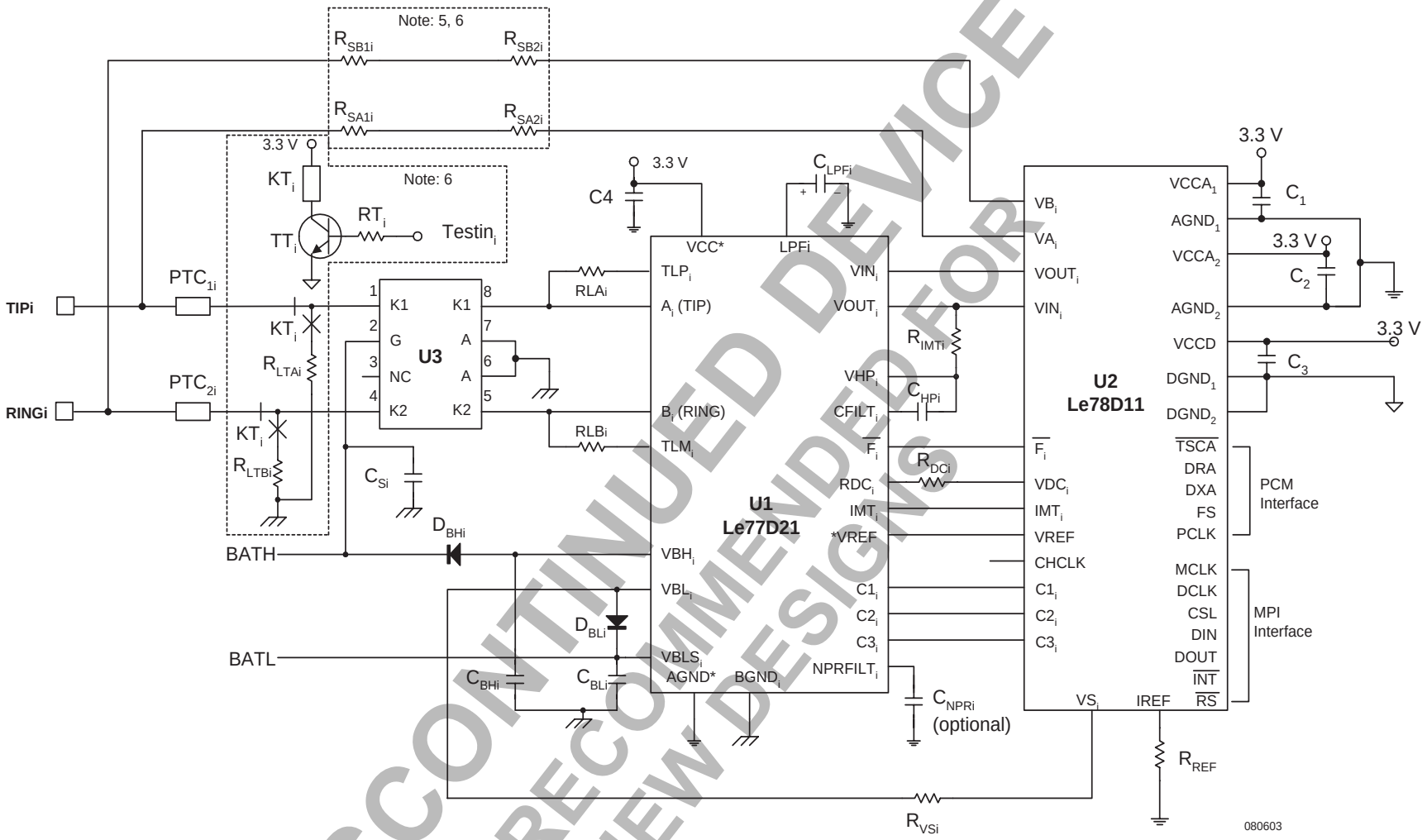
** denotes pins that are common to both channels.*

i = per channel component

NOT RECOMMENDED FOR NEW DESIGNS NOT RECOMMENDED FOR NEW DESIGNS

APPLICATION CIRCUIT

Single Channel Configuration



Notes:

1. ** denotes pins that are common to both channels.*
2. *i = per channel component*
3. *Protection is voltage tracking device*
4. *Total impedance seen by the SLIC device should be at least 200 Ω (100-Ω fuse resistance and telephone handset).*
5. *Devices used in the standard application for test diagnostic capability.*
6. *Circuitry used in the enhanced application for test diagnostic capability.*

APPLICATION CIRCUIT PARTS LIST

The following list defines the parts and part values for a low cost solution required to meet target specification limits for 70 V_{PK} ringing for two channels of the line card. The protection circuit is not included.

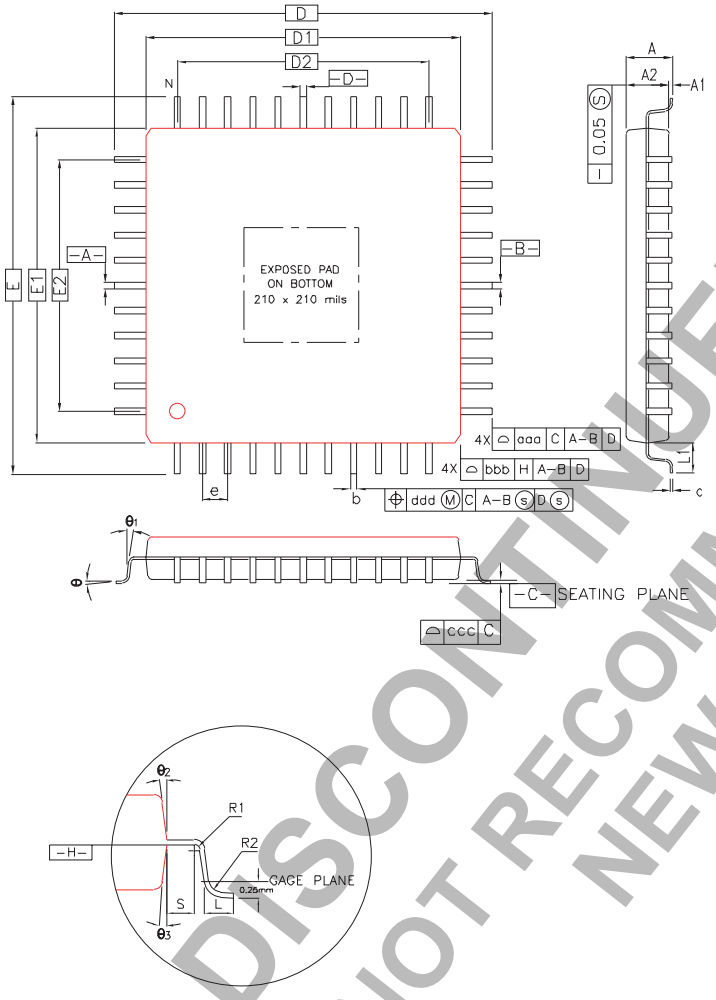
Item	Quantity (see note 1)	Type	Value	Tol.	Rating	Comments	Note
C1, C2, C3, C4	4	Capacitor	100 nF	10%	16 V	Panasonic / ECJ-1VB1C104K, 0603	2,3
C_{NPRi}	2	Capacitor	100 nF	10%	16 V	Kemet / C0805C104K8RAC (optional)	
C_{BL}	1	Capacitor	100 nF	10%	100 V	Kemet / C1210C104K1RAC	
C_{VBHi}	2	Capacitor	100 nF	10%	100 V	Kemet / C1210C104K1RAC	
C_{HPi}	2	Capacitor	1.5 µF	10%	6.3 V	Panasonic / ECJ-2YB0J155K,0805	
C_{LPFi}	2	Capacitor	4.7 µF Tantalum	10%	10 V	Kemet / T491A475K010AS	
D_{BHi}, $D_{BLi, i}$	4	Diode	150 mA		100 V	General Semiconductor / EDF1DS	
U3, U5	2	Protector	TISP61089B			Bournet	
P_{TCi}, P_{TCi}	4	PTC	50 Ω			AsiaCom / MZ2L-50R	
R_{DCi}	2	Resistor	20.0 k	1%	1/16 W	Panasonic / ERJ-3EKF2002V	
R_{REF}	1	Resistor	69.8 k	1%	1/16 W	Panasonic / ERJ-3EKF6982V	
R_{IMTi}	2	Resistor	100 k	1%	1/16 W	Panasonic / ERJ-3EKF1003V	
R_{VSi}	2	Resistor	475 k	1%	1/16 W	Panasonic / ERJ-3EKF4753V	
R_{SA1i},$R_{SB1i,}$ R_{SA2i}, R_{SB2i}	8	Resistor	237 k	1%	1/8 W	Panasonic / ERJ-8ENF2373V	
R_{LAi},R_{LBi}	4	Resistor	1.3 k	1%	0.5 W	Panasonic / ERJ-12NF1301V	
R_{LTAi},R_{LTBi}	4	Resistor	150 k	1%	1/4 W	Panasonic / ERJ-14NF1503U	3
R_{LTi}	2	Resistor	8.06 k	1%	1/4 W	Panasonic / ERJ-14NF8061U	3
KT_i	2	Relay	3.3 V		50 mW	Aromat TXS-2-3V	3
TT_i	2	Transistor	PNP			Diode Inc MMBT3904-7	3

Note:

1. *Quantities required for a complete two-channel solution.*
2. *Used in standard application test.*
3. *Used in enhanced application circuit test.*

PHYSICAL DIMENSIONS

44-Pin eTQFP



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D		12.00 BSC.	
D1		10.00 BSC.	
E		12.00 BSC.	
E1		10.00 BSC.	
R2	0.08	—	0.20
R1	0.08	—	—
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	—	0.20
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	—	—
b	0.17	0.20	0.27
e		0.80 BSC	
D2		8.00	
E2		8.00	
aaa		0.20	
bbb		0.20	
ccc		0.10	
ddd		0.20	
N		44	

NOTES:

1. CONTROLLING DIMENSION IN MILLIMETER UNLESS OTHERWISE SPECIFIED.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. "D1" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM "b" DIMENSION BY MORE TAHN 0.08 mm.
4. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 mm AND 0.5 mm PITCH PACKAGES.
5. SQUARE DOTTED LINE IS E-PAD OUTLINE.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.

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