TOSHIBA MOS INTEGRATED CIRCUIT

TC5332202 AP

SILICON GATE CMOS

32 MBIT (2,097,152 WORD BY 16 BITS) CMOS MASK ROM

DESCRIPTION

The TC5332202AP is a 33,554,432-bit Read Only Memory organized as 2,097,152 words by 16 bits.

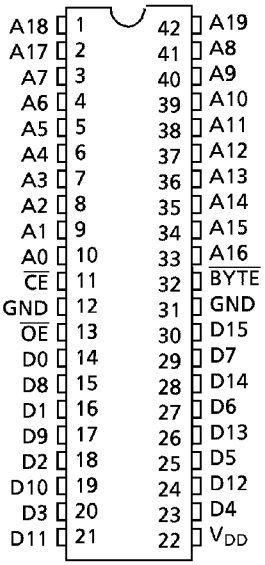
The TC5332202AP is most suitable for application such as program memory, data memory, and character generators.

The TC5332202AP is packaged in a standard 600 mil 42-pin DIP.

FEATURES

- Single 5 V Power Supply
- Access Time: 120 ns (max)
- Power Dissipation
  - Operating Current: 45 mA (max)
  - Standby Current : 100 μA (max)
- Fully Static Operation
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- TC5332202AP: DIP42−P−600

PIN ASSIGNMENT (TOP VIEW)

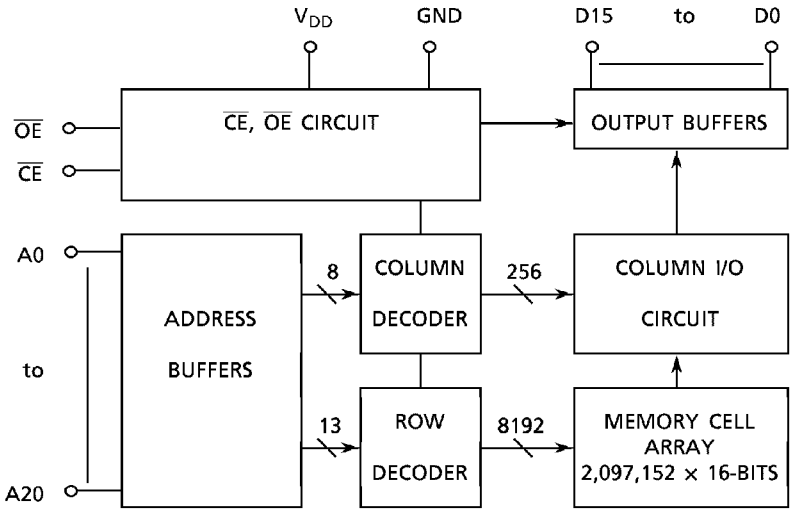


TC5332202AP

PIN NAMES

A0 to A20	Address Inputs
D0 to D15	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	D0 to D15	POWER
Read (16-Bit)	L	L	Data Out	Active
Output Deselect	L	H	High Impedance	Active
Standby	H	*	High Impedance	Standby

H: V_{IH} L: V_{IL} *: V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.5 to 7.0	V
V_{IN}	Input Voltage	− 0.5 to 7.0	V
V_{OUT}	Output Voltage	0 to V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{STG}	Storage Temperature	− 55 to 150	°C
T_{OPR}	Operating Temperature	− 10 to 70	°C
T_{SOLDER}	Soldering Temperature (10 s)	260	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = − 10° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	− 0.3	−	0.8	V

DC CHARACTERISTICS (Ta = − 10° to 70°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 to V_{DD}	−	± 5.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to V_{DD}	−	± 5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V	− 1.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V	2.0	−	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	−	2	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2 V	−	100	μA
I_{DDO1}	Operating Current	V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 120 ns I_{OUT} = 0 mA	−	50	mA
I_{DDO2}		V_{IN} = V_{DD} − 0.2 V/0.2 V t_{cycle} = 120 ns, I_{OUT} = 0 mA	−	45	mA

CAPACITANCE (f = 1 MHz, Ta = 25°C, V_{DD} = 5.0 V)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0 V	−	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	−	15	pF

Note: This parameter is periodically sampled and is not tested for every component.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = − 10° to 70°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CYC}	Cycle Time	120	–	ns
t_{ACC}	Address Access Time	–	120	ns
t_{CE}	Chip Enable Access Time	–	120	ns
t_{OE}	Output Enable Access Time	–	60	ns
t_{CEE}	Output Enable Time from $\overline{CE}$	0	–	ns
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	ns
t_{CED}	Output Disable Time from $\overline{CE}$	–	45	ns
t_{OED}	Output Disable Time from $\overline{OE}$	–	35	ns
t_{OH}	Output Hold Time	5	–	ns

AC TEST CONDITIONS

Output Load	: 100 pF + 1 TTL
Input Levels	: 0.6 V/2.4 V
Timing Measurement Reference Levels	Input : 0.8 V/2.2 V
	Output: 0.8 V/2.2 V
Input Rise and Fall Time	: 5 ns

16-BIT READ MODE