PRELIMINARY

Notice This is not a final specification
Some parametric limits are subject to change

MH51232FRN-10,-12,-15

16777216-BIT(524288-WORD BY 32-BIT)CMOS FLASH MEMORY

DESCRIPTION

The Mitsubishi MH51232FRN are high-speed 16777216-bit CMOS Flash Memories. They are suitable for the applications with microprocessor micro-controller where on board reprogramming is required. The MH51232FRN are fabricated by N-channel double polysilicon gate for memory and CMOS technology for peripheral circuits.

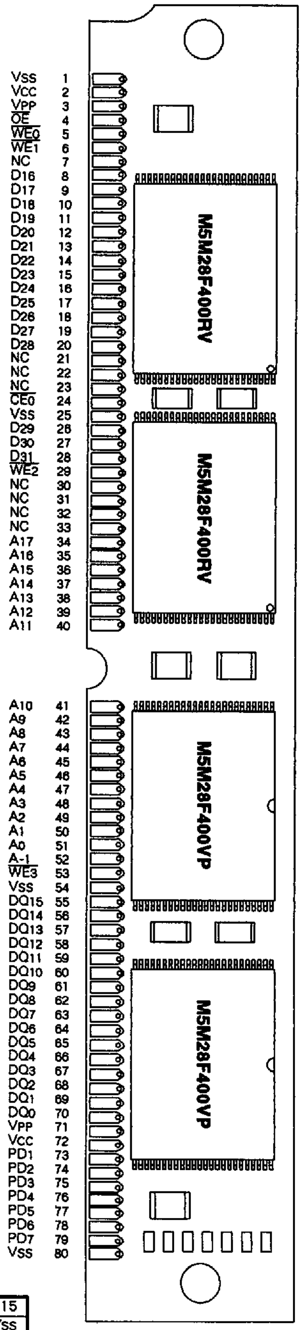
FEATURES

- 524288-word by 32-bit organization
- Utilizes industry standard 512K × 8 FLASH in (TSOP) (I)
- Access time
  - MH51232FRN-10 ································ 100ns (max.)
  - MH51232FRN-12 ································ 120ns (max.)
  - MH51232FRN-15 ································ 150ns (max.)
- Low power consumption Active ·············· 330W (max.)
  - Stand-by ········ 11mW (max.)
- Power supply voltage $V_{CC} = 5V \pm 0.5V$
  - $V_{PP} = 12V \pm 0.6V$
- Chip erase or block erase
- Block Address (A_{13}~A_{17})
- Auto program or auto erase (chip/block)
- Program/erase operation controlled by software command
- Program/erase pulses controlled by an embedded timer
- 10000 program/erase cycles
- Tri-state output buffer
- TTL-compatible input and output in read and write mode
- Contained device-identifier code
- Incorporated data-protection
- 80pin Single in line module
- Includes decoupling capacitors (0.15 μF × 8)
- Gold plating contact

APPLICATION

Micro-computer systems and peripheral equipments

PIN CONFIGURATION (TOP VIEW) (Single side)



	-10	-12	-15
PD1	Vss	Vss	Vss
PD2	Vss	Vss	Vss
PD3	Vss	Vss	Vss
PD4	NC	NC	NC
PD5	NC	Vss	NC
PD6	NC	NC	Vss
PD7	Vss	Vss	Vss

Outline 80N9-M

NC : NO CONNECTION

FUNCTION

MH51232FRN are set to the Read-only mode or Read-write mode by applying the voltage of V_{PPL} or V_{PPH}, respectively, to V_{PP} pin. In Read-only mode, three operation modes, Read. Output disable and Stand-by are accessible. While, in Read-write mode, four operation modes, Read, Output disable, Stand-by and Write are functional.

Read

Set $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$, $\overline{OE}$ and $\overline{WE}$ and address signals to the address inputs(A_{-1}~A_{17}) make the data contents of the designated address location available at data input/output(D_0 ~D_{31}).

Output Disable

When $\overline{OE}$ is at high level, output from the devices is disabled. Data input/output are in a high-inpedance (High-Z) state.

Stand-by

When $\overline{CE}$ is high level, the devices is in the stand-by mode and its power consumption is substantially reduced. Data input/output are in a high-inpedance (High-Z) state.

Write

Software command accomplishes program and erase operations via the command latch in the device, When high voltage is supplied to V_{PP}. The contents of the latch serve as input to the internal controller. The controller output dictates the function of device. The command latch is written by bringing $\overline{WE}$ to low level, while $\overline{CE}$ is at low level and $\overline{OE}$ is at high level. Addresses and data are latched on the rising edge of $\overline{WE}$. Standard micro-processor write timings are used.

DATA PROTECTION

1. Power Supply Voltage
   When the power supply voltage (Vcc) is less than 3.0V, the device is set to the Read-only mode.
2. Write Inhibit
   In the cases, as below, write mode is not set.
   1) When $\overline{CE}$ and $\overline{OE}$ are terminated to the low level.
   2) From 100ns through 5 μs after the later rising edge of $\overline{WE}$ for program.
   3) From 100ns through 5ms after the later rising edge of $\overline{WE}$ for erase.
3. Over-erase Protection
   Just after powering up, erase command input is refused and erase operation is not executed. Once byte-program is performed or verified data is not FFH in the erase-verify mode, successive command input for erase will be accepted. Because of this, it is applicable to the case of multi-chip erasing simultaneously.

SOFTWARE COMMAND

When V_{PP} is low ($V_{PP} = V_{PPL}$), the contents of command latch are fixed to 00H, and the device is in read-only mode. When V_{PP} is high ($V_{PP} = V_{PPH}$), the device enters read/write mode. The device operations are selected by writing specific software command into the command latch.

Read Command

The device is in read mode after writing Read Command (00H) to the command latch. The device continues to be in read mode until the other commands are written. When V_{PP} powers-up to high voltage($V_{PP} = V_{PPH}$), the default contents of the command latch is 00H. So it is ensured that the false afteration of memory data does not occur during V_{PP} power transition.

Program Command

Program Command is the command for byte-program or word-program, and program is initiated by twice of write cycles. Program Command (40H) is written to the command latch in first write cycle, and the address and data to be programmed are latched in second write cycle. Then the address and data are latched on the rising edge of $\overline{WE}$ pulse. The program operation is initiated at the rising edge of $\overline{WE}$ in second write cycle, and terminates in 10 μs, controlled by the internal timer.

Program Verify Command

Following byte program or word program, the programmed byte or word must be verified. The program-verify is initiated by writing Program Verify Command (C0H) to the command latch. After writing Program Verify Command, programmed data is verified in read mode. Then the address information is not needed.

Chip Erase Command

Chip Erase Command is the command for chip-erase, and chip-erase is initiated by writing twice of the Erase Command (20H) consecutively to the command latch. The erase operation is initiated with the rising edge of the $\overline{WE}$ pulse and terminates in 9.5ms, controlled by the internal timer. This two-step sequence for chip-erase prevents from erasing accidentally.

Block Erase Command

Block Erase Command is the command for block-erase, and block-erase is initiated by twice of write cycles. Block-erase Command (60H) is written to the command latch in first write cycle, and the block addressed (A_{13}~A_{17}) and Command (60H) are latched in second write cycle. The erase operation is initiated with the rising edge of the $\overline{WE}$ pulse and terminates in 9.5ms, controlled by the internal timer.

Erase Verifiv Command
Following each erase, all bytes or words must be verified. The erase verify is initiated by writing Erase Verify Command (A0H) to the command latch, while the address to be verified is latched on the rising edge of the $\overline{WE}$ pulse. The erase verify command must be written to the command latch and each address is latched before each byte word is verified. The operation continues for each byte or word until a byte or word is not erased, or the last address is accessed.

Auto Chip Erase Command
Auto Chip Erase Command is the command for auto chip-erase, and auto chip-erase is initiated by writing twice of the Erase Command (30H) consecutively to the command latch. The erase operation is initiated with the rising edge of the $\overline{WE}$ pulse and terminates automatically. So it is not necessary to verify. And the complete of erase can be indicated by status polling.

Auto Block Erase Command
Auto Block Erase Command is the command for auto block-erase, and auto block-erase is initiated by twice of write cycles. Auto Block-erase Command (20H) is written to the command latch in first write cycle, and the block addresses (A_{13}~A_{17}) and Command (D0H) are latched in second write cycle. The erase operation is inintiated with the rising edge of the $\overline{WE}$ pulse and terminates, automatically. So it is not necessary to verify. And the completion of erase can be indicated by status polling.

Status Polling
Status Polling is the indication of the end of auto-erase. During the auto-erase, if read operation is done, the data of D7 is "0". When auto-erase is completed, the D7 is "1".

Auto Program Command
Auto Program Command is the command for auto byte-program or word-program, and program is initiated by twice of write cycles. Program Command (10H) is written to the command latch in first write cycle, and the address and data to be programmed are latched in second write cycle. Then the address and data are latched on the rising edge of $\overline{WE}$ pulse. The program operation is initiated at the rising edge of $\overline{WE}$ in second write cycle, and terminates, automatically. So it is not necessary to verify. And the complete of program can be indicated by data polling.

Data Polling
Data Polling is the indication of the end of auto-program. During the auto-program, if read operation is done, the data of D7 is the inverse of written datum. When auto-program is completed, the true datum will become valid.

Reset Command
Reset Command is the command to safely abort the erase or program sequences. Following erase or program command in first write cycle, the operation is aborted safely by writing the two consecutive Reset Commands (FFH). Then the device enters read mode without altering memory contents.

Read Device Identifier Code
Though PROM programmers can normally read device identifier codes by raising A_9 to high voltage, multiplexing high voltage onto address lines is not desired for micro-processor system. It is an other means to read device identifier codes that Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

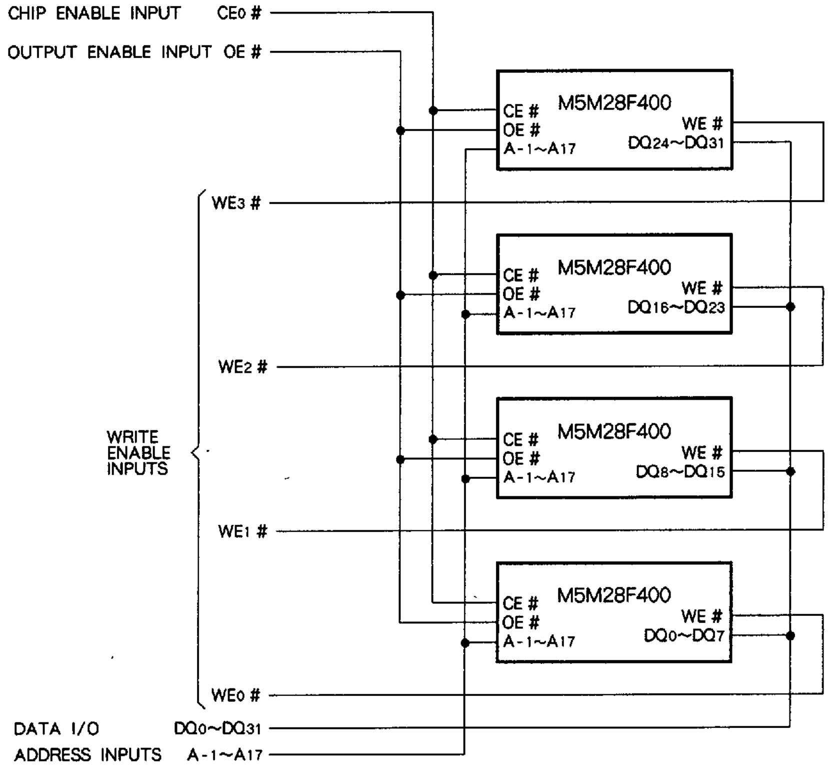
The device identifier mode allows the reading of a binary code from the device that identifies the manufacturer and device type. The PROM programmers read the manufacturer code and device code by raising A_9 to high valtage, and automatically select the corresponding programming algorithm.

MODE SELECTION

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	Data I/O
						D_0~D_{31}
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	Hi-Z
	Stand-by	V_{IH}	X	X	V_{PPL}	Hi-Z
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	Hi-Z
	Stand-by	V_{IH}	X	X	V_{PPH}	Hi-Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	Data in

Note 1 : X can be V_{IL} or V_{IH}

BLOCK DIAGRAM



ABSOLUTE MAXMUM RATINGS

Symbol	Parameter	Test conditions	Ratings	Unit
V_{I1}	All input or output voltage expect V_{PP}/A_9	With respect to Ground	- 0.6~7	V
V_{I2}	V_{PP} supply voltage		- 0.6~14.0	V
V_{I3}	A_9 supply voltage		- 0.6~13.5	V
T_{opr}	Operating temperature		- 10~80	℃
T_{stg}	Storage temperature		- 40~100	℃

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$)	Ta = 25℃, f = 1MHz			80	pF
C_{OUT}	Output capacitance	V_{in} = V_{out} = 0V			30	pF

SOFTWARE COMMAND DEFINITION

Command	bus cycle	First bus cycle			Second bus cycle		
		Mode	Address	Data	Mode	Address	Data
Read	1	Write	X	00H	———	———	———
Program	2	Write	X	40H	Write	Program Address	Program Data.
Auto Program	2	Write	X	10H	Write	Program Address	Program Data
Program Verify	2	Write	X	C0H	Read	X	Verify Data
Chip Erase	2	Write	X	20H	Write	X	20H
Block Erase	2	Write	X	60H	Write	Block Address	60H
Auto Chip Erase	2	Write	X	30H	Write	X	30H
Auto Block Erase	2	Write	X	20H	Write	Block Address	D0H
Erase Varify	2	Write	Verify Address	A0H	Read	X	Verify Data
Reset	2	Write	X	FFH	Write	X	FFH
Read device identifier code	2	Write	X	90H	Read	ADI	DDI

Note 2 : Write and read mode are defined in mode selection table.
3 : ADI = Address of Device identifier : A0 = 0 for manufacture code, A0 = 1 for device code.
DDI = Data of device identifier : 1CH for manufacture code, D6H for device code.
X = : X can be V_{IL} or V_{IH}

DEVICE IDENTIFIER CODE

Pins / Code	A_0	D_{31}	D_{30}	D_{29}	D_{28}	D_{27}	D_{26}	D_{25}	D_{24}	D_{23}	D_{22}	D_{21}	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	Hex Data
	A_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Manufacture Code	V_{IL}	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	1C1CH
Device Code	V_{IH}	1	1	0	1	0	1	1	0	1	1	0	1	0	1	1	0	D6D6H

Note 4 : A_9 = 11.5V~13.0V
A_1~A_8, A_{10}~A_{17}, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
A_{-1} = V_{IL}
V_{CC} = V_{PP} = 5V ± 10%

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 0.5V, unless othrwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
I_{LI}	Input leakage current	$0 \leqq V_{IN} \leqq V_{CC}$			40	μA
I_{LO}	Output leakage current	$0 \leqq V_{OUT} \leqq V_{CC}$			40	μA
I_{SB1}	Vcc standby current	$V_{CC} = 5.5V$, $\overline{CE} = V_{IH}$			4	mA
I_{SB2}		$V_{CC} = 5.5V$, $\overline{CE} = V_{CC} \pm 0.2V$			400	μA
I_{CC1}	Vcc active read current	$V_{CC}=5.5V$, $\overline{CE}=V_{IL}$, f=10MHz, $I_{OUT}=0mA$			280	mA
I_{CC2}	Vcc program current	$V_{PP} = V_{PPH}$			120	mA
I_{CC3}	Vcc erase current	$V_{PP} = V_{PPH}$			120	mA
I_{PP1}	VPP read current	$0 \leqq V_{PP} \leqq V_{CC}$			40	μA
		$V_{CC} < V_{PP} \leqq V_{CC} + 1.0V$			400	
		$V_{PP} = V_{PPH}$			400	
I_{PP2}	VPP program current	$V_{PP} = V_{PPH}$			200	mA
I_{PP3}	VPP erase current	$V_{PP} = V_{PPH}$			200	mA
V_{IL}	Input low voltage		−0.5		0.8	V
V_{IH}	Input high voltage		2.0		Vcc+0.5	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH1}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
V_{OH2}		$I_{OH} = -100\mu A$	Vcc-0.4			
V_{PPL}	VPP during read-only mode		0		Vcc+1.0	V
V_{PPH}	VPP during read/write mode		11.4	12.0	12.6	V

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 0.5V, unless otherwise noted)

Read-Only Mode

Symbol	Parameter	MH51232FRN-10 Min	MH51232FRN-10 Max	MH51232FRN-12 Min	MH51232FRN-12 Max	MH51232FRN-15 Min	MH51232FRN-15 Max	Unit
t_{RC}	Read cycle time	100		120		150		ns
$t_{a(AD)}$	Address access time		100		120		150	ns
$t_{a(CE)}$	Chip enable access time		100		120		150	ns
$t_{a(OE)}$	Output enable access time		50		60		70	ns
t_{CLZ}	Chip enable to output in low Z	0		0		0		ns
t_{OLZ}	Ouput enable to output in low Z	0		0		0		ns
t_{DF}	Output enable high to output in high Z		25		30		35	ns
t_{OH}	Output hold from $\overline{CE}$,$\overline{OE}$, addresses	0		0		0		ns
t_{WRR}	Write recovery time before read	6		6		6		μs

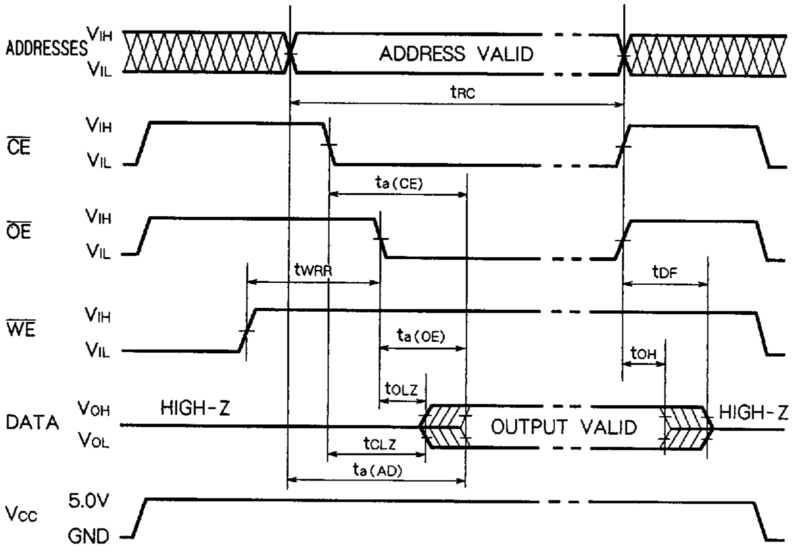
Note 5 : VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

Read/Write Mode

Symbol	Parameter	Limits						Unit
		MH51232FRN-10		MH51232FRN-12		MH51232FRN-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	100		120		150		ns
t_{AS}	Address set-up time	30		30		30		ns
t_{AH}	Address hold time	40		50		70		ns
t_{DS}	Data set-up time	50		50		50		ns
t_{DH}	Data hold time	30		30		30		ns
t_{WRR}	Write recovery time before read	6		6		6		μs
t_{RRW}	Read recovery time before write	0		0		0		μs
t_{CS}	Chip enable set-up time before write	5		5		5		ns
t_{CH}	Chip enable hold time	45		55		75		ns
t_{WP}	Write pulse width	40		50		60		ns
t_{WPH}	Write pulse width high	60		70		90		ns
t_{DP}	Duration of programming operation	10		10		10		μs
t_{DE}	Duration of erase operation	9.5		9.5		9.5		ms
t_{CESP}	Chip enable set-up time before status polling	100		100		100		ns
t_{CEDP}	Chip enable set-up time before data polling	100		100		100		ns
t_{DAEC}	Duration of auto-chip erase operation	0.5	30	0.5	30	0.5	30	s
t_{DAEB}	Duration of auto-block erase operation	0.5	30	0.5	30	0.5	30	s
t_{DAP}	Duration of auto-program operation	10	400	10	400	10	400	μs
t_{VSC}	V_{PP} set-up time to chip enable low	1		1		1		μs

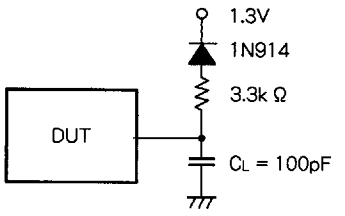
Note 6 : a. Read timing parameters during read/write mode are the same as during read-only mode.
b. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC WAVEFORMS FOR READ OPERATIONS

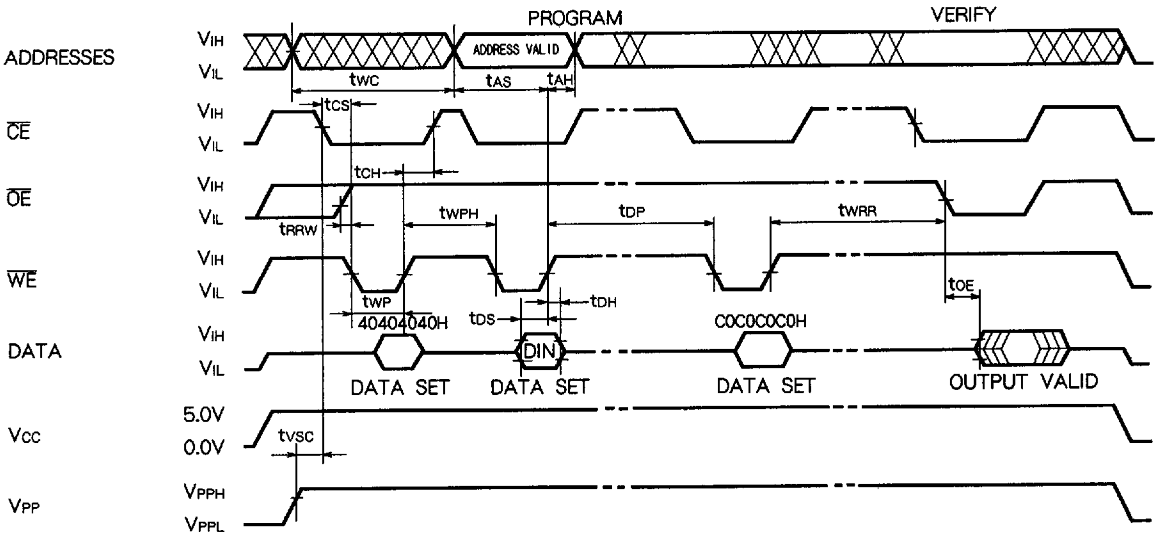


TEST CONDITIONS
FOR AC CHARACTERISTICS

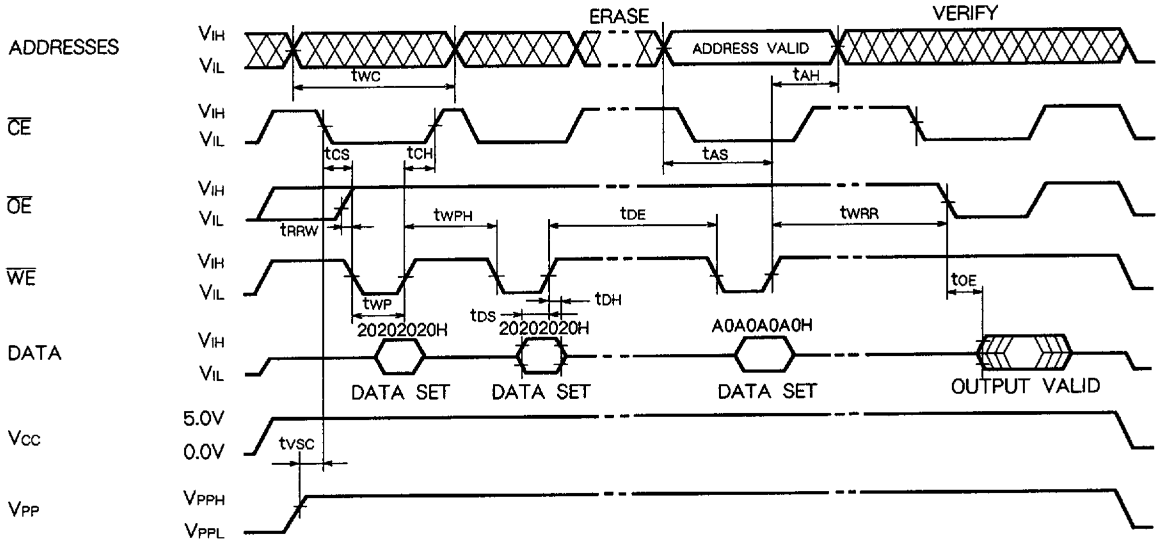
Input voltege : $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall times : ≦ 10ns
Reference voltage
at timing measurement : 1.5V
Output load : 1TTL gate + C_L
(= 100pF)
or



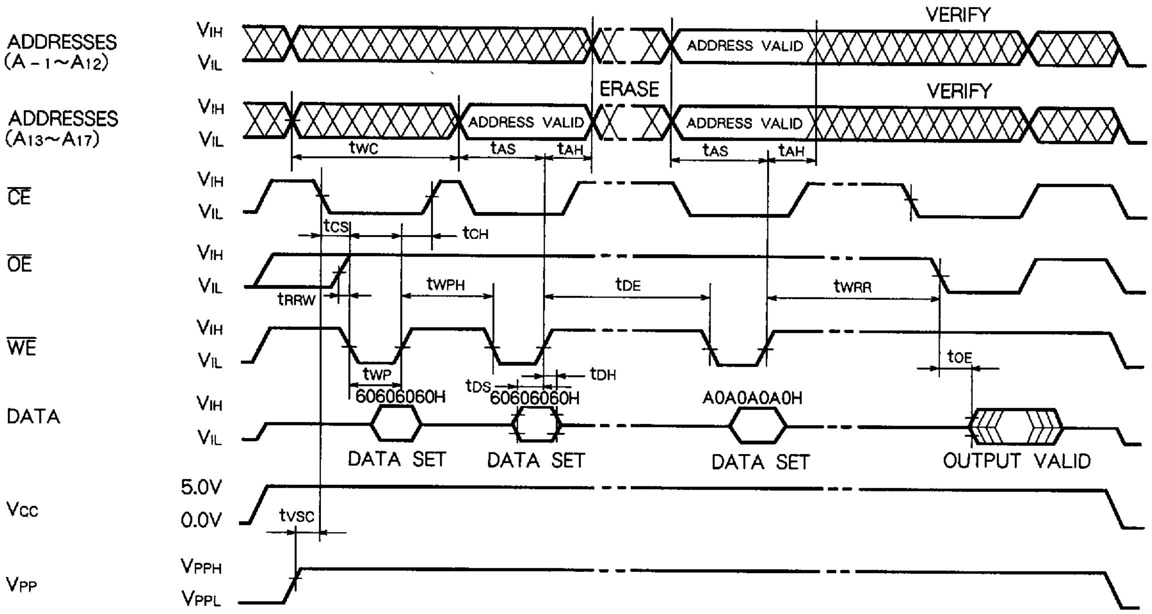
AC WAVEFORMS FOR PROGRAM OPERATION



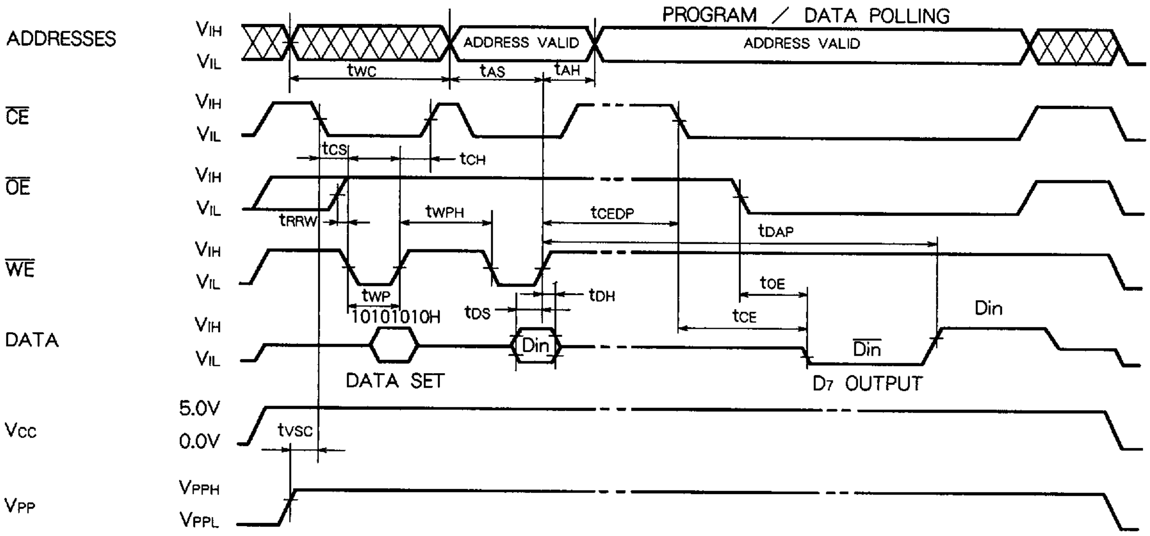
AC WAVEFORMS FOR CHIP ERASE OPERATION



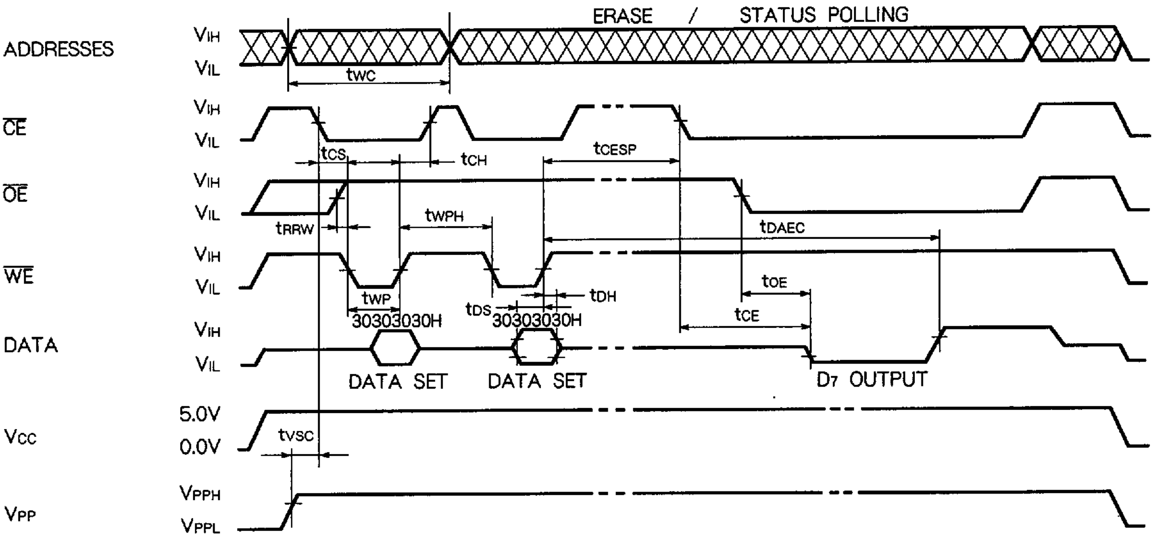
AC WAVEFORMS FOR BLOCK ERASE OPERATION



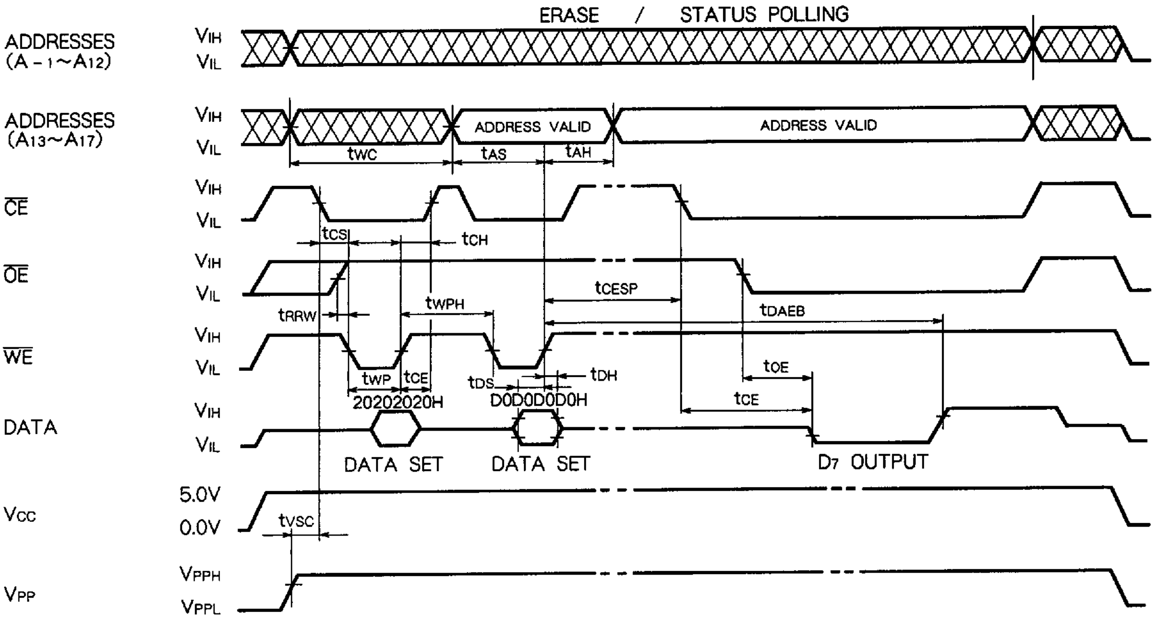
AC WAVEFORMS FOR AUTO PROGRAM OPERATION



AC WAVEFORMS FOR AUTO CHIP ERASE OPERATION

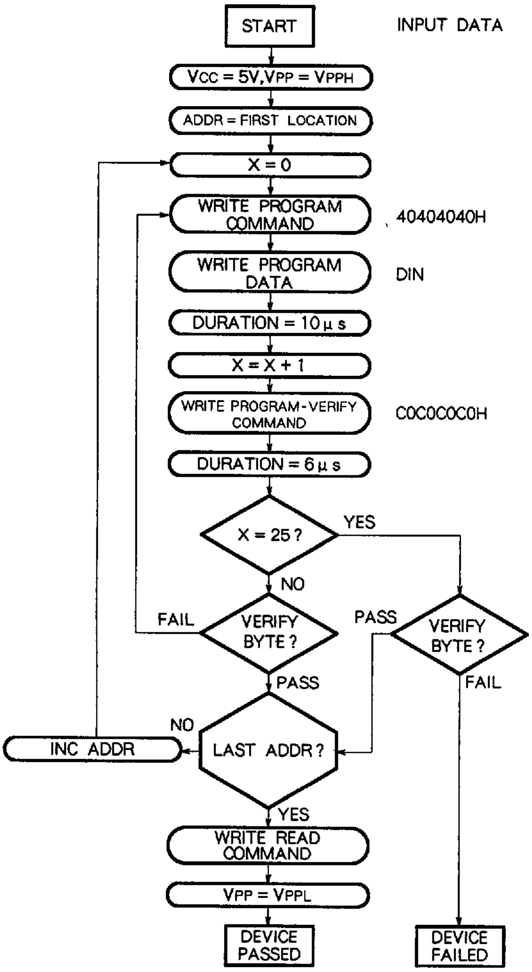


AC WAVEFORMS FOR AUTO BLOCK ERASE OPERATION



PROGRAMMING AND ERASE ALGORITHM FLOW CHART

PROGRAM :



ERASE :