

FEATURES

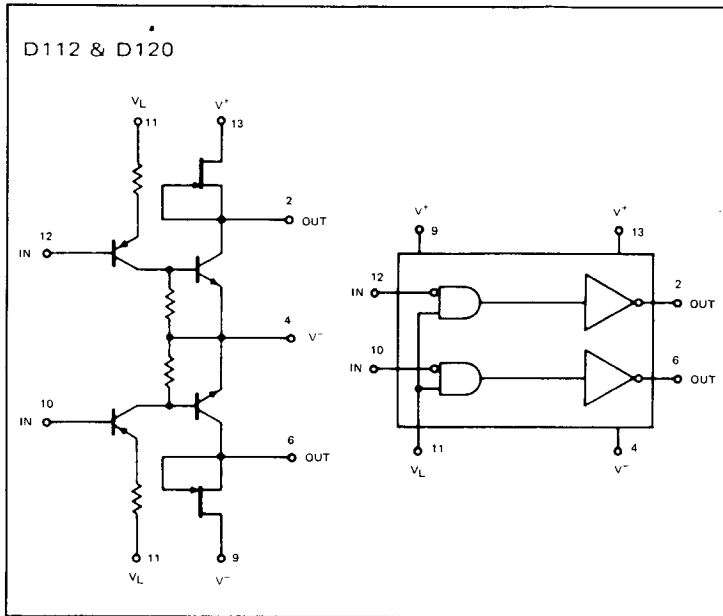
- Two separate channels
- J-FET Collector Pull-up
- Interfaces 5V Logic
- Two switching speeds to choose from

GENERAL DESCRIPTION

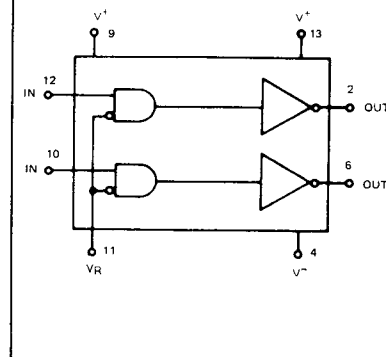
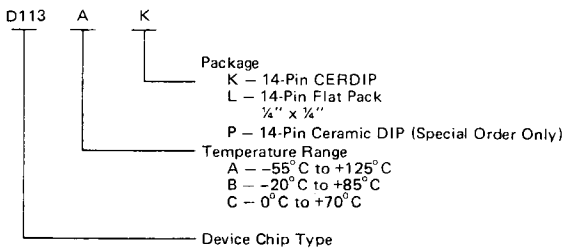
This series contains 2 separate channels each with J-FET collector pull-up, in one package. Two switching speeds are provided for speed-power ratio selection.

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SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwg DD, FD-2, JD)



ORDERING INFORMATION



D112/113/120/121

INTERSI

Pos. Supply to Emitter ($V^+ - V^-$)	33V
Output to Emitter ($V_{OUT} - V^-$)	33V
Logic Supply to Emitter ($V_L - V^-$)	30V
Ref. to Emitter ($V_R - V^-$)	31V
Input to Ref. ($V_{IN} - V^-$)	2V
Ref. to Input ($V_R - V_{IN}$)	6V
Logic Supply to Input ($V_L - V_{IN}$)	$\pm 6V$
Current (any pin)	30mA

Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Dissipation (Note)	750mW
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70 C. For higher temperatures, derate 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

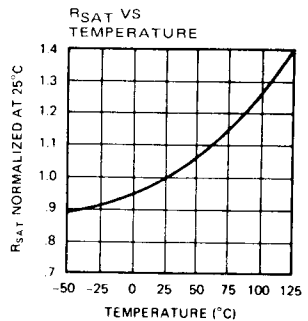
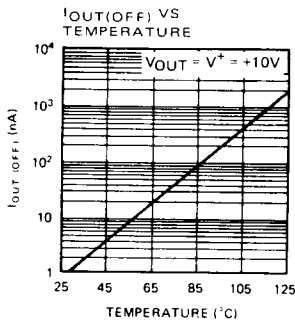
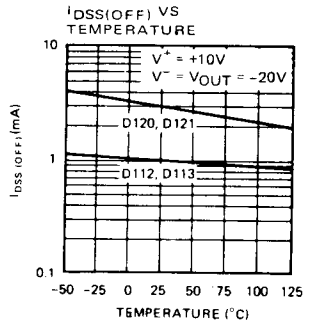
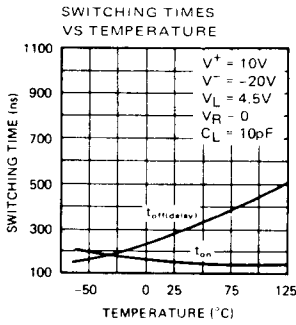
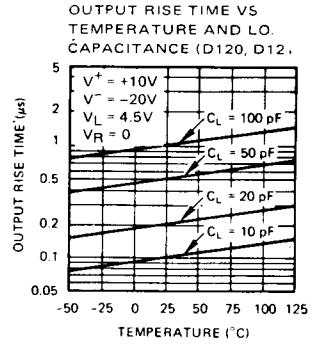
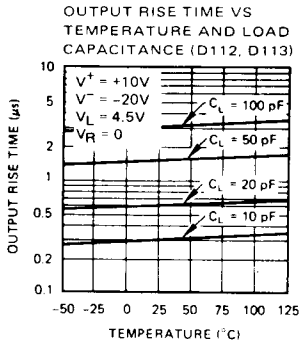
Test conditions unless otherwise specified are as follows: $V^- = -20V$, $V^+ = +10V$, $I_{OUT} = 0$, $V_L = 4.5V$, $V_R = 0$. Output and power supply measurements based on specified input conditions.

		PARAMETER (NOTE)	LIMIT			UNITS	CONDITION	
			-55°C	25°C	125°C			
INPUT	D112 D120	$I_{IN(ON)}$	1.5	1.5	1.2	MAX	mA	$V_{IN} = 0.4V$
		$I_{IN(OFF)}$	1.0	1.0	20		μA	$V_{IN} = 4.1V$
	D113 D121	$V_{IN(ON)}$	1.3	1.0	0.8	MAX	V	$I_{IN} = 1 mA$
		$I_{IN(OFF)}$	1.0	1.0	100		μA	$V_{IN} = 0.4V$
OUTPUT	D112 D113	$I_{DSS(OFF)}$	-2.2	-1.8	-1.8	MAX	mA	$V_{OUT} = -20V$ $V_{EE} = -20V$
		$I_{DSS(OFF)}$	-0.6	-0.4	-0.4	MIN		
	D120 D121	$I_{DSS(OFF)}$	-7.5	-5.7	-5.1	MAX		
		$I_{DSS(OFF)}$	-3.2	-3.0	-2.0	MIN		
	ALL	$V_{OUT(OFF)}$	9.9	9.9	9.8	MIN	V	$I_{OUT} = -10 \mu A$
		$V_{OUT(ON)}$	-19.2	-19.2	-19.0	MIN	V	$I_{OUT} = 1 mA$
POWER SUPPLY	D112	$I_{L(ON)}$		2.0		MAX	mA	One channel ON
		$I_{CC(ON)}$		1.8				
		$I_{EE(ON)}$		3.8				
	D120	$I_{L(ON)}$		2.0				
		$I_{CC(ON)}$		5.7				
		$I_{EE(ON)}$		7.7				
	D113	$I_{R(ON)}$		0.5				
		$I_{CC(ON)}$		1.8				
		$I_{EE(ON)}$		2.8				
	D121	$I_{R(ON)}$		0.5				
		$I_{CC(ON)}$		5.7				
		$I_{EE(ON)}$		6.7				
	ALL	$I_{L(OFF)}$		250				
		$I_{R(OFF)}$		150				
		$I_{CC(OFF)}$		50				
		$I_{EE(OFF)}$		250				
SWITCHING TIMES	D112 D113	t_{OFF}		1.5		MAX	μs	(See Switching Times)
		t_{ON}		0.25				
	D120 D121	t_{OFF}		0.60				
		t_{ON}		0.25				

NOTE: (OFF) and (ON) subscripts refer to the conduction state of the driver

TYPICAL PERFORMANCE CURVES

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APPLICATION TIPS

The recommended resistors for interfacing with RTL, DTL, and T²L Logic is shown in figures 1 and 2.

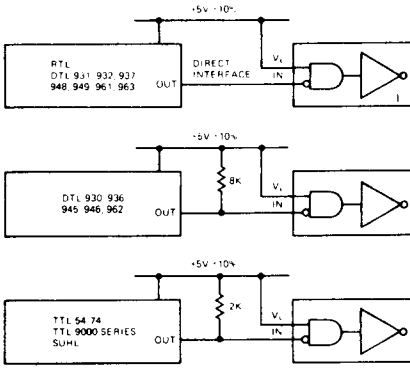


Figure 1. D112 and D120 Interface

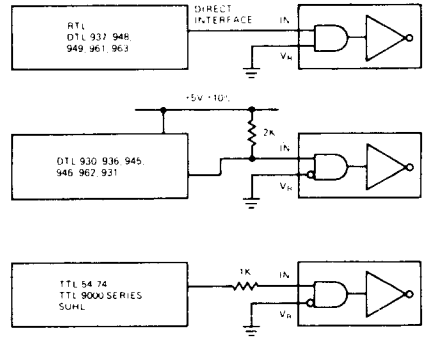
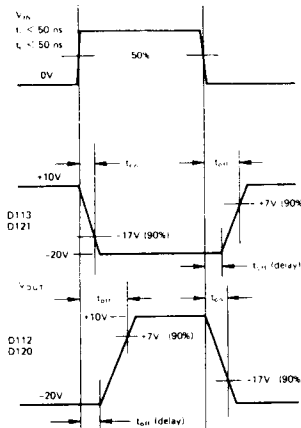


Figure 2. D113 and D121 Interface

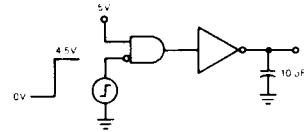
Enable Control

The V_R and V_L pins can be used as a STROBE or an ENABLE control. The requirements for the enable driver are as follows: I_L (ON) X no. of channels used for the D112 & D120 and I_R (ON) X no. of channels used for the D113 & D121. The voltage at V_L must be greater than the voltage at V_{IN} by at least +4V.

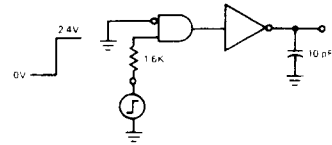
SWITCHING TIMES



D112, D120



D113, D121



Circuit Diagrams