SONY CXD8069G

Preliminary

4:2:2 D1 Video Decoder

Outline

The CXD8069G is Bi-CMOS IC for decoding the signals which conforms to 4:2:2 digital video parallel interface standardized in SMPTE and EBU formats. As for the band width of input data, either 10 bits or 8 bits are available for this IC. 10 bits data can be rounded to 8 bits data for output. With its built-in FIFO for jitter absorption, the CXD8069G can remove the jitter from an input signal by in-putting the system clock.

Features

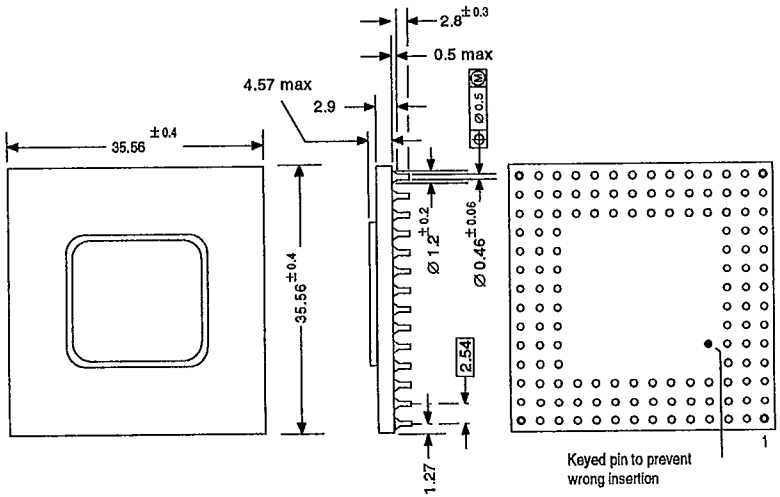
- Input: 10(8) bit word
  4:2:2 Digital Video
  (Conforming to SMPTE RP-125 format document and EBU tech 3246 format document).
- Output:

1.	Y output	10 bit (13.5MHz rate)
	Cb, Cr Multiplex output	10 bit (13.5MHz rate)
2.	Y Output	10 bit (13.5MHz rate)
	Cb Output	10 bit (6.75MHz rate)
	Cr Output	10 bit (6.75MHz rate)

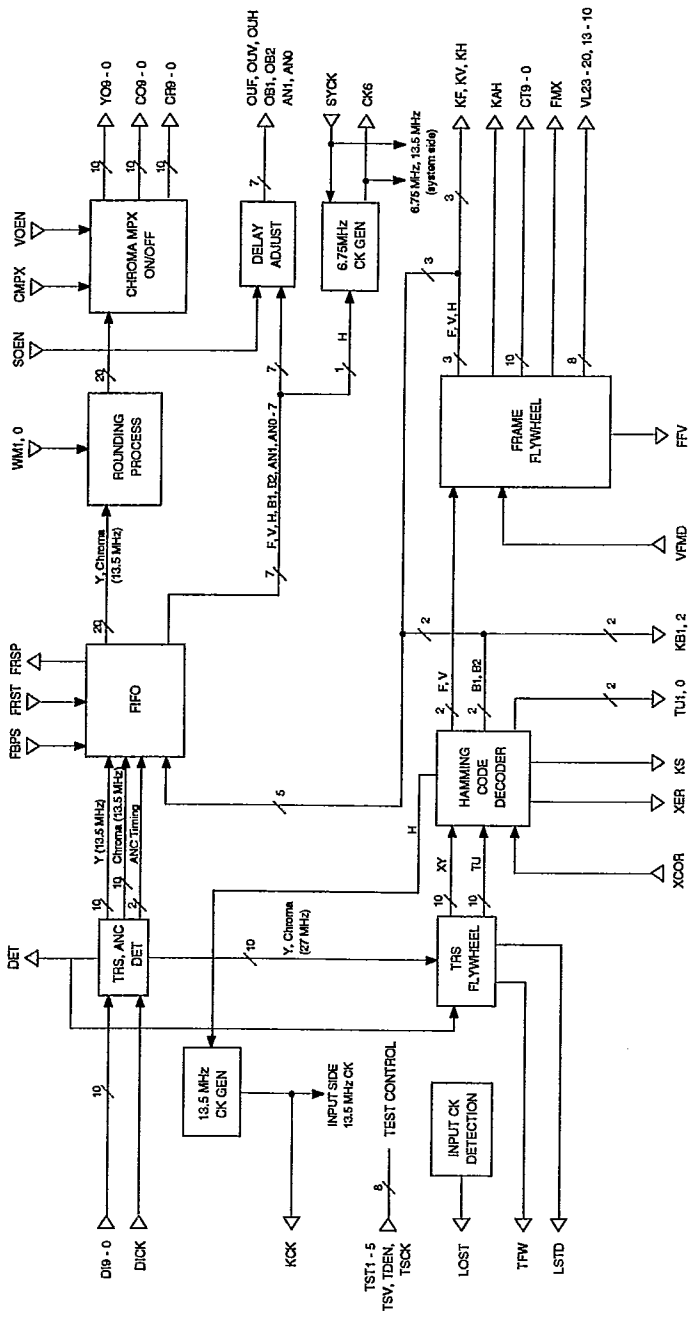
- Detection of header of an ancillary data.
- Flywheel effect on F, V, H information in the TRS (Timing Reference Signal).
- Equipped with built-in FIFO (For jitter absoption) for clock interchange from input side to system side.
- Automatic 525/625 detection, sense the existence of 27MHz input clock.
- Output the line number on which V information in TRS is falling in 525 mode.
- Provide the timing signal which corresponds to the trailing edge of analog H-sync.
- Output the value of internal frame counter.

Package Outline

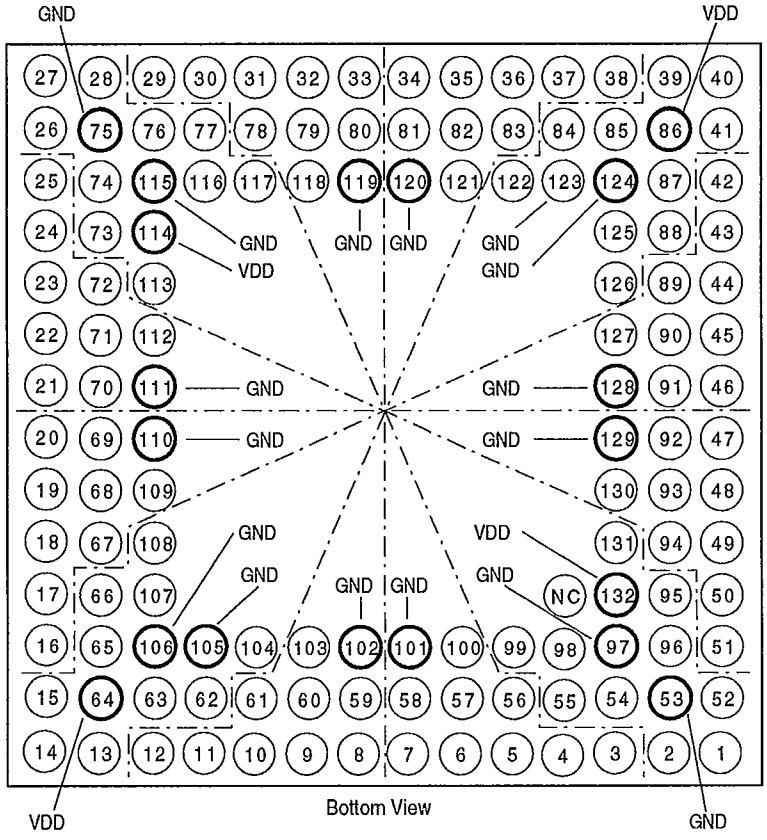
132 Pin PGA.



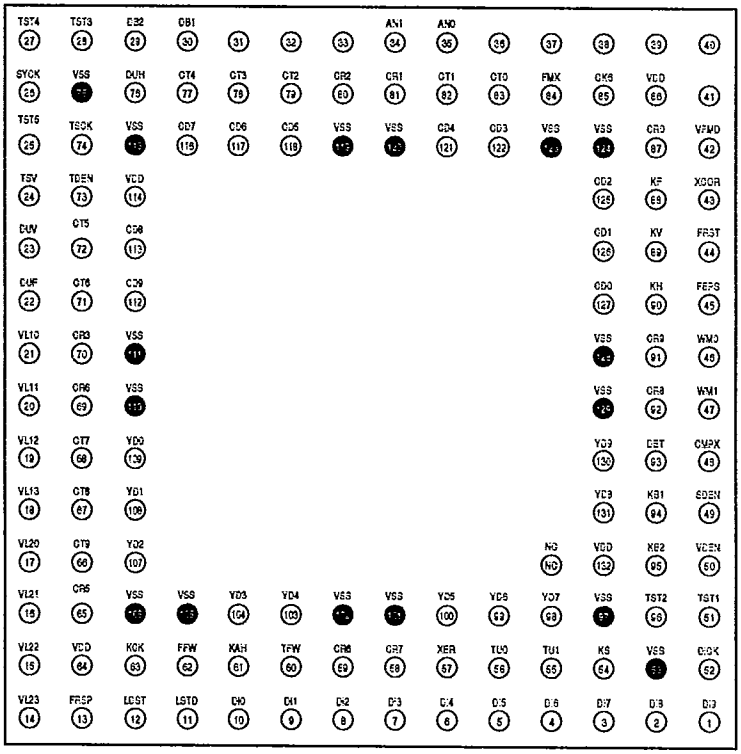
Block Diagram



Pin Configuration (Bottom View)



Package PGA132



Bottom View

CXD8069G Pin Assignment

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I	D19	36	-	--	71	I/O	CT6	106	-	Vss
2	I	D18	37	-	--	72	I/O	CT5	107	O	YD2
3	I	D17	38	-	--	73	I	TDEN	108	O	YD1
4	I	D16	39	-	--	74	I	TSCK	109	O	YD0
5	I	D15	40	-	--	75	-	Vss	110	-	Vss
6	I	D14	41	-	--	76	O	OUH	111	-	Vss
7	I	D13	42	I	VFMD	77	I/O	CT4	112	O	CD9
8	I	D12	43	I	XCOR	78	I/O	CT3	113	O	CD8
9	I	D11	44	I	FRST	79	I/O	CT2	114	-	Vcc
10	I	D10	45	I	FBPS	80	O	CR2	115	-	Vss
11	O	LSTD	46	I	WM0	81	O	CR1	116	O	CD7
12	O	LDST	47	I	WM1	82	I/O	CT1	117	O	CD6
13	O	FRSP	48	I	CMPX	83	I/O	CT0	118	O	CD5
14	O	VL23	49	I	SDEN	84	I/O	FMX	119	-	Vss
15	O	VL22	50	I	VDEN	85	O	CK6	120	-	Vss
16	O	VL21	51	I	TST1	86	-	Vcc	121	O	CD4
17	O	VL20	52	I	DICK	87	O	CR0	122	O	CD3
18	O	VL13	53	-	Vss	88	O	KF	123	-	Vss
19	O	VL12	54	O	KS	89	O	KV	124	-	Vss
20	O	VL11	55	O	TU1	90	O	KH	125	O	CD2
21	O	VL10	56	O	TU0	91	O	CR9	126	O	CD1
22	O	DUF	57	O	XER	92	O	CR8	127	O	CD0
23	O	DUV	58	O	CR7	93	O	DET	128	-	Vss
24	I	TSV	59	O	CR6	94	O	KB1	129	-	Vss
25	I	TST5	60	O	TFW	95	O	KB2	130	O	YD9
26	I	SYCK	61	O	KAH	96	I	TST2	131	O	YD8
27	I	TST4	62	I/O	FFW	97	-	Vss	132	-	Vcc
28	I	TST3	63	O	KCK	98	O	YD7			
29	O	DB2	64	-	Vcc	99	O	YD6			
30	O	DB1	65	O	CR5	100	O	YD5			
31	-	--	66	I/O	CT9	101	-	Vss			
32	-	--	67	I/O	CT8	102	-	Vss			
33	-	--	68	I/O	CT7	103	O	YD4			
34	O	ANI	69	O	CR6	104	O	YD3			
35	O	ANO	70	O	CR3	105	-	Vss			

Decoder - Functional Pin Description

1. Input Pin

D19-0 -- Data Input for 10bit parallel interface. DI9 corresponds to MSB and DI0 corresponds to LSB. Defined by a trailing edge of the clock supplied to "DICK" pin. In case of an 8 bit input, "DI9-2" are used.

DICK -- 27MHz clock input for parallel interface.

SYCK -- Sytem side 13.5MHz clock signal input to interchange clock, input the clock signal generated by "PLL" which is locked to the input reference signal. If not necessary to intercahnge the clock, input 13.5MHz clock from "KCK" output (for easy emplanation, the circuit before the FIFO is temporarily referred to "Input side" and the circuit after the FIFO is referred to "system side").

XCOR -- Mode selection for error processing of XY byte in the TRS (Timing Reference Signal).
H: Detection, L: Correction
an internal pull-up resistor is implemented.

FRST -- When low level is input, intilialize the position of RD/WR pointer of FIFO (6 length, ring buffer type) used fro clock interchange. The value of pointer is initialized by keeping input to low level for more than 150ns on condition that both "DICK" pin and "SYCK" pin are accepting clock pulse.

FBPS -- Bypass setting of FIFO used for clock interchange.
H: Bypass off, L: Bypass on.
An internal pull-up resistor is implemented. If not necessary to interchange the clock, it is also possible to operate only with the use of input reference signal by bypassing FIFO and inputting the input side 13.5MHz clock from "KCK" output pin.

WM1,0 -- Mode selection fro rounding of 9th and 10th bit in the 10 bit data of parallel interface.

WM1	WM0	Rounding
0	0	Through
0	1	Truncate
1	0	Round up
1	1	Round to the closest

During V, H blanking and SAV (except EAV), the 9th and 10th bits are always passed through.

CMPX -- Chroma Multiplex output mode setting.
H: MPX on L: MPX off
When MPX is on , Cb and Cr are put togehter and output at 13.5MHz rate from "CO9-0" output pin. When MPX is off, Cb and Cr are individually output at 6.75MHz rate from separate output pins. (Cb: CO9-0, Cr: CR9-0)

VOEN -- Output enable/Disable selection for YO9-0, CO9-0, CR9-0 output pins.
H: Enable L: Disable
All for test input. An internal pull-up resistor is implemented. They are usually open or connected to +5V.

2. Output Pin

YO9-0 -- Y data output after clock interchange. The phase is defined by the system side 13.5MHz clock.

XER -- Output the result of EAV error check on XY byte in the input TRS. Errors are identified by high level. This output will be high in such a case where an error is detected while "XCOR" input is being set to high (error detection mode). On the other hand, it will remain low while "XCOR" input is being set to low (correction mode) except when an error is not corrected.

VL13-10 -- Output the status of the lines on which V pulse is falling in the 1st field of 525 mode.

VL				525-V
13	12	11	10	Falling Line (F1)
0	0	0	0	10
0	0	0	1	11
		I		I
1	0	0	1	19
1	0	1	0	20

VL23-20 --- Output the status of the lines on which V pulse is falling in the 2nd field of 525 mode.

VL				525-V
23	22	21	20	Falling Line (F2)
0	0	0	0	273
0	0	0	1	274
		I		I
1	0	0	1	282
1	0	1	0	283

FRSP -- Output the reset signal (active low) of FIFO used for clock interchange for monitoring purpose. Output the 'or' ED signal between the reset input from "FRST" pin and the reset signal generated inside the IC.

KB1, KB2, KS, OB1, OB2, TU1, TU) -- Monitor pins, these are usually not used.

CO9-0 -- Output the chroma data after clock interchange. When "CMPX" input is set to high, output chroma multiplex data of Cb and Cr (defined by system side 13.5MHz clock). When"CMPX" input is set to low, output Cb only (defined by system side 6.75MHz clock). 3-state output (controlled by "VOEN" pin)

CR9-0 -- Cr data output after clock interchange. 3-state output (contolled by "VOEN" pin)

OUF, OUV, OUH -- Output F, V and H pulses after clock interchange, which are actually the out puts of KF, KV and KH after FIFO. Defined by sustem side 13.5MHz clock. 3-state output (contorlled by "SOEN" pin). If clock signal is not supplied to "DICK" pin while clock is upplied to "SYCK" pin, all these pins will output high level.

AN1,0 -- Output ancillary data start timing after clock interchange. When TT byte in the header (oo, FF, FF, TT, MM, LL) of ancillary data is output from either CO9-2 or YO9-2, "ANI" and "ANO" will be lowered by 1 clock (usually high) for each case. Defined by system side 13.5MHz clock. (Controlled by "SOEN" pin).

CT9-0 -- Output the values of F and H counters. Separate the value of frame-flywheel counter into H part (10 bit) and F part (10 bit) and output both of them with a time sharing method. Only when H counter value is 16, output F counter value.

For example, as H counter is reset by EAV timing, it covers the range of from 0 to 857 in 525 mode and from 0 to 863 in 625 mode. On the other hand, F counter is reset by the trailing edge of F bit in the input, consequently, 0 is put out in the period of F counter value output right after the trailing edge of F bit. The range of F counter is from 0 to 524 mode and from 0 to 624 in 625 mode.

FMX -- When CT9-0 pin is outputting F counter value, output low level and when CT9-0 is outputting H counter value, output high level. Defined by input side 13.5MHz clock.

DET -- TRS (Timing reference signal) detection pulse. When FF, 00, 00 sequence is detected amoung the significant 8 bits in the 10 bit input signal fro DI9-2, output low pulse with 1ck width is defined by input side 27MHz.

FFW -- Frame flywheel status. H: Lock L: Unlock

TFW -- TRS flywheel status. H: Lock L: Unlock

KCK -- Clock signal output defined by input side 13.5MHz which is half the frquency of input signal from "DICK" input (27MHz) and which phase is determined by EAV timing.

CK6 -- system side 6.75MHz clock signal formed from "SYCK" input signal (system side 13.5MHz clock).

LSTD -- Line standard status deteced from the intervals between each TRSs in the input data.
H: 525 L: 625

LOST -- Output H signal when it is judged that "DICK" pin does not accept 27MHz clock. Only applicable to the case where the clock signal is supplied to "SYCK" pin.

KF, KV, KH -- Output F, V, and H pulses before clock interchange, which are extracted from TRS in the input data and have logic conforming to that is defined in the TRS. For example, since H bit is "1" during EAV, and "0" during SAV, KH will be such a pulse as it becomes high level during H blanking.

KAH -- Output pulse with 50% duty which falls at the point equivalent to the leading edge of analog H sync pulse.

Electrical Characteristics

(Absolute Maximum Rating) (Ta=25°C)

Item	Symbol	Maximum Rating	Unit
Power voltage	V_{DD}	-0.5 ~ +7.0	V
Input voltage	V_I	-0.5 ~ +7.0	V
Output voltage	V_O	-0.5 ~ +5.5	V
Storage temperature	T_{STG}	-65 ~ +150	°C

(Recommended Operation Rating)

Item	Symbol	Min.	Max.	Unit
Power voltage	V_{DD}	4.5	5.5	V
High level input voltage	V_{IH}	2.0	V_{DD}	V
Low level input voltage	V_{IL}	0	0.8	V
High level output current	I_{OH}	-1	--	mA
Low level output current	I_{OL}	--	12	mA
Ambient Temperature	T_a	0	85	°C

(DC Characteristic Specification)
(V_{DD} = 5V ± 10%, Ta=0 °C to +85 °C)

Item	Symbol	Condition	Min.	Typ.	Max	Unit
Input clamp voltage	V_{IC}	V_{DD}=4.5V, I_{IL}=-18mA	-1.5	-0.8	--	V
High level output voltage	V_{OH}	V_{DD}=4.5V, I_{OH}=-1mA	+2.5	+3.4	--	V
Low level output voltage	V_{OL}	V_{DD}=4.5V, I_{OL}=24mA	--	+0.3	+0.5	V
High level input current	I_{IH}	V_{DD}=5.5V, V_I=2.7V (Note)	-20	--	+20	µA
Low level input current	I_{IL}	V_{DD}=5.5V, V_I=0.4V (Note)	-20	--	+20	µA
Output short current	I_{OS}	V_{DD}=5.5V, V_O=0V	-100	-40	-25	mA
High impedance output leak	I_{OZ}	V_{DD}=5.5V, V_{OH}=2.7V, V_{OL}=0.4V	-20	--	+20	µA
Input Threshold voltage	V_{TH}		--	+1.4	--	V
Supply current	I_{DD}			+150	+210	mA

Note: Except the inputs on which an internal pull-up resistor is implemented.

Electrical Characteristics

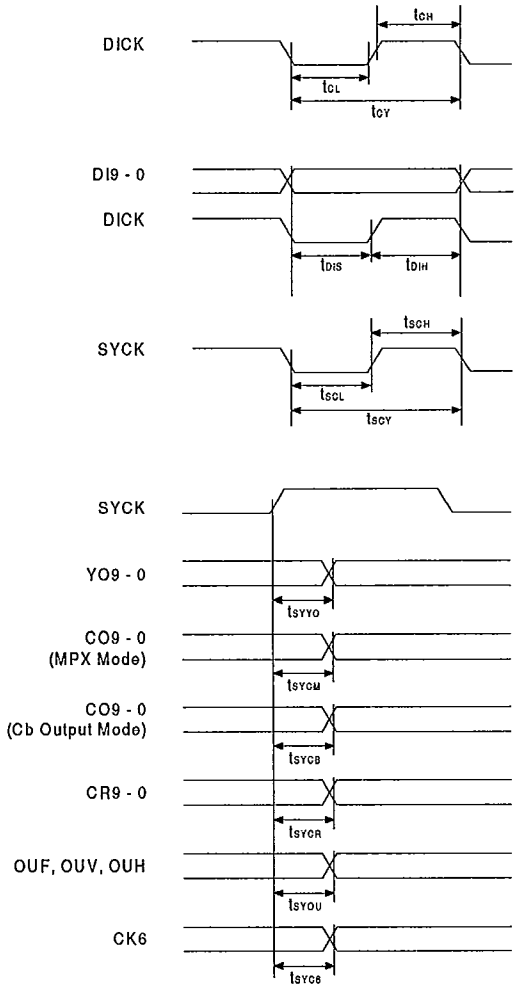
(Input/Output Capacitance Characteristics)

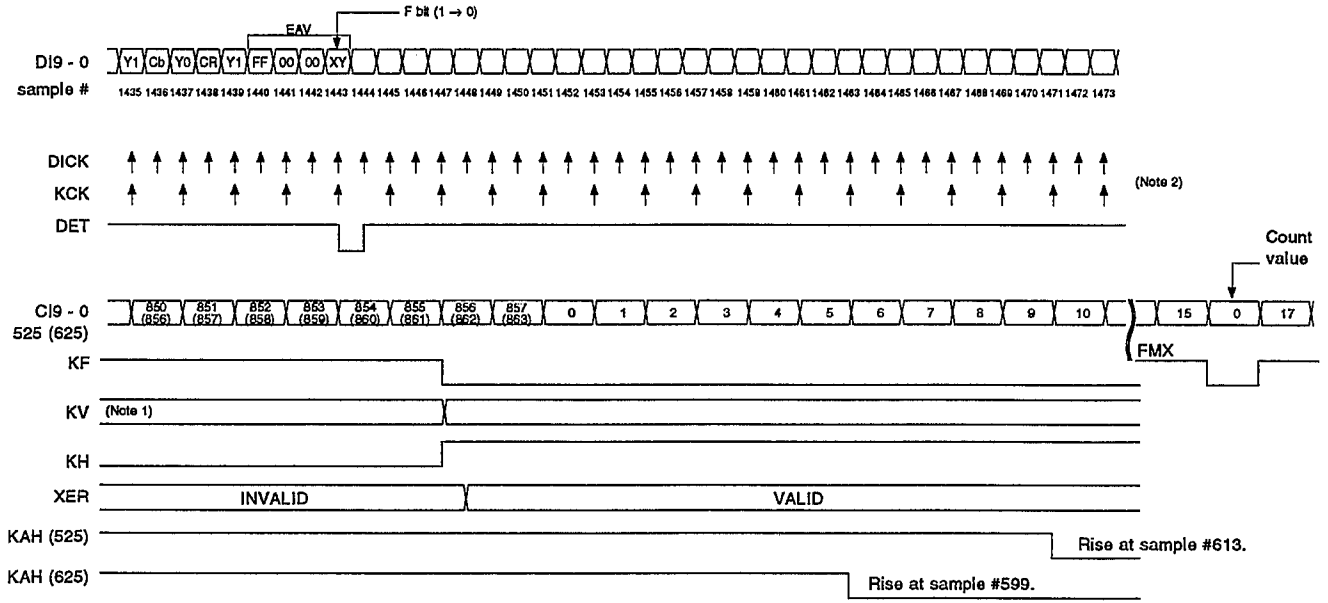
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input terminal	C_{IN}	$V_{DD} = V_I = 0V$			10	pF
Output terminal	C_{OUT}	$f = 1MH$			15	pF
In/output terminal	$C_{I/O}$				20	pF

AC Characteristic

Item	Symbol	Min.	Typ.	Max.	Unit
DICK Cycle Period	TCY	30	37		ns
DICK Low Time	TCL	5	18.5		ns
DICK High Time	TCH	5	18.5		ns
DI9~0 Setup Time	TDIS	2			ns
DI9~0 Hold Time	TDIH	5			ns
SYCK Cycle Period	TSCY	60	74		ns
SYCK Low Time	TSCL	5	37		ns
SYCK High Time	TSCH	5	7		ns
SYCK→ TO9~0 Delay	TSYYO	4		17	ns
SYCK→ CO9~0 Delay (MPX Mode)	TSYCM	5		22	ns
SYCK→ CO9~0 Delay (Cb output mode)	TSYCB	7		28	ns
SYCK→ CR9~0 Delay	TSYCR	5		22	ns
SYCK→ OUF, OUV, OUH Delay	TSYOU	4		17	ns
SYCK→ CK6 Delay	TSYC6	3		13	ns

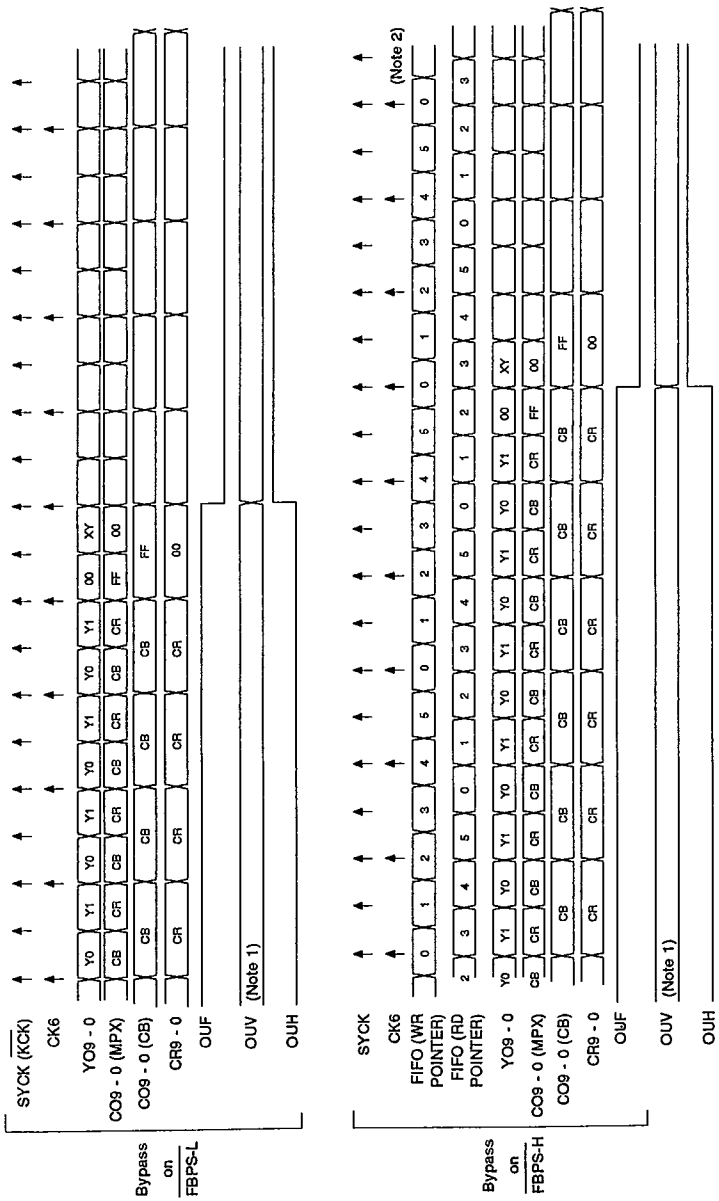
Pin Name


DICK
tCH
tCL
tCY
DI9 - 0
DICK
tDIS
tDIH
SYCK
tSCH
tSCL
tSCY
SYCK
YO9 - 0
tSYYO
CO9 - 0
(MPX Mode)
tSYCM
CO9 - 0
(Cb Output Mode)
tSYCB
CR9 - 0
tSYCR
OUF, OUV, OUH
tSYOU
CK6
tSYC6



NOTES: 1. KV and OUV change on the particular lines.
2. Phase is arbitrary. Pointer values are for example only.

CXD8069G - TIMING VICINITY OF EAV



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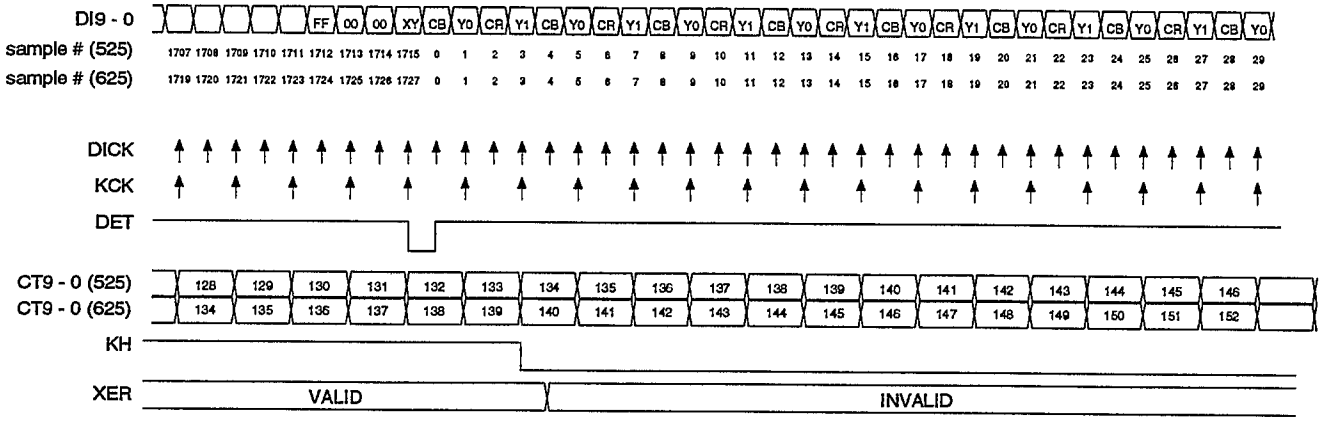
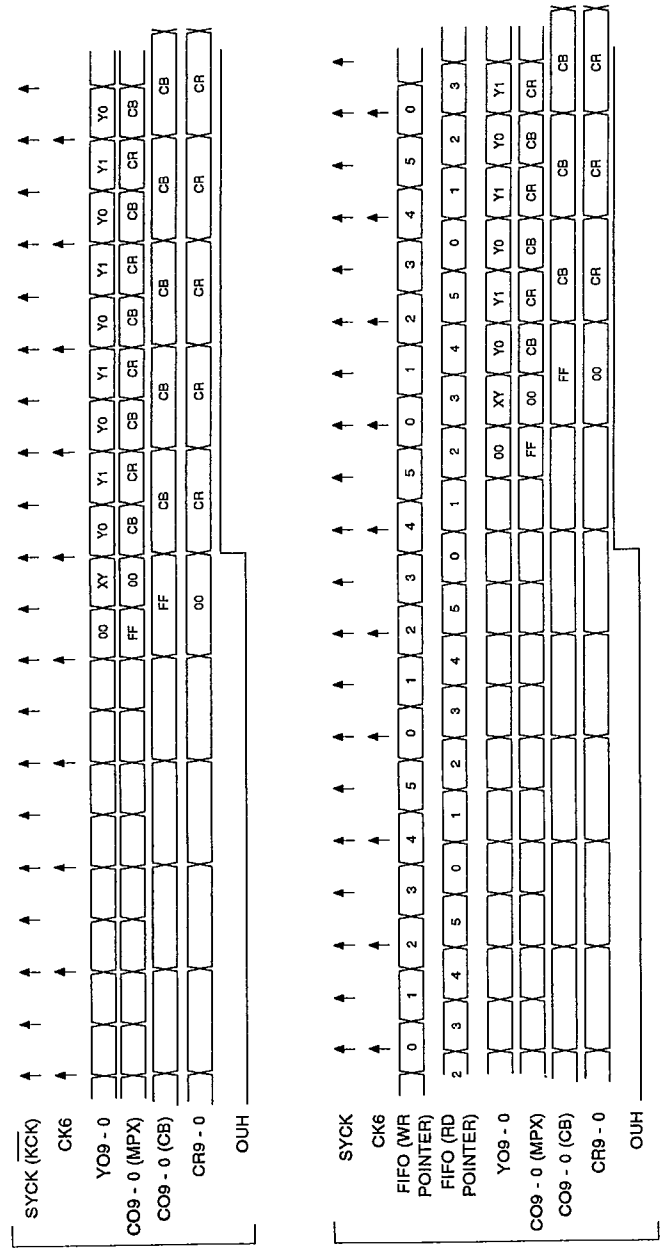
CXD8069G - TIMING VICINITY OF EAV



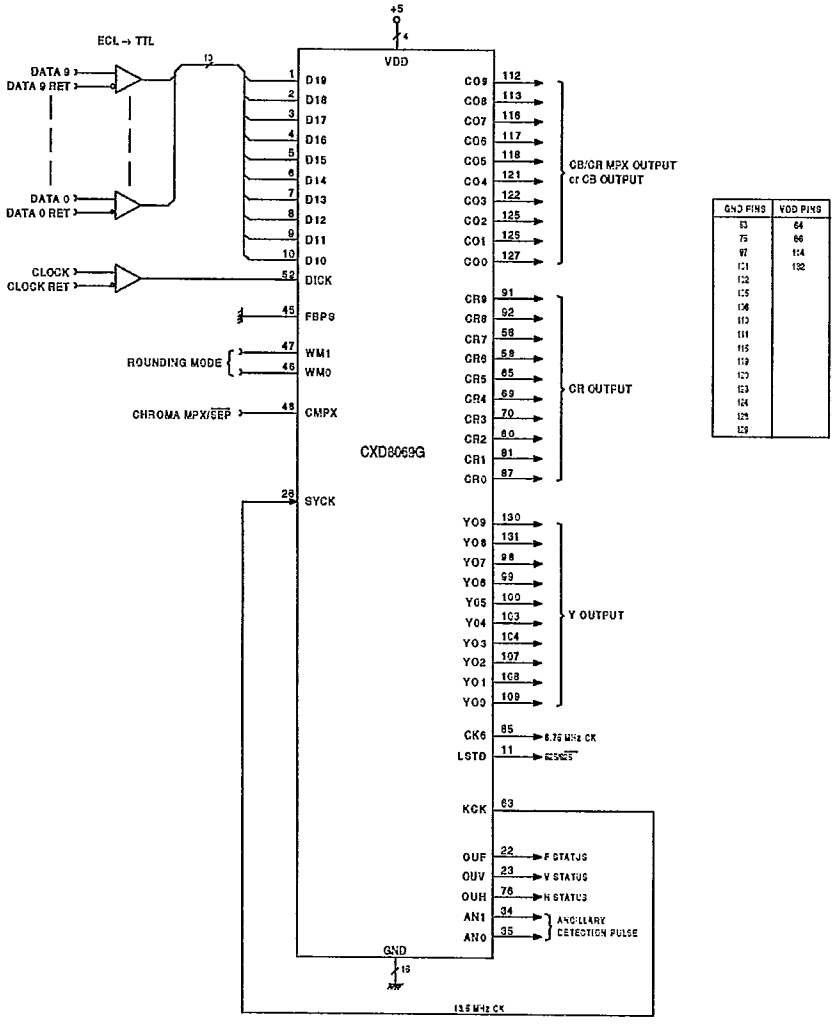
NOTE: Phase is arbitrary. Pointer values are for example only.

CXD8069G - TIMING VICINITY OF SAV

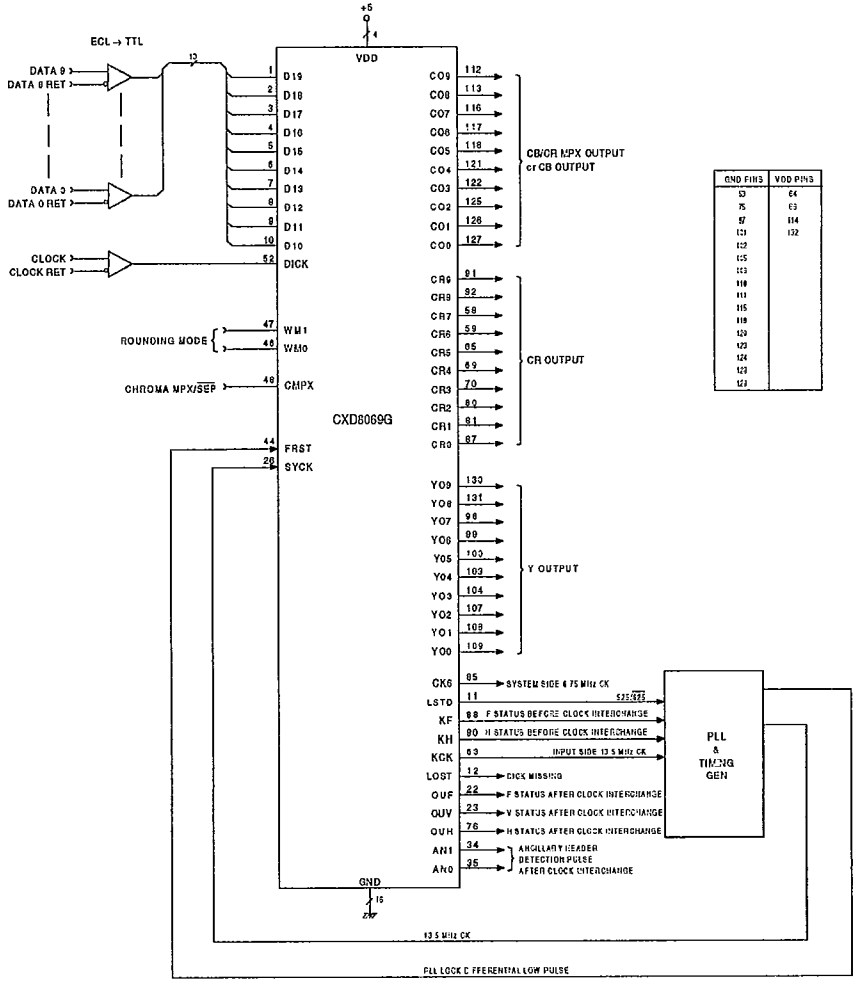


NOTE: Phase is arbitrary. Pointer values are for example only.

CXD8069G - TIMING VICINITY OF SAV



APPLICATION EXAMPLE
(when not using an internal FIFO)



APPLICATION EXAMPLE
(when using an internal FIFO)