

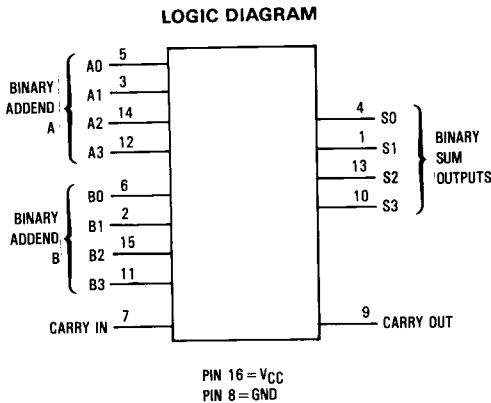
*Product Preview*  
**4-Bit Binary Full Adder with Fast Carry**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC283 is identical in pinout to the LS283. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC283 is a high-speed 4-bit binary Full Adder with internal carry lookahead. The device adds two 4-bit words (A and B) plus the Carry-In bit. The binary sum appears at the Sum outputs (S), and any resulting carries appear at the Carry-Out pin.

Because of the symmetry of the binary add function, the HC283 can be used either with all inputs and outputs active-high (positive logic), or with all inputs and outputs active-low (negative logic). With active-high inputs, Carry In must be held low when no carry-in is intended.

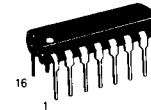
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 212 FETs or 53 Equivalent Gates



**MC54/74HC283**



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



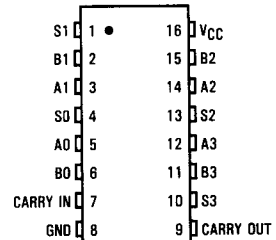
**D SUFFIX**  
**SOIC**  
**CASE 751B-03**

**ORDERING INFORMATION**

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 7.

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Outputs	
A <sub>n</sub>	B <sub>n</sub>	C <sub>In</sub> = C <sub>O</sub> <sub>n-1</sub>	S <sub>n</sub>	C <sub>O</sub> <sub>n</sub> = C <sub>I</sub> <sub>n+1</sub>
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

n=0, 1, 2, 3 (A<sub>3</sub>, B<sub>3</sub>, and S<sub>3</sub> are the most significant bits)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

# MC54/74HC283

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC283

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Projected Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Carry In to Sum Out (Figures 1 and 3)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A or B to Sum Out (Figures 1 and 3)	2.0	270	340	405	ns
		4.5	54	68	81	
		6.0	46	58	69	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Carry In to Carry Out (Figures 2 and 3)	2.0	195	245	295	ns
		4.5	39	49	59	
		6.0	33	42	50	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A or B to Carry Out (Figures 2 and 3)	2.0	225	280	340	ns
		4.5	45	56	68	
		6.0	38	48	58	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		130	

## SWITCHING WAVEFORMS

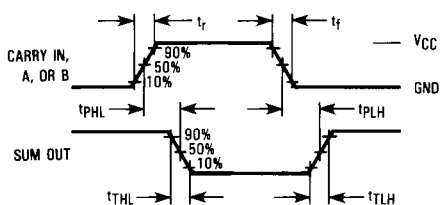


Figure 1

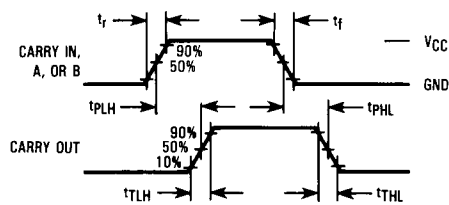
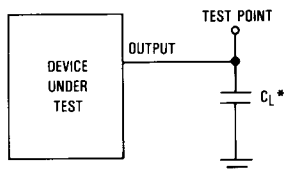


Figure 2



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

