

TDA2577A Sync Circuit With Vertical Oscillator and Driver

Product Specification

Linear Products

DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

FEATURES

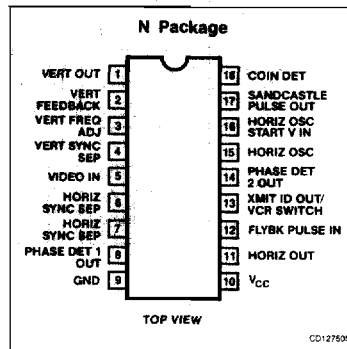
- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise-only conditions
- Time constant externally switchable (e.g., fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector (φ_2) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3 levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the supply voltage

- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6.5V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with precorrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

APPLICATIONS

- Video monitors
- TV receivers
- Video processing

PIN CONFIGURATION



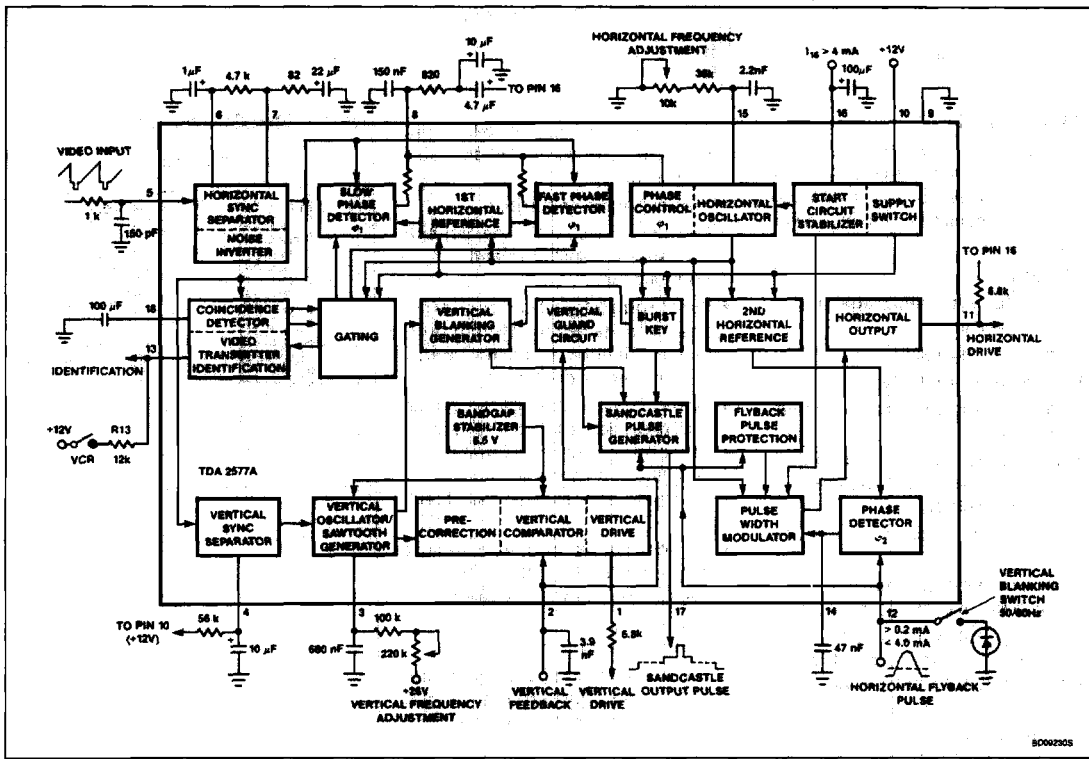
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	-25°C to +65°C	TDA2577AN

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

BLOCK DIAGRAM



Sync Circuit With Vertical Oscillator and Driver

TDA2577A

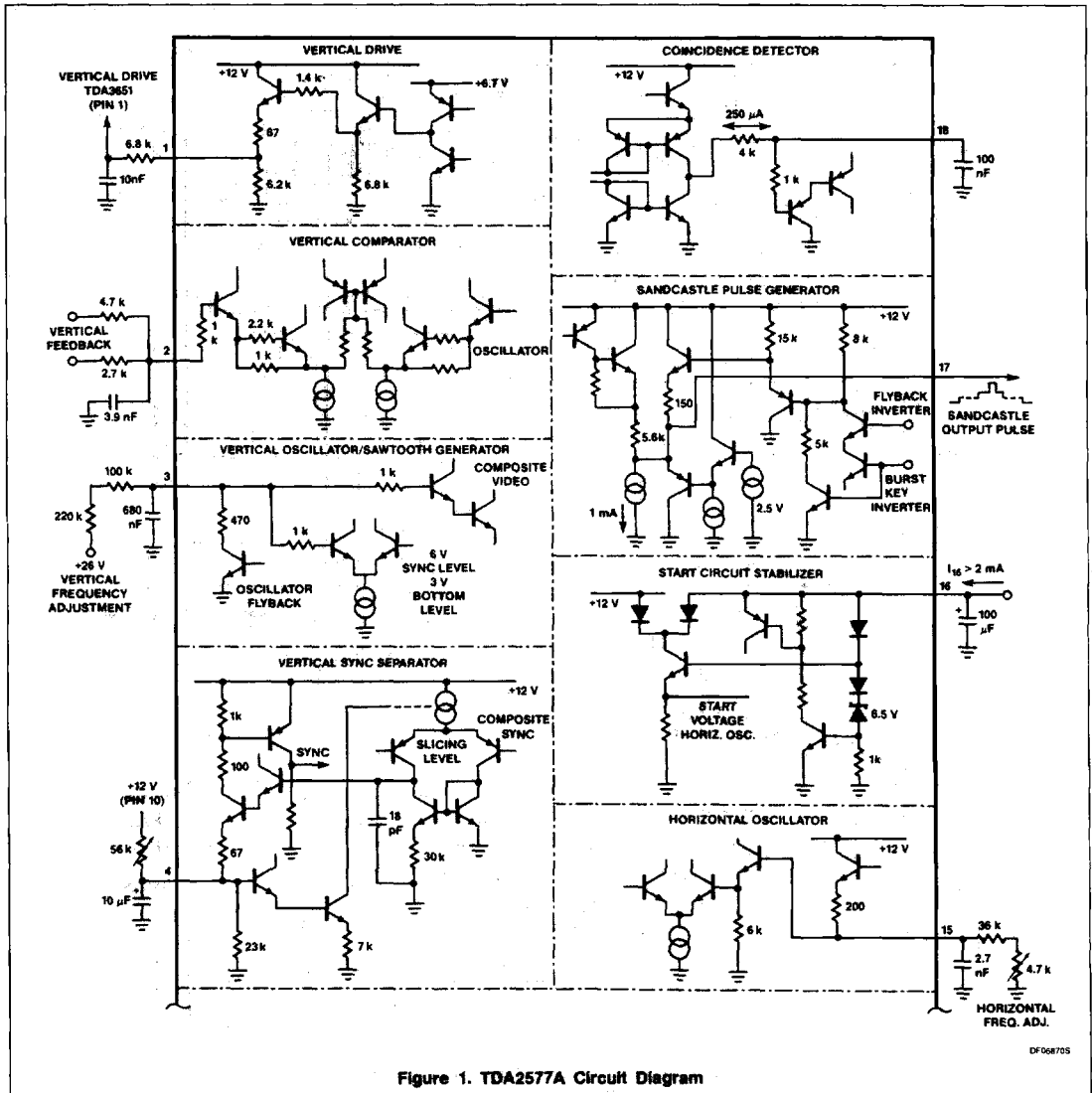


Figure 1. TDA2577A Circuit Diagram

DF068705

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

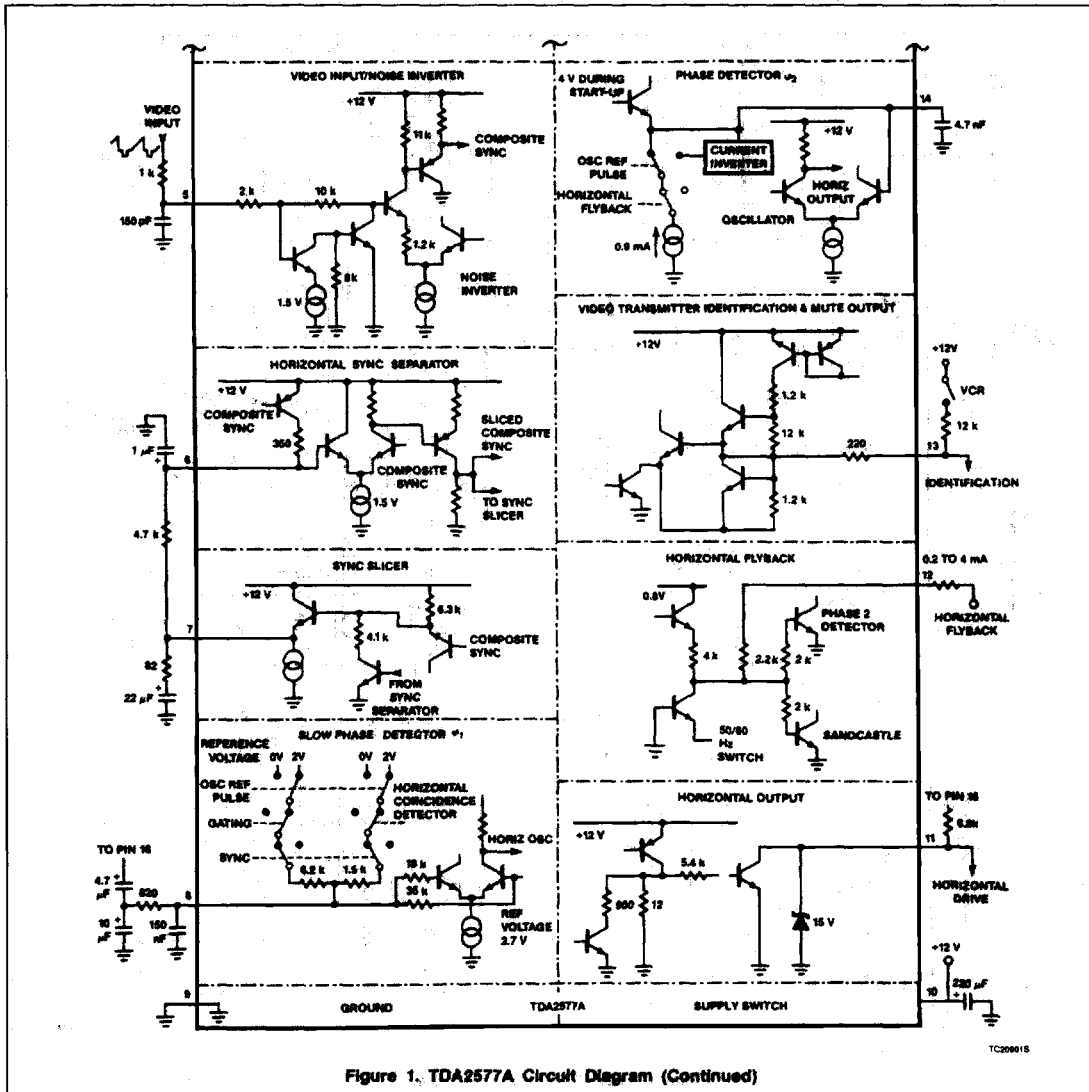


Figure 1. TDA2577A Circuit Diagram (Continued)

TC00015

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
I_{16}	Start current (Pin 16)	8	mA
$V_{CC} = V_{10-9}$	Supply voltage (Pin 10)	13.2	V
P_{TOT}	Total power dissipation	1.1	W
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient in free air	50	°C/W

DC ELECTRICAL CHARACTERISTICS $I_{16} = 5\text{mA}$; $V_{CC} = 12\text{V}$; $T_A = 25^\circ\text{C}$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
I_{16}	Supply current at Pin 16	4		8	mA
V_{16-9}	Stabilized supply voltage (Pin 16)	8.0	8.7	9.5	V
I_{10}	Supply current (Pin 10)		55	70	mA
$V_{CC} = V_{10-9}$	Supply voltage (Pin 10)	10	12	13.2	V
Video input (Pin 5)					
V_{5-9}	Top-sync level	1.5	3.1	3.75	V
$V_{5-9(P-P)}$	Sync pulse amplitude (peak-to-peak value) ¹	0.15	0.6	1	V
	Slicing level	35	50	65	%
t_1	Delay between video input and detector output		0.35		μs
Noise gate (Pin 5)					
V_{5-9}	Switching level		0.7	1	V
First control loop (sync to oscillator; Pin 8)					
Δf	Holding range		± 800		Hz
Δf	Catching range	± 600	800	1100	Hz
	Control sensitivity video with respect to oscillator, burst key, and flyback pulse for slow time constant for fast time constant		1 275		kHz/ μs kHz/ μs
Second control loop (horizontal output to flyback; Pin 14)					
$\Delta t_D/\Delta t_O$	Control sensitivity; static ²		400		$\mu\text{s}/\mu\text{s}$
t_D	Control range	1		50	μs
	Controlled edge		negative		
Phase adjustment (via 2nd control loop; Pin 14)					
	Control sensitivity		25		$\mu\text{A}/\mu\text{s}$
$\pm I_{14}$	Maximum permissible control current		0	50	μA
Horizontal oscillator (Pin 15)					
f_{OSC}	Frequency (no sync)		15625		Hz
Δf_{OSC}	Frequency spread ($C_{OSC} = 2.2\text{nF}$; $R_{OSC} = 40\text{k}\Omega$)			4	%
Δf_{OSC}	Frequency deviation between starting point of output signal and stabilized condition		6	8	%
T_C	Temperature coefficient		1×10^{-4}		°C

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

DC ELECTRICAL CHARACTERISTICS (Continued) $I_{16} = 5\text{mA}$; $V_{CC} = 12\text{V}$; $T_A = 25^\circ\text{C}$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal output (Pin 11)					
V_{11-9}	Output voltage; high level			13.2	V
V_{11-9}	Voltage at which protection starts	13		15.8	V
V_{11-9}	Output voltage; low level start condition at $I_{11} = 10\text{mA}$		0.3	0.5	V
V_{11-9}	normal condition at $I_{11} = 40\text{mA}$		0.3	0.5	V
δ	Duty factor of output signal during starting (no phase shift; voltage at Pin 11 Low)		65		%
δ	Duty factor of output signal without flyback pulse	45	50	55	%
	Controlled edge	negative			
	Duration of output pulse (see Figure 2)	$t_p + t_o + 2.5$			μs
Sandcastle output pulse (Pin 17)					
V_{17-9}	Output voltage during: burst key horizontal blanking vertical blanking	10			V
V_{17-9}		4.2	4.6	5	V
V_{17-9}		2	2.5	3	V
t_p	Pulse duration burst key horizontal blanking vertical blanking for 50Hz application ($-I_{12} : 0$ to 0.1mA) for 60Hz application ($-I_{12} : \text{typ. } 0.2\text{mA}$)	3.6	4	4.4	μs
		flyback pulse ³			
				21 17	lines lines
t_2	Delay between the start of the sync at the video input and the rising edge of the burst key pulse	4.8	5.2	5.6	μs
Coincidence detector; video transmitter identification circuit; time constant switches (Pin 18); see also Figure 1					
$\pm I_{18}$	Detector output current		300		μA
V_{18-9}	Voltage during noise ⁴		0.3		V
V_{18-9}	Voltage level for in-sync condition		7.5		V
V_{18-9}	Switching level slow-to-fast	3.2	3.5	3.8	V
V_{18-9}	Switching level mute function active; φ_1 fast-to-slow vertical period counter 3 periods fast	1.0	1.2	1.4	V
V_{18-9}		0.08	0.12	0.16	V
V_{18-9}	Switching level slow-to-fast (locking) mute function inactive	1.5	1.7	1.9	V
V_{18-9}	Switching level fast-to-slow (locking)	4.7	5.0	5.3	V
V_{18-9}	Switching level for VCR (fast time constant) without mute function	8.2	8.6	9	V

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

DC ELECTRICAL CHARACTERISTICS (Continued) $I_{16} = 5\text{mA}$; $V_{CC} = 12\text{V}$; $T_A = 25^\circ\text{C}$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Video transmitter identification output (Pin 13)					
V_{13-9}	Output voltage active (no sync) at $I_{13} = 1\text{mA}$	10	11		V
V_{13-9}	Output voltage active (no sync) at $I_{13} = 5\text{mA}$	7	10		V
V_{13-9}	Output voltage inactive		0.1	0.5	V
VCR switching (Pin 13)					
I_{13}	Input current for fast time constant phase detector φ_1 , with mute function active	0.4	0.6	0.8	mA
Flyback input pulse (Pin 12)					
V_{12-9}	Switching level		1		V
I_{12}	Input current	0.2		4	mA
$V_{12-9(P-P)}$	Input pulse amplitude (peak-to-peak value)			12	V
R_{12-9}	Input resistance		2.7		k Ω
t_0	Delay time of sync pulse (measured in φ_1) to flyback at switching level; $t_{FL} = 12\mu\text{s}^2$ (see also Figure 3)		1.3		μs
Duration of vertical blanking pulse (Pin 12)					
$-I_{12}$	Required input current (negative) for 50Hz application; 21 lines blanking for 60Hz application; 17 lines blanking	0.15	0.2	0.3	mA
$-I_{12}$				0.1	mA
$-I_{12}$	Maximum allowed input current			0.4	mA
Vertical sawtooth generator (Pin 3)					
f_S	Vertical frequency (no sync)		46		Hz
Δf_S	Frequency spread ($C_{OSC} = 680\text{nF}$; $R_{OSC} = 180\text{k}\Omega$; at +26V)			4	%
	Synchronization range		22		%
I_3	Input current at $V_{3-9} = 6\text{V}$			2	μA
Δf_S	Frequency shift for $V_{CC} = 10$ to 13V			0.2	%
T_C	Temperature coefficient		1×10^{-4}		$^\circ\text{C}^{-1}$
Comparator (Pin 2)					
V_{2-9}	Input voltage DC level AC level (peak-to-peak value)	4.0	4.4	4.8	V
$V_{2-9(P-P)}$					1.6
I_2	Input current at $V_{2-9} = 6\text{V}$			2	μA
	Sawtooth internal pre-correction (parabolic convex)		3		%
Vertical output stage; emitter-follower (Pin 1)					
V_{1-9}	Output voltage at $I_1 = 10\text{mA}$	3.2	3.6	5	V
I_1	Output current			20	mA
Vertical guard circuit					
V_{2-9}	Activating voltage levels (vertical blanking level is 2.5V) switching level Low switching level High	2.7	3	3.3	V
V_{2-9}		5.4	5.8	6.3	V

NOTES:

- Up to $1V_{p,p}$ the slicing level is constant; at amplitudes exceeding $1V_{p,p}$, the slicing level will increase.
- t_0 = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
 t_0 = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (Pin 8).
- The duration of the flyback pulse is measured at the input switching level, which is about $1V(t_{FL})$.
- Depends on DC level at Pin 5; value given applicable for $V_{5-9} \approx 5\text{V}$.

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geq 4mA$), which can be taken directly from the supply line. Therefore, it is possible to derive the main supply (Pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting up, the second phase detector (ψ_2) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6.5V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between Pins 6 and 7 determines its value. A 4.7k Ω resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3.1V. The amplitude selective noise inverter is activated at a level of 0.7V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared to a

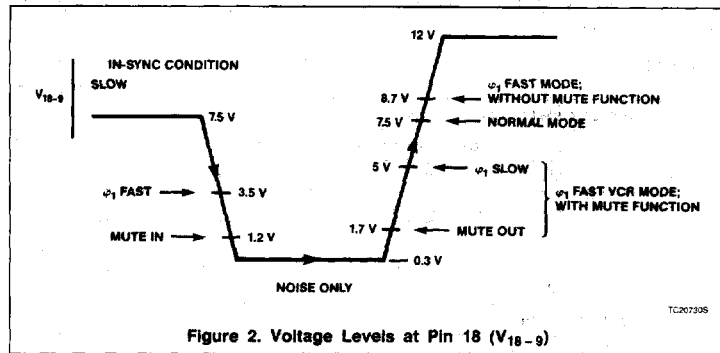


Figure 2. Voltage Levels at Pin 18 (V_{18-9})

waveform with its rising edge referring to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared to another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore, the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched

off during catching. Also, the output current of the phase detector is increased fivefold during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync, or no-video condition is detected by the video transmitter identification/coincidence detector circuit (Pin 18). The voltage on Pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Figure 2. The complete survey of the switching actions is given in Table 1.

Table 1. Switching Levels at Pin 18

VOLTAGE AT PIN 18	FIRST PHASE DETECTOR ψ_1		MUTE OUTPUT AT PIN 13		RECEIVING CONDITIONS			
	Time Constant		Gating				On	Off
	Slow	Fast	On	Off				
7.5V	X		X		X	Video signal detected		
7.5 to 3.5V	X		X		X	Video signal detected		
3.5 to 1.2V		X		X	X	Video signal detected		
1.2 to 0.1V	X		X	*	X	Noise only		
0.1 to 1.7V	X	*	X	*	X	New video signal detected		
1.7 to 5.0V		X		X		Horizontal oscillator locked		
5.0 to 7.5V	X		X		X	VCR playback with mute function		
8.7V	X	X	X	X	X	Horizontal oscillator locked VCR playback without mute function		

Where: * = 3 vertical periods.

The stability of displayed video information (e.g., channel number) during noise-only conditions is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on Pin 5 during noise-only conditions should not exceed 5.5V. Otherwise, the time constant switch may be set to fast due to the average voltage level on Pin 18 dropping below 0.1V. When the voltage on Pin 18 drops below 100mV, a counter is activated which sets the time constant switch to fast,

and not gated for 3 vertical periods. This condition occurs when a new video signal is present at Pin 5. When the horizontal oscillator is locked, the voltage on Pin 18 increases. Nominally, a level of 5V is reached within 15ms (1 vertical period). The mute switching level of 1.2V is reached within 5ms ($C_{18} = 47nF$). If the video transmitter identification circuit is required to operate under VCR playback conditions, the first phase detector can be set to fast by connecting a resistor of 180k Ω between Pin 18 and

ground. Also, a current of 0.6mA into Pin 13 sets the first phase detector to fast without affecting the mute output function (active High with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1k Ω to the supply (Pin 10).

The supply for the horizontal oscillator (Pin 15) and horizontal output stage (Pin 11) is derived from the voltage at Pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into Pin 16

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

of 3.5mA, which will result in a supply voltage of about 5.5V (for guaranteed operation of all devices $I_{16} > 4\text{mA}$). It is possible that the main supply voltage at Pin 10 is 0V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at Pin 10. At 5.5V, all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at Pin 14 is clamped by means of an internally-loaded NPN emitter-follower. This ensures that the duty factor of the horizontal output signal (Pin 11) remains at about 65%. The second phase detector will close if the supply voltage at Pin 10 reaches 8.8V. At this value, the supply current for the horizontal oscillator and output stage is delivered by Pin 10, which also causes the voltage at Pin 16 to change to a stabilized 8.7V. This change switches off the NPN emitter-follower at Pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at Pin 16, and the duty factor of the output signal at Pin 12 is at the value required by the delay at the horizontal deflection stage. Thus, switch-off delays in the horizontal output

stage are compensated. When no horizontal flyback signal is detected, the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47nF capacitor connected to Pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to Pin 2) via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at Pin 1. For a linear sawtooth in the oscillator, the load resistor at Pin 3 should be connected to a voltage source of 26V or higher. The sawtooth amplitude is not influenced by the main supply at Pin 10. The feedback signal is applied to Pin 2 and compared to the sawtooth signal at Pin 3. For an economical feedback circuit with less picture bounce, the sawtooth signal is internally precorrected by 3% (convex) referred to Pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at Pin 3 and the feedback signal at Pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at Pin 13.

To minimize the influence of the horizontal part on the vertical part, a 6.5V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at Pin 17, has three different voltage levels. The highest level (11V) can be used for burst gating and black level clamping. The second level (4.6V) is obtained from the horizontal flyback pulse at Pin 12 and used for horizontal blanking. The third level (2.5V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50Hz, the blanking pulse duration is 21 lines and for 60Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at Pin 12.

The IC also incorporates a vertical guard circuit which monitors the vertical feedback signal at Pin 2. If this level is below 3V or higher than 5.8V, the guard circuit will insert a continuous level of 2.5V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

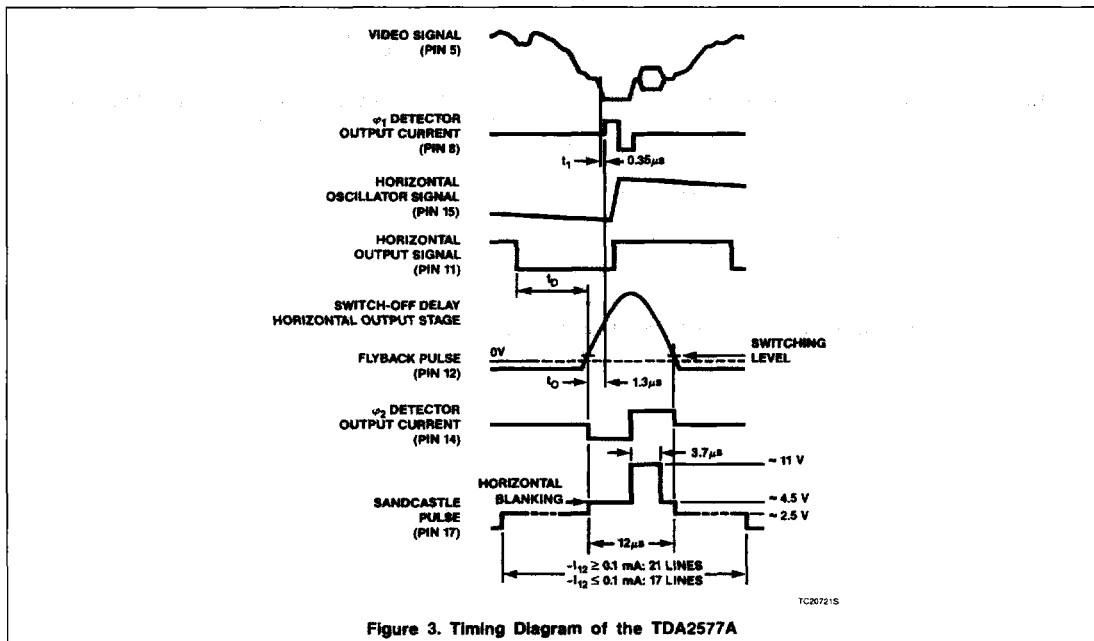


Figure 3. Timing Diagram of the TDA2577A

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

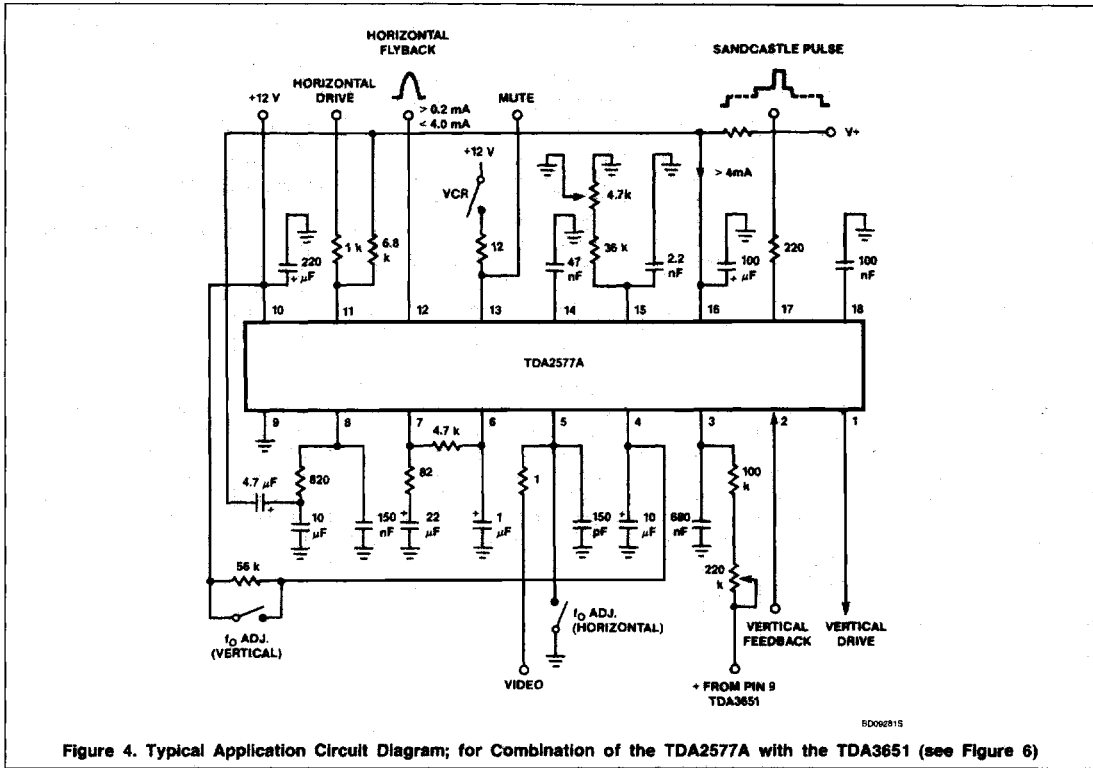


Figure 4. Typical Application Circuit Diagram; for Combination of the TDA2577A with the TDA3651 (see Figure 6)

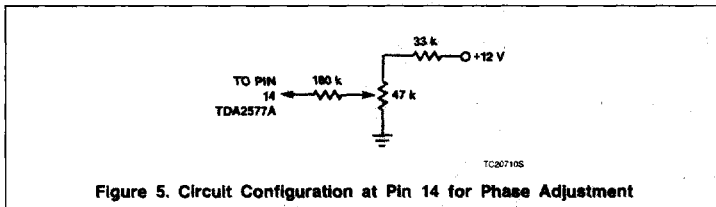


Figure 5. Circuit Configuration at Pin 14 for Phase Adjustment

Sync Circuit With Vertical Oscillator and Driver

TDA2577A

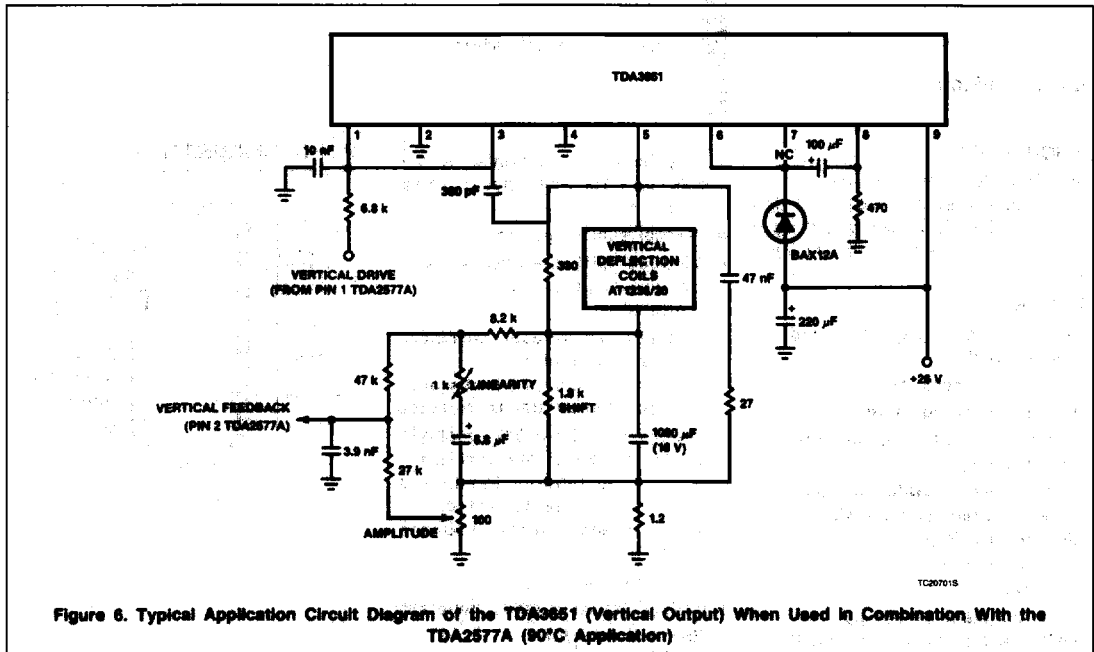


Figure 6. Typical Application Circuit Diagram of the TDA3651 (Vertical Output) When Used in Combination With the TDA2577A (90°C Application)