

MICRON
TECHNOLOGY, INC.
MT8D88C25632
256K x 32, 512K x 16 IC DRAM CARD

T-46-23-18

IC DRAM CARD

1 MEGABYTE

256K x 32, 512K x 16

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{\text{RAS}}$ inputs
- Multiple $\overline{\text{RAS}}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{\text{RAS}}$ -ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V $\pm 5\%$ power supply
- Low power; 8mW standby, 1.8W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS

- Timing
 - 60ns access
 - 70ns access
 - 80ns access

MARKING

-6
-7
-8

GENERAL DESCRIPTION

The MT8D88C25632 is a 1 megabyte, IC DRAM card organized as a 256K x 32 bit memory array. It may also be configured as a 512K x 16 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{\text{CAS}}$ inputs allow byte accesses.

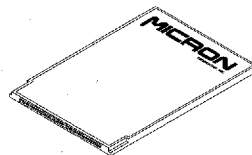
All inputs to the DRAMs are buffered, with the exception of $\overline{\text{RAS}}$. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT8D88C25632 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{\text{RAS}}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{\text{RAS}}$ selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View)

88-Pin Card (U-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	31	NC	61	NC
2	DQ0	32	NC	62	NC
3	DQ1	33	NC	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	CAS2
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	CAS3
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	WE
11	NC	41	DQ14	71	PD1 (Vss)
12	NC	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	NC
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	RAS0	52	DQ24	82	DQ29
23	CAS0	53	DQ25	83	DQ30
24	CAS1	54	NC	84	DQ31
25	NC	55	OE (Vss)	85	DQ32
26	RAS2	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT8D88C25632 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT8D88C25632 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

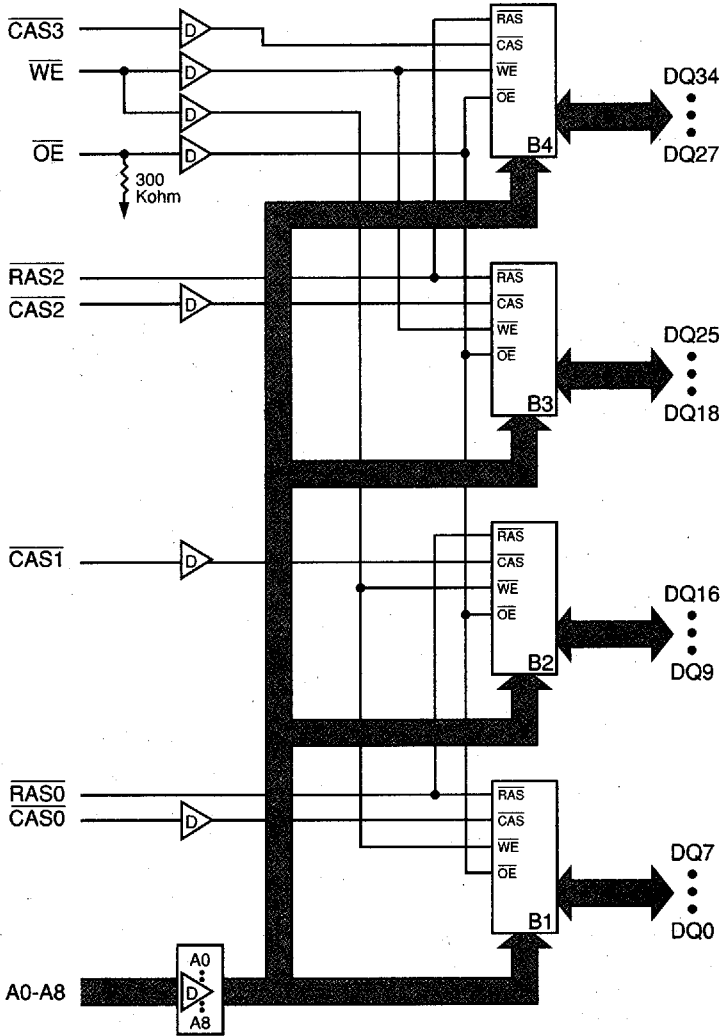
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FUNCTIONAL BLOCK DIAGRAM

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- NOTE:**
1. D = 74AC11244 line drivers.
 2. B1 through B4 = 256K x 8 memory blocks.
 3. \overline{OE} is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.

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PIN DESCRIPTIONS

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PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	RAS0, RAS2	Input	Row Address Strobe: \overline{RAS} is used to clock-in the 9 row-address bits. Two \overline{RAS} inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	\overline{CAS} 0-3	Input	Column Address Strobe: \overline{CAS} is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four \overline{CAS} inputs allow byte access control for any memory bank configuration.
70	\overline{WE}	Input	Write Enable: \overline{WE} is the READ/WRITE control for the DQ pins. If \overline{WE} is LOW prior to \overline{CAS} going LOW, the access is an EARLY-WRITE cycle. If \overline{WE} is HIGH while \overline{CAS} is LOW, the access is a READ cycle, provided \overline{OE} is also LOW. If \overline{WE} goes LOW after \overline{CAS} goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	\overline{OE}	Input	Output Enable: \overline{OE} is the input/output control for the DQ pins. \overline{OE} is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by \overline{RAS} and \overline{CAS} .
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITES may be performed by using the corresponding \overline{CAS} select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 61, 62, 64, 65, 69, 77, 78, 79	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V \pm 5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

The MT8D88C25632 is a 1 megabyte memory card structured as a 256K x 32 bit memory array ($\overline{RAS0} = \overline{RAS2}$). It also may be configured as a 512K x 16 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both \overline{RAS} lines.

Most x32 bit applications use the same signal to control the \overline{CAS} inputs. $\overline{RAS0}$ controls the lower 16 bits, and $\overline{RAS2}$ controls the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding \overline{CAS} pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each \overline{RAS} is then a bank select for the 512K x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle [READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of \overline{RAS} addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. \overline{RAS} is used to latch the first 9 bits and \overline{CAS} the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{CAS} . WE must fall prior to \overline{CAS} (EARLY WRITE); if WE goes LOW after \overline{CAS} , the outputs (Q) will be activated

and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation. Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of \overline{RAS} inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 through 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT8D88C25632 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, eight thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT8D88C25632 operates reliably up to 55°C.

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MEMORY TRUTH TABLE

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FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA IN/OUT
						t _R	t _C	DQ0-DQ34
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L (NC)	ROW	COL	Data Out
	2nd Cycle	L	H→L	H	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L (NC)	ROW	COL	Data Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	H	X	X	X	High-Z
BATTERY BACKUP REFRESH		H→L	L	H	X	X	X	High-Z

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PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS						PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC	X	X	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	X
2MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	NC	X	X	X
4MB	512K x 8, 9	19	10	9	512	NC	Vss	Vss	Vss	Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	X	X	X
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	X	X
8MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	NC	X	X	X
16MB	2 Meg x 8, 9	21	11	10	1,024	NC	NC	Vss	Vss	Vss	X	X	X
16MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	NC	X	X	X
32MB	4 Meg x 1, 4, 16, 18	22	12	11	1,024	Vss	Vss	NC	Vss	Vss	X	X	X
Access Timing	100ns					X	X	X	X	X	Vss	Vss	X
	80ns					X	X	X	X	X	NC	Vss	X
	70ns					X	X	X	X	X	Vss	NC	X
	60ns					X	X	X	X	X	NC	NC	X
	50ns					X	X	X	X	X	Vss	Vss	X
Refresh Control	Standard					X	X	X	X	X	X	X	NC
	Auto					X	X	X	X	X	X	X	Vss

NOTE: Vss = Ground.



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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -0.5V to +5.25V
 Operating Temperature, T_A (Ambient) 0°C to +55°C
 Storage Temperature -20°C to +80°C
 Power Dissipation 15W
 Short Circuit Output Current 50mA
 Card Insertions (Connector's Life Cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = 5V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs	V _{IH}	3.5	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input (0V ≤ V _{IN} ≤ 5.25V; all other pins not under test = 0V)	Non-buffered	I _{IN}	-12	12	μA
	Buffered	I _{IB}	-2	2	μA
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.25V)	I _{OZ}	-10	10	μA	
OUTPUT LEVELS	V _{OH}	2.4		V	
	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) (RAS = CAS = V _{IH})	I _{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc - 0.2V)	I _{CC2}	1.6	1.6	1.6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹ RC = ¹ RC (MIN))	I _{CC3}	680	600	520	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _{IL} , CAS, Address Cycling: ¹ PC = ¹ PC (MIN))	I _{CC4}	520	440	360	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = V _{IH} ; ¹ RC = ¹ RC (MIN))	I _{CC5}	680	600	520	mA	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ¹ RC = ¹ RC (MIN))	I _{CC6}	680	600	520	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = ¹ RAS (MIN) up to 300ns; ¹ RC = 125μs; WE, A0-A8 and DQ = Vcc - 0.2V or 0.2V (DQ may be left open)	I _{CC7}	1.6	1.6	1.6	mA	3, 5


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CAPACITANCE
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PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CAS0, CAS1, CAS2, CAS3, A0-A8, OE	C11		9	pF	2
Input Capacitance: WE	C12		13	pF	2
Input Capacitance: RAS0, RAS2	C13		50	pF	2
Input/Output Capacitance: DQ	C10		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; V_{CC} = 5V ±5%)

AC CHARACTERISTICS PARAMETER	SYM	-6		-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	^t RC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	23
Access time from RAS	^t RAC		60		70		80	ns	14, 23
Access time from CAS	^t CAC		25		30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	^t RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	^t RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	^t RSH	25		30		30		ns	26
RAS precharge time	^t RP	40		50		60		ns	23
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55		65		75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	^t RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15		ns	26
Row address setup time	^t ASR	10		10		10		ns	26
Row address hold time	^t RAH	5		5		5		ns	25
RAS to column address delay time	^t RAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	^t ASC	5		5		5		ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	^t RCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5		5		ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	^t WCS	5		5		5		ns	24

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 5\%$)

AC CHARACTERISTICS		-6		-7		-8		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Write command hold time	t_{WCH}	15		20		20		ns	24
Write command hold time (referenced to $\overline{\text{RAS}}$)	t_{WCR}	40		50		55		ns	25
Write command pulse width	t_{WP}	10		15		15		ns	23
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	25		30		30		ns	26
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	20		25		25		ns	24
Data-in setup time	t_{DS}	5		5		5		ns	24, 32
Data-in hold time	t_{DH}	5		10		10		ns	25, 32
Data-in hold time (referenced to $\overline{\text{RAS}}$)	t_{DHR}	45		55		60		ns	23
Transition time (rise or fall)	t_T	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	t_{REF}		128		128		128	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	10		10		10		ns	26
$\overline{\text{CAS}}$ setup time ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh)	t_{CSR}	20		20		20		ns	5, 26
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh)	t_{CHR}	10		10		10		ns	5, 25
$\overline{\text{WE}}$ hold time ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh)	t_{WRH}	5		5		5		ns	22, 25
$\overline{\text{WE}}$ setup time ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh)	t_{WRP}	20		20		20		ns	22, 26
$\overline{\text{WE}}$ hold time (WCBR test cycle)	t_{WTH}	5		5		5		ns	22, 25
$\overline{\text{WE}}$ setup time	t_{WTS}	20		20		20		ns	22, 26
READ-WRITE cycle time	t_{RWC}	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	90		95		100		ns	23
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	80		90		100		ns	31, 27
Column Address to $\overline{\text{WE}}$ delay time	t_{AWD}	65		70		75		ns	31, 24
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	50		65		55		ns	31, 24
Output buffer turn-off delay	t_{OE}		25		30		30	ns	20, 33, 26
Output disable	t_{OD}		25		30		30	ns	35, 26
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle	t_{OEH}	5		10		10		ns	34, 27
$\overline{\text{OE}}$ hold time from $\overline{\text{RAS}}$ during HIDDEN REFRESH cycle	t_{ORD}	10		10		10		ns	21, 26

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NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, $f = 1$ MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100 μ s is required after power-up followed by eight \overline{RAS} refresh cycles (\overline{RAS} -ONLY or CBR with \overline{WE} HIGH) before proper device operation is assured. The eight \overline{RAS} cycle wake-up should be repeated any time the \overline{REF} refresh requirement is exceeded.
8. AC characteristics assume $t_T = 5$ ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100 pF.
14. Assumes that $t_{RCD} < t_{RCD} (MAX)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} \geq t_{RCD} (MAX)$.
16. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, \overline{CAS} must be pulsed HIGH for t_{CPN} .
17. Operation within the $t_{RCD} (MAX)$ limit ensures that $t_{RAC} (MAX)$ can be met. $t_{RCD} (MAX)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (MAX)$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{RAD} (MAX)$ limit ensures that $t_{RCD} (MAX)$ can be met. $t_{RAD} (MAX)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} (MAX)$ limit, then access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. $t_{OFF} (MAX)$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
22. t_{WTS} and t_{WTH} are setup and hold specifications for the \overline{WE} pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of t_{WRP} and t_{WRH} in the CBR refresh cycle.
23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
30. The maximum current ratings are based with the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one half when used in the x16 mode.
31. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS} (MIN)$, the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD} (MIN)$, $t_{AWD} \geq t_{AWD} (MIN)$ and $t_{CWD} \geq t_{CWD} (MIN)$, the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. \overline{OE} held HIGH and \overline{WE} taken LOW after \overline{CAS} goes LOW results in a LATE-WRITE (\overline{OE} controlled) cycle.

NEW
IC DRAM CARD

MICRON
TECHNOLOGY INC**MT8D88C25632**
256K x 32, 512K x 16 IC DRAM CARD**T-46-23-18****NOTES (continued)**

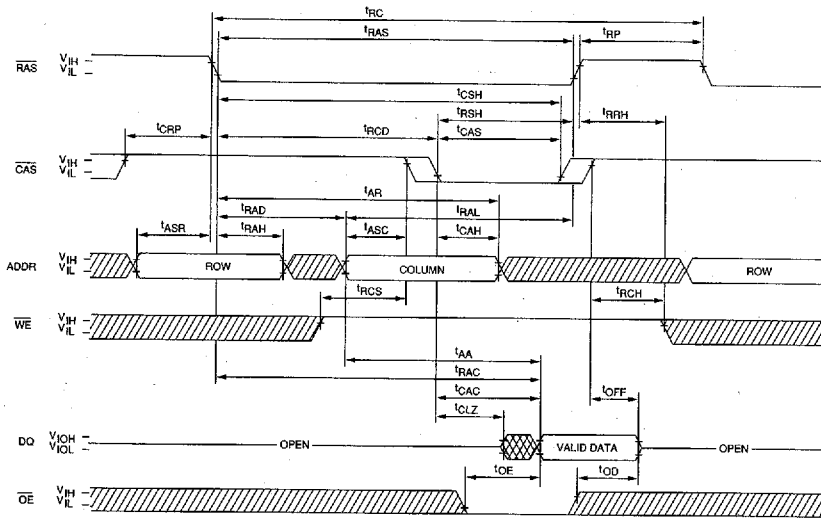
32. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
33. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both 'OD and 'OE met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{\text{CAS}}$

- remains LOW and $\overline{\text{OE}}$ is taken back LOW after 'OE is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
35. The DQs open during READ cycles once 'OD or 'OFF occur. If $\overline{\text{CAS}}$ goes HIGH first, $\overline{\text{OE}}$ becomes a "don't care." If $\overline{\text{OE}}$ goes HIGH and $\overline{\text{CAS}}$ stays LOW, $\overline{\text{OE}}$ is not a "don't care," and the DQs will provide the previously read data if $\overline{\text{OE}}$ is taken back LOW (while $\overline{\text{CAS}}$ remains LOW).

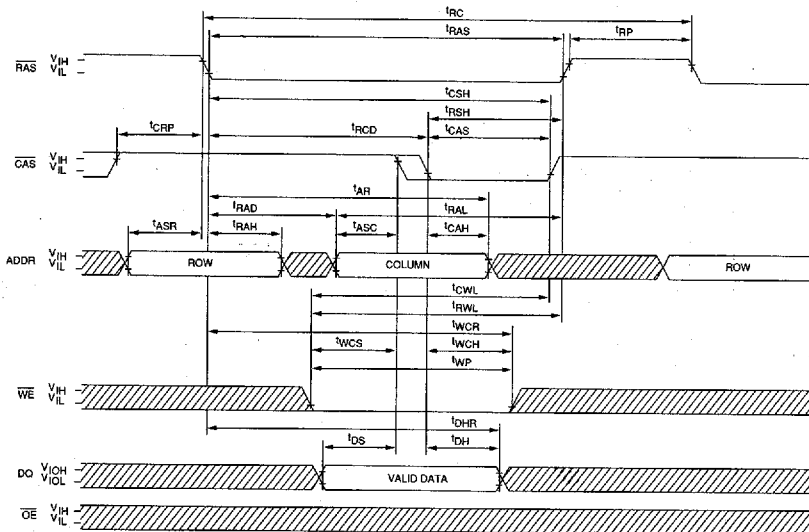
NEW
IC DRAM CARD

READ CYCLE

T-46-23-18



EARLY-WRITE CYCLE



▨ DON'T CARE
▩ UNDEFINED

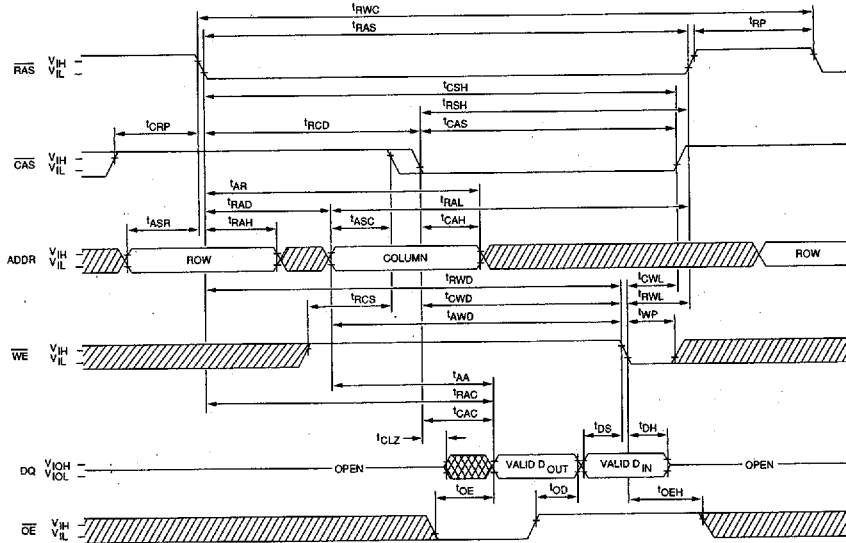
NEW
IC DRAM CARD



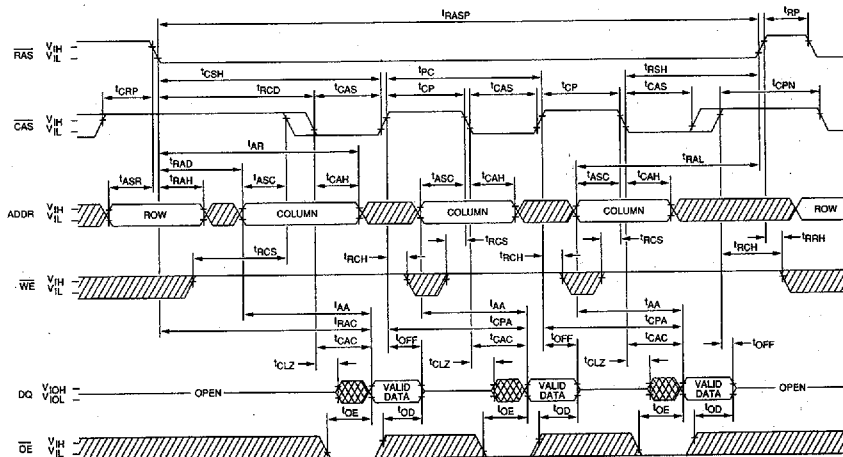
MT8D88C25632
256K x 32, 512K x 16 IC DRAM CARD

T-46-23-18

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



▨ DON'T CARE
▩ UNDEFINED

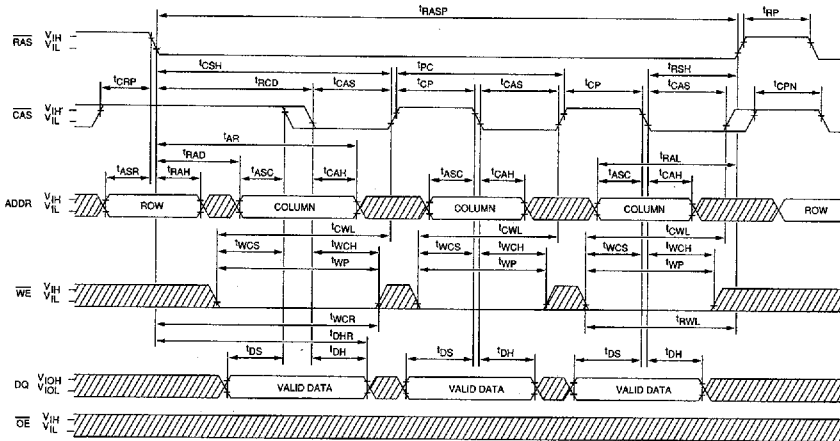
NEW IC DRAM CARD



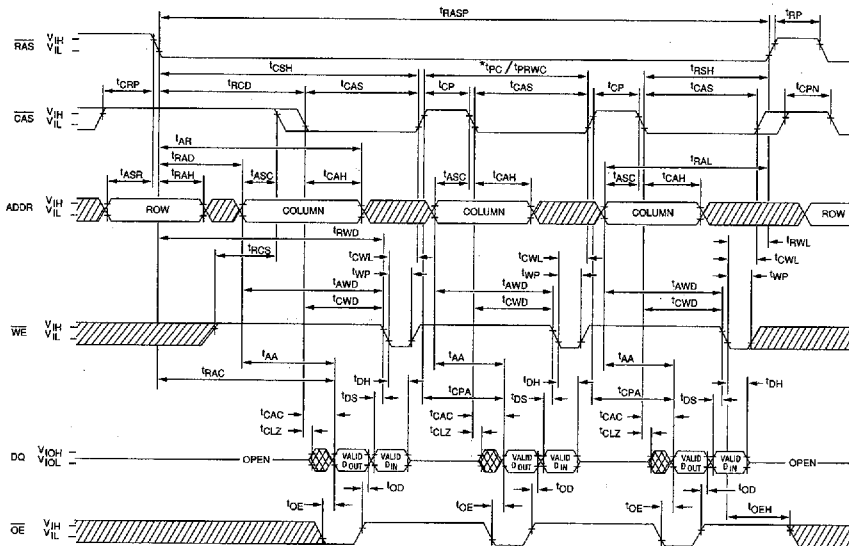
MT8D88C25632
256K x 32, 512K x 16 IC DRAM CARD

FAST-PAGE-MODE EARLY-WRITE CYCLE

T-46-23-18



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



▨ DON'T CARE
▩ UNDEFINED

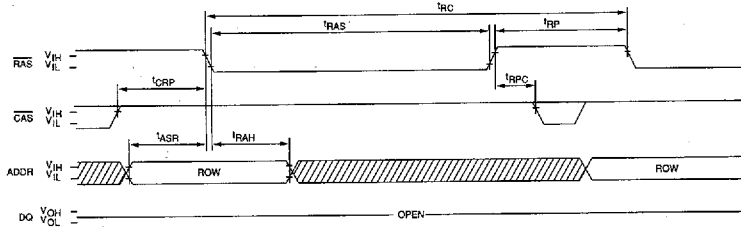
NEW IC DRAM CARD



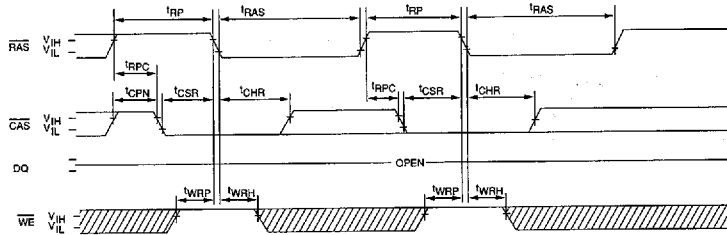
MT8D88C25632
256K x 32, 512K x 16 IC DRAM CARD

RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)

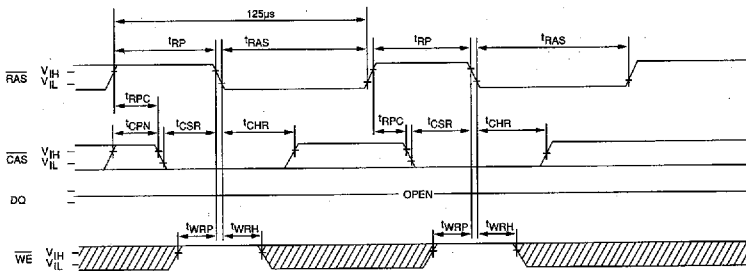
T-46-23-18



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE
(A0-A8 = DON'T CARE)

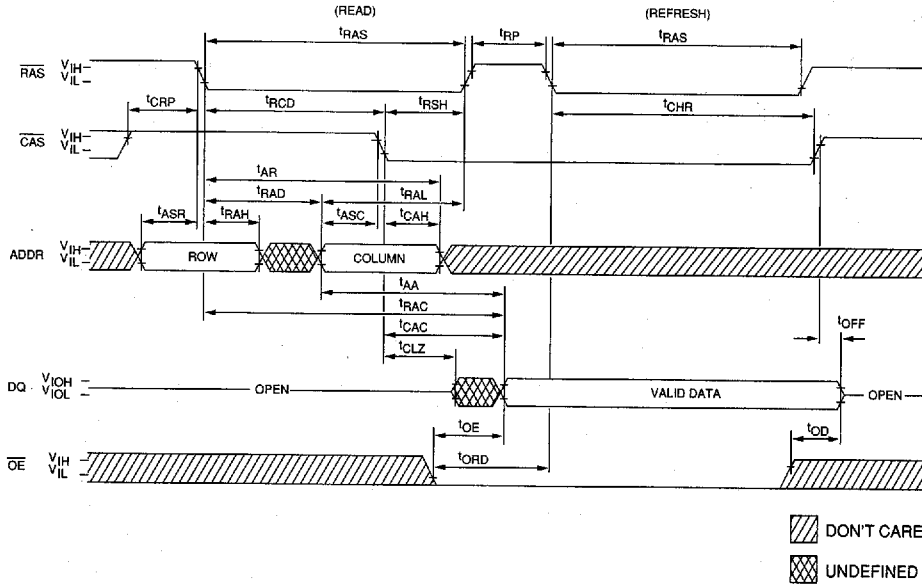


▨ DON'T CARE
▩ UNDEFINED

NEW IC DRAM CARD

HIDDEN REFRESH CYCLE²¹
(WE = HIGH)

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IC DRAM CARD



MT8D88C25632
256K x 32, 512K x 16 IC DRAM CARD

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RESERVED JEDEC, JEIDA and PCMCIA
88-PIN ASSIGNMENT
 (All Possible Combinations)

MT8D88C25632 PIN ASSIGNMENT
 (JEDEC Standard)

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IC DRAM CARD

