AMCC®

FEATURES

- Micro-power Bipolar technology
- Complies with ANSI, Bellcore, and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for OC-48/STM-16 (2488.32 Mbit/s) NRZ data
- 155 MHz reference frequency
- Lock detect—monitors run length and frequency
- Low-jitter PECL interface
- 5V supply

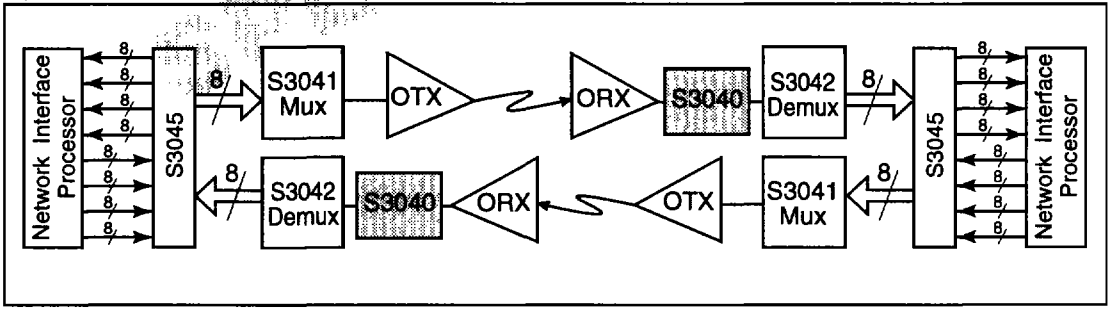
GENERAL DESCRIPTION

The function of the S3040 clock recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3040 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

The S3040 receives an OC-48/STM-16 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential PECL bit clock and retimed data.

The S3040 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

Figure 1. System Block Diagram

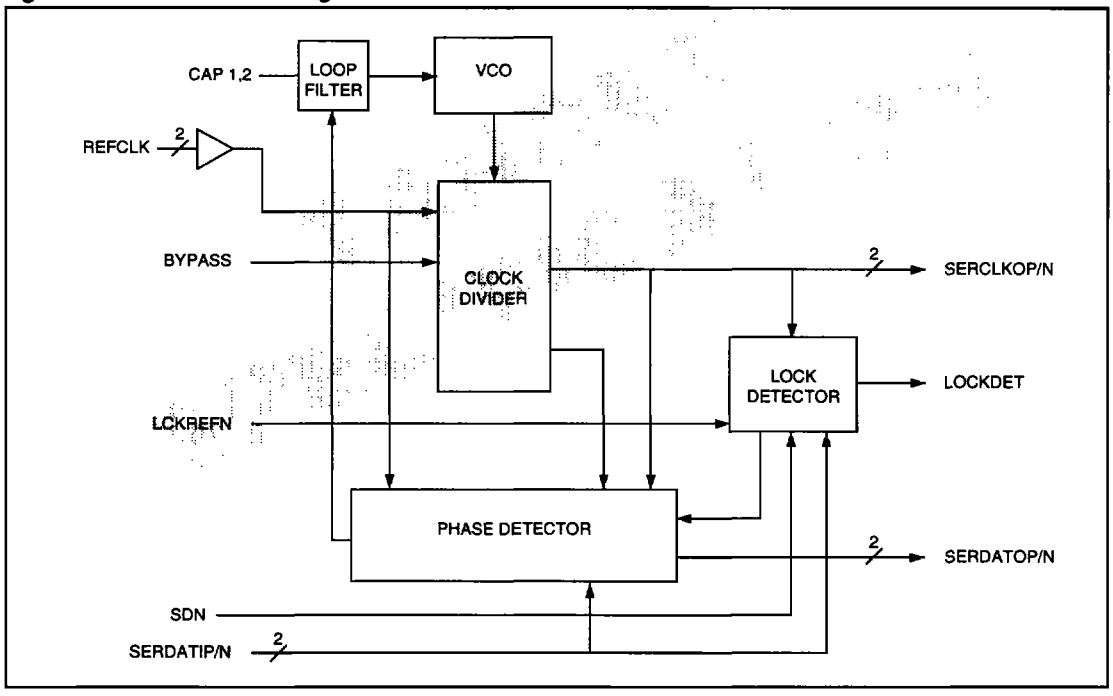


7

S3040 OVERVIEW

The S3040 supports clock recovery for the OC-48/ STM-16 data rate. Differential serial data is input to the chip at the specified rate and clock recovery is performed on the incoming data stream. An external crystal is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3040.

Figure 2. Functional Block Diagram



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