

# OKI Semiconductor

## ML9041

### DOT MATRIX LCD CONTROLLER DRIVER

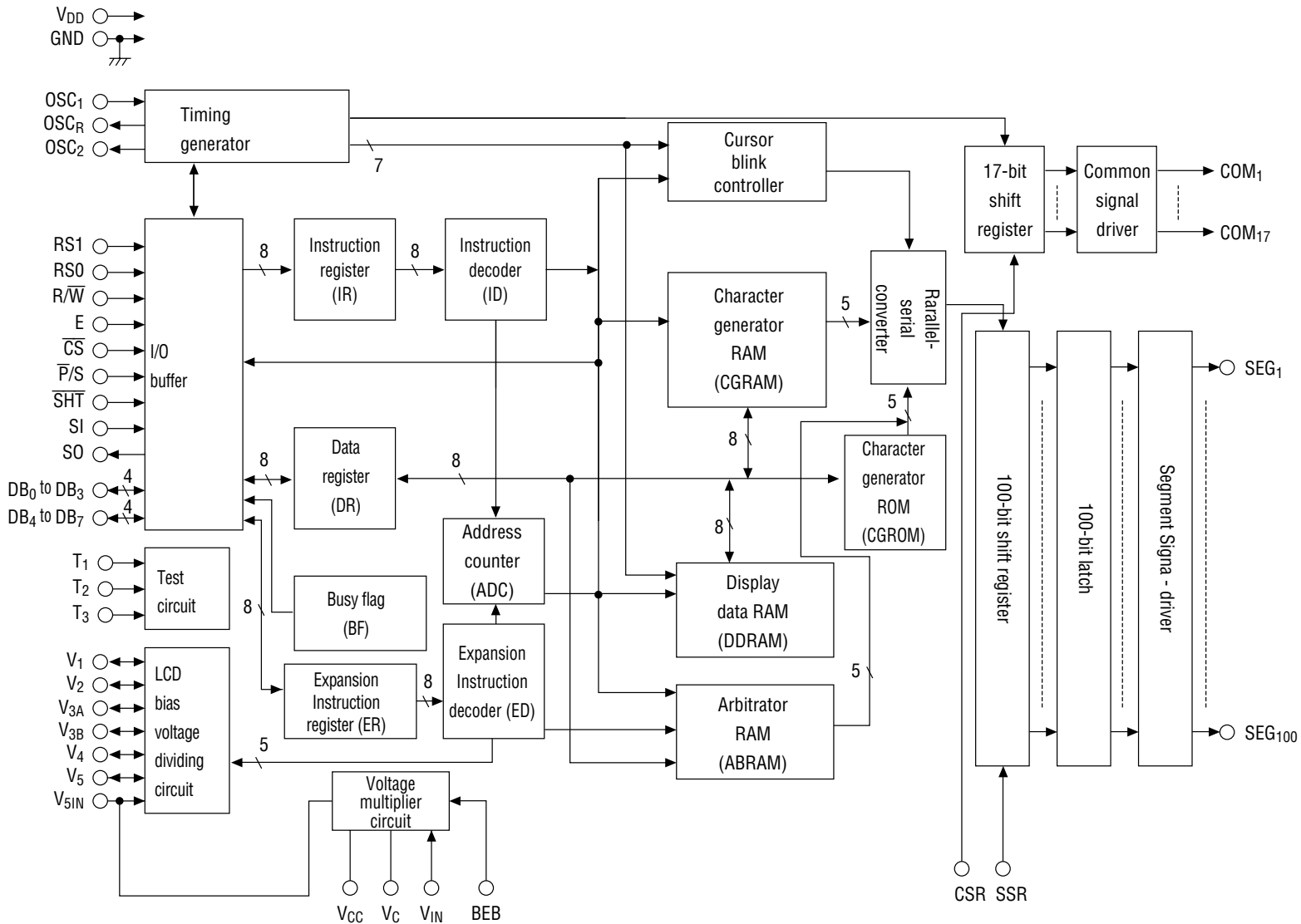
#### GENERAL DESCRIPTION

The ML9041 used in combination with an 8-bit or 4-bit microcontroller controls the operation of a character type dot matrix LCD.

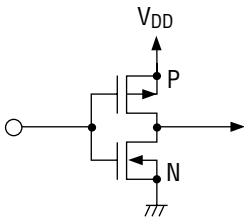
#### FEATURES

- Easy interfacing with 8-bit or 4-bit microcontroller
- Switchable between serial and parallel interfaces
- Dot-matrix LCD controller/driver for a small ( $5 \times 7$  dots) or large ( $5 \times 10$  dots) font
- Built-in circuit allowing automatic resetting at power-on
- Built-in 17 common signal drivers and 100 segment signal drivers
- Built-in character generation ROM capable of generating 160 small characters ( $5 \times 7$  dots) or 32 large characters ( $5 \times 10$  dots)
- Creation of character patterns by programming: up to 8 small character patterns ( $5 \times 8$  dots) or up to 4 large character patterns ( $5 \times 11$  dots)
- Built-in RC oscillation circuit using external or internal resistors
- Program-selectable duties: 1/9 duty (1 line:  $5 \times 7$  dots + cursor + arbitrator), 1/12 duty (1 line:  $5 \times 10$  dots + cursor + arbitrator), or 1/17 duty (2 lines:  $5 \times 7$  dots + cursor + arbitrator)
- Built-in bias dividing resistors to drive the LCD
- Bi-directional transfer of segment outputs
- Bi-directional transfer of common outputs
- Equipped with a 100-dot arbitrator
- Display shifting on each line
- Built-in contrast control circuit
- Built-in voltage multiplier circuit
- Chip (Gold Bump) Product name : ML9041CVWA

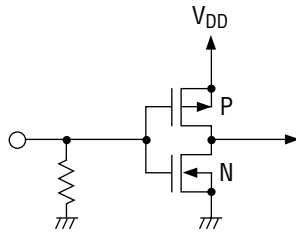
**BLOCK DIAGRAM**



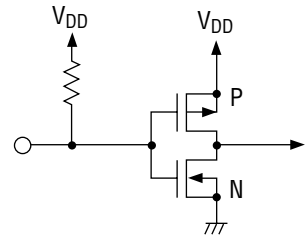
I/O CIRCUITS



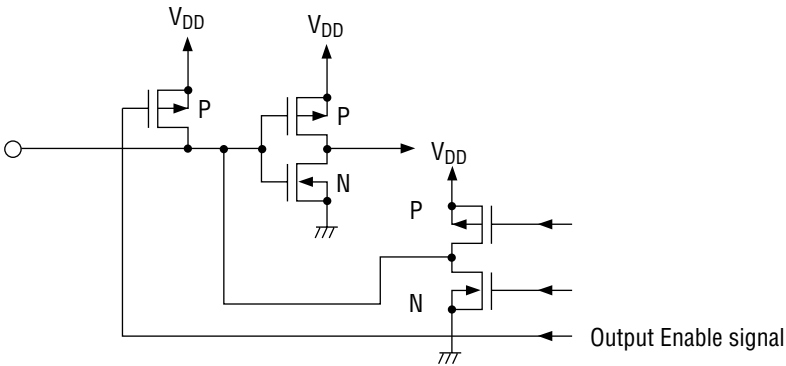
Applied to pins E, SSR, CSR, BEB,  $\overline{CS}$ ,  $\overline{P/S}$ ,  $\overline{SHT}$ , and SI



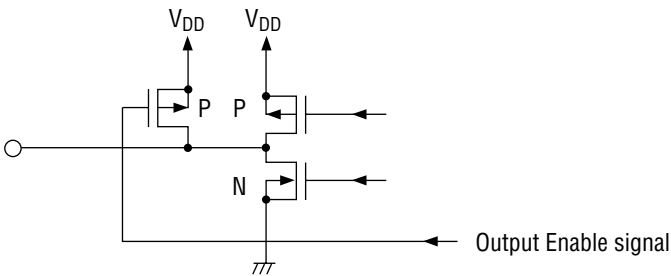
Applied to pins T<sub>1</sub>, T<sub>2</sub>, and T<sub>3</sub>



Applied to pins R $\overline{W}$ , RS<sub>1</sub>, and RS<sub>0</sub>



Applied to pins DB0 to DB7



Applied to pins S0

**PIN DESCRIPTIONS**

| Symbol   | Description   |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |
|--|---|--------------------------------|-----------------|------------------|---|---|---------------|---|---|----------------------|---|---|--------------------------------|
| R/W  | The input pin with a pull-up resistor to select Read (“H”) or Write (“L”) in the Parallel I/F Mode.<br>This pin should be open in the Serial I/F Mode.  |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |
| RS <sub>0</sub> , RS <sub>1</sub>                        | The input pins with a pull-up resistor– to select a register in the Parallel I/F Mode. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">RS<sub>1</sub></th> <th style="text-align: center;">RS<sub>0</sub></th> <th style="text-align: center;">Name of register</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">H</td> <td style="text-align: center;">Data register</td> </tr> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">L</td> <td style="text-align: center;">Instruction register</td> </tr> <tr> <td style="text-align: center;">L</td> <td style="text-align: center;">L</td> <td style="text-align: center;">Expansion Instruction register</td> </tr> </tbody> </table><br>This pin should be open in the Serial I/F Mode. | RS <sub>1</sub>                | RS <sub>0</sub> | Name of register | H | H | Data register | H | L | Instruction register | L | L | Expansion Instruction register |
| RS <sub>1</sub>  | RS <sub>0</sub>   | Name of register               |                 |                  |   |   |               |   |   |                      |   |   |                                |
| H  | H   | Data register                  |                 |                  |   |   |               |   |   |                      |   |   |                                |
| H  | L   | Instruction register           |                 |                  |   |   |               |   |   |                      |   |   |                                |
| L  | L   | Expansion Instruction register |                 |                  |   |   |               |   |   |                      |   |   |                                |
| E  | The input pin for data input/output between the CPU and the ML9041 and for activating instructions in the Parallel I/F Mode.<br>This pin should be open in the Serial I/F Mode.   |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |
| DB <sub>0</sub> to DB <sub>3</sub>                       | The input/output pins to transfer data of lower-order 4 bits between the CPU and the ML9041 in the Parallel I/F Mode. Each pin is equipped with a pull-up resistor. These 4 lines are not used for the 4-bit interface.<br>This pin should be open in the Serial I/F Mode.  |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |
| DB <sub>4</sub> to DB <sub>7</sub>                       | The input/output pins to transfer data of upper 4 bits between the CPU and the ML9041 in the Parallel I/F Mode. Each pin is equipped with a pull-up resistor.<br>This pin should be open in the Serial I/F Mode.  |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |
| OSC <sub>1</sub><br>OSC <sub>2</sub><br>OSC <sub>R</sub> | The clock oscillation pins required for LCD drive signals and the operation of the ML9041 by instructions sent from the CPU.<br>To input external clock, the OSC <sub>1</sub> pin should be used. The OSC <sub>R</sub> and the OSC <sub>2</sub> pins should be open.<br>To start oscillation with an external resistor, the resistor should be connected between the OSC <sub>1</sub> and OSC <sub>2</sub> pins. The OSC <sub>R</sub> pin should be open.<br>To start oscillation with an internal resistor, the OSC <sub>2</sub> and OSC <sub>R</sub> pins should be short-circuited outside the ML9041. The OSC <sub>1</sub> pin should be open.  |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |
| COM <sub>1</sub> to COM <sub>17</sub>                    | The LCD common signal output pins.<br>For 1/9 duty, non-selectable voltage waveforms are output via COM <sub>10</sub> to COM <sub>17</sub> . For 1/12 duty, non-selectable voltage waveforms are output via COM <sub>13</sub> to COM <sub>17</sub> .  |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |
| SEG <sub>1</sub> to SEG <sub>100</sub>                   | The LCD segment signal output pins.   |                                |                 |                  |   |   |               |   |   |                      |   |   |                                |

| Symbol   | Description   |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|--|---|------|---------------------|---------------------|-------------------------|-------------------------|---|-----|---|-------------|------|---|-----|---|-------------------|------|---|------|---|--------------|-------|---|------|---|--------------------|------|---|------|---|--------------|-------|---|------|---|--------------------|------|---|-----|---|-------------|------|---|-----|---|-------------------|------|---|------|---|--------------|------|---|------|---|---------------------|-------|---|------|---|--------------|------|---|------|---|---------------------|-------|
| CSR  | The input pin to select the transfer direction of the common signal output data.<br>Refer to the Expansion Instruction Codes section about the AS bit.  |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | <table border="1"> <thead> <tr> <th>CSR</th> <th>duty</th> <th>AS bit</th> <th>shift direction</th> <th>arbitrator's common pin</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>1/9</td> <td>L</td> <td>COM1 → COM9</td> <td>COM9</td> </tr> <tr> <td>L</td> <td>1/9</td> <td>H</td> <td>COM2 → COM9, COM1</td> <td>COM1</td> </tr> <tr> <td>L</td> <td>1/12</td> <td>L</td> <td>COM1 → COM12</td> <td>COM12</td> </tr> <tr> <td>L</td> <td>1/12</td> <td>H</td> <td>COM2 → COM12, COM1</td> <td>COM1</td> </tr> <tr> <td>L</td> <td>1/17</td> <td>L</td> <td>COM1 → COM17</td> <td>COM17</td> </tr> <tr> <td>L</td> <td>1/17</td> <td>H</td> <td>COM2 → COM17, COM1</td> <td>COM1</td> </tr> <tr> <td>H</td> <td>1/9</td> <td>L</td> <td>COM9 → COM1</td> <td>COM1</td> </tr> <tr> <td>H</td> <td>1/9</td> <td>H</td> <td>COM8 → COM1, COM9</td> <td>COM9</td> </tr> <tr> <td>H</td> <td>1/12</td> <td>L</td> <td>COM12 → COM1</td> <td>COM1</td> </tr> <tr> <td>H</td> <td>1/12</td> <td>H</td> <td>COM11 → COM1, COM12</td> <td>COM12</td> </tr> <tr> <td>H</td> <td>1/17</td> <td>L</td> <td>COM17 → COM1</td> <td>COM1</td> </tr> <tr> <td>H</td> <td>1/17</td> <td>H</td> <td>COM16 → COM1, COM17</td> <td>COM17</td> </tr> </tbody> </table> | CSR  | duty                | AS bit              | shift direction         | arbitrator's common pin | L | 1/9 | L | COM1 → COM9 | COM9 | L | 1/9 | H | COM2 → COM9, COM1 | COM1 | L | 1/12 | L | COM1 → COM12 | COM12 | L | 1/12 | H | COM2 → COM12, COM1 | COM1 | L | 1/17 | L | COM1 → COM17 | COM17 | L | 1/17 | H | COM2 → COM17, COM1 | COM1 | H | 1/9 | L | COM9 → COM1 | COM1 | H | 1/9 | H | COM8 → COM1, COM9 | COM9 | H | 1/12 | L | COM12 → COM1 | COM1 | H | 1/12 | H | COM11 → COM1, COM12 | COM12 | H | 1/17 | L | COM17 → COM1 | COM1 | H | 1/17 | H | COM16 → COM1, COM17 | COM17 |
|  | CSR   | duty | AS bit              | shift direction     | arbitrator's common pin |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | L   | 1/9  | L                   | COM1 → COM9         | COM9                    |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | L   | 1/9  | H                   | COM2 → COM9, COM1   | COM1                    |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | L   | 1/12 | L                   | COM1 → COM12        | COM12                   |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | L   | 1/12 | H                   | COM2 → COM12, COM1  | COM1                    |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | L   | 1/17 | L                   | COM1 → COM17        | COM17                   |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | L   | 1/17 | H                   | COM2 → COM17, COM1  | COM1                    |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | H   | 1/9  | L                   | COM9 → COM1         | COM1                    |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | H   | 1/9  | H                   | COM8 → COM1, COM9   | COM9                    |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | H   | 1/12 | L                   | COM12 → COM1        | COM1                    |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
|  | H   | 1/12 | H                   | COM11 → COM1, COM12 | COM12                   |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| H  | 1/17  | L    | COM17 → COM1        | COM1                |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| H  | 1/17  | H    | COM16 → COM1, COM17 | COM17               |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| SSR  | The input pin to select the transfer direction of the segment signal output data.<br>“L”: Data transfer from SEG <sub>1</sub> to SEG <sub>100</sub><br>“H”: Data transfer from SEG <sub>100</sub> to SEG <sub>1</sub>   |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| V <sub>1</sub> , V <sub>2</sub> , V <sub>3A</sub> , V <sub>3B</sub> , V <sub>4</sub> | The pins to output bias voltages to the LCD.<br>For 1/4 bias : The V <sub>2</sub> and V <sub>3B</sub> pins are shorted.<br>For 1/5 bias : The V <sub>3A</sub> and V <sub>3B</sub> pins are shorted.   |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| BEB  | The input pin to enable or disable the voltage multiplier circuit.<br>“L” disables the voltage multiplier circuit. “H” enables the voltage multiplier circuit.<br>The voltage multiplier circuit doubles the input voltage V <sub>IN</sub> and outputs it to the V <sub>5IN</sub> pin.<br>The voltage multiplier circuit can be used only when generating a level lower than GND.   |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| V <sub>IN</sub>  | The pin to input voltage to the voltage multiplier.   |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| V <sub>5</sub> , V <sub>5IN</sub>  | The pins to supply the LCD drive voltage.<br>The LCD drive voltage is supplied to the V <sub>5</sub> pin when the voltage multiplier is not used (BEB = 0) and the internal contrast adjusting circuit is also not used. At this time, the V <sub>5IN</sub> pin should be open.<br>The LCD drive voltage is supplied to the V <sub>5IN</sub> pin when the voltage multiplier is not used (BEB = 0) but the internal contrast adjusting circuit is used. At this time, the V <sub>5</sub> pin should be open.<br>When the voltage multiplier is used (BEB = 1), the V <sub>5IN</sub> and V <sub>5</sub> pins should be open (the multiplied voltage is output to the V <sub>5IN</sub> pin). In this case, the internal contrast adjusting circuit is used automatically.   |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| V <sub>C</sub>   | The pin to connect the positive pin of the capacitor for the voltage multiplier.  |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |
| V <sub>CC</sub>  | The pin to connect the negative pin of the capacitor used for the voltage multiplier.   |      |                     |                     |                         |                         |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |       |   |      |   |                    |      |   |      |   |              |       |   |      |   |                    |      |   |     |   |             |      |   |     |   |                   |      |   |      |   |              |      |   |      |   |                     |       |   |      |   |              |      |   |      |   |                     |       |

| Symbol   | Description   |
|--|---|
| T <sub>1</sub> , T <sub>2</sub> , T <sub>3</sub> | The input pins for test circuits (normally open). Equipped with a pull-down resistor.   |
| V <sub>DD</sub>                                  | The power supply pin.   |
| GND  | The ground level input pin.   |
| $\overline{P/S}$                                 | The input pin to select the parallel or serial interface.<br>“L” selects the parallel interface.<br>“H” selects the serial interface.   |
| $\overline{CS}$                                  | The pin to enable this IC in the serial I/F mode.<br>“L” enables this IC.<br>“H” disables this IC.<br>This pin should be open in the parallel I/F mode.   |
| $\overline{SHT}$                                 | The pin to input shift clock in the serial I/F mode.<br>Data inputting to the SI pin is carried out synchronizing with the rising edge of this clock signal.<br>Data outputting from the SO pin is carried out synchronizing with the falling edge of this clock signal.<br>This pin should be open in the parallel I/F mode. |
| SI   | The pin to input DATA in the serial I/F mode.<br>Data inputting to this pin is carried out synchronizing with the rising edge of the $\overline{SHT}$ signal.<br>This pin should be open in the parallel I/F mode.  |
| SO   | The pin to output DATA in the serial I/F mode.<br>Data inputting to this pin is carried out synchronizing with the falling edge of the $\overline{SHT}$ signal.<br>This pin should be open in the parallel I/F mode.  |

**ABSOLUTE MAXIMUM RATINGS**

(GND = 0V)

| Parameter           | Symbol                    | Condition                | Rating                           | Unit             | Applicable pins  |
|---------------------|---------------------------|--------------------------|----------------------------------|------------------|--|
| Supply Voltage      | $V_{DD}$                  | $T_a = 25^\circ\text{C}$ | -0.3 to +6.5                     | V                | $V_{DD} - \text{GND}$  |
| LCD Driving Voltage | $V_1, V_2, V_3, V_4, V_5$ | $T_a = 25^\circ\text{C}$ | $V_{DD} - 7.5$ to $V_{DD} + 0.3$ | V                | $V_1, V_4, V_5, V_{5IN}, V_2, V_{3A}, V_{3B}$  |
| Input Voltage       | $V_i$                     | $T_a = 25^\circ\text{C}$ | -0.3 to $V_{DD} + 0.3$           | V                | $R/\bar{W}, E, \text{SHT}, \text{CSR}, \bar{P}/\text{S}, \text{SSR}, \text{SI}, \text{RS}_0, \text{RS}_1, \text{BEB}, \bar{\text{CS}}, T_1$ to $T_3, \text{DB}_0$ to $\text{DB}_7, V_{IN}$ |
| Storage Temperature | $T_{STG}$                 | —                        | -55 to +125                      | $^\circ\text{C}$ | —  |

**RECOMMENDED OPERATING CONDITIONS**

(GND = 0V)

| Parameter             | Symbol                       | Condition | Range                             | Unit             | Applicable pins                 |
|-----------------------|------------------------------|-----------|-----------------------------------|------------------|---------------------------------|
| Supply Voltage        | $V_{DD}$                     | —         | 2.5 to 5.5                        | V                | $V_{DD} - \text{GND}$           |
| LCD Driving Voltage   | $V_{DD} - V_5$<br>(See Note) | —         | 2.8 to 7.0                        | V                | $V_{DD} - V_5$<br>( $V_{5IN}$ ) |
| Input Voltage         | $V_{IN}$                     | BEB = 1   | $V_{DD} - 1.40$ to $V_{DD} - 3.5$ | V                | $V_{DD} - V_{IN}$               |
| Operating Temperature | $T_{op}$                     | —         | -40 to +85                        | $^\circ\text{C}$ | —                               |

Note: This voltage should be applied across  $V_{DD}$  and  $V_5$ . The following voltages are output to the  $V_1, V_2, V_{3A}$  ( $V_{3B}$ ) and  $V_4$  pins:

- 1/4 bias

$$V_1 = \{V_{DD} - (V_{DD} - V_5) / 4\} \pm 0.15\text{V}$$

$$V_2 = V_{3B} = \{V_{DD} - (V_{DD} - V_5) / 2\} \pm 0.15\text{V}$$

$$V_4 = \{V_{DD} - 3 \times (V_{DD} - V_5) / 4\} \pm 0.15\text{V}$$

- 1/5 bias

$$V_1 = \{V_{DD} - (V_{DD} - V_5) / 5\} \pm 0.15\text{V}$$

$$V_2 = \{V_{DD} - 2 \times (V_{DD} - V_5) / 5\} \pm 0.15\text{V}$$

$$V_{3A} = V_{3B} = \{V_{DD} - 3 \times (V_{DD} - V_5) / 5\} \pm 0.15\text{V}$$

$$V_4 = \{V_{DD} - 4 \times (V_{DD} - V_5) / 5\} \pm 0.15\text{V}$$

The voltages at the  $V_1, V_2, V_{3A}$  ( $V_{3B}$ ),  $V_4$  and  $V_5$  pins should satisfy

$$V_{DD} > V_1 > V_2 > V_{3A} (V_{3B}) > V_4 > V_5.$$

(Higher ← → Lower)

\* Do not apply short-circuiting across output pins and across an output pin and an input/output pin or the power supply pin in the output mode.

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

(GND = 0V, V<sub>DD</sub> = 2.5V to 5.5V, T<sub>a</sub> = -40 to +85°C)

| Parameter   | Symbol                | Condition  | Min   | Typ                   | Max                | Unit                 | Applicable pin   |   |
|---|-----------------------|--|---|-----------------------|--------------------|----------------------|--|---|
| “H” Input Voltage 1                                       | V <sub>IH1</sub>      | —  | 0.8V <sub>DD</sub>  | —                     | V <sub>DD</sub>    | V                    | R/W, RS <sub>0</sub> , RS <sub>1</sub> ,<br>E, DB <sub>0</sub> to DB <sub>7</sub><br>SHT, P/S, SI, CS                    |   |
| “L” Input Voltage 1                                       | V <sub>IL1</sub>      | —  | -0.3  | —                     | 0.2V <sub>DD</sub> |                      |  |   |
| “H” Input Voltage 2                                       | V <sub>IH2</sub>      | —  | 0.8V <sub>DD</sub>  | —                     | V <sub>DD</sub>    | V                    | OSC <sub>1</sub> ,<br>SSR, CSR, BEB  |   |
| “L” Input Voltage 2                                       | V <sub>IL2</sub>      | —  | -0.3  | —                     | 0.2V <sub>DD</sub> |                      |  |   |
| “H” Output Voltage 1                                      | V <sub>OH1</sub>      | I <sub>OH</sub> = -0.1mA   | 0.75V <sub>DD</sub>   | —                     | —                  | V                    | DB <sub>0</sub> to DB <sub>7</sub> , SO  |   |
| “L” Output Voltage 1                                      | V <sub>OL1</sub>      | I <sub>OL</sub> = +0.1mA   | —   | —                     | 0.2V <sub>DD</sub> |                      |  |   |
| “H” Output Voltage 2                                      | V <sub>OH2</sub>      | I <sub>OH</sub> = -13μA  | 0.9V <sub>DD</sub>  | —                     | —                  | V                    | OSC <sub>2</sub>   |   |
| “L” Output Voltage 2                                      | V <sub>OL2</sub>      | I <sub>OL</sub> = +13μA  | —   | —                     | 0.1V <sub>DD</sub> |                      |  |   |
| COM Voltage Drop  | V <sub>CH</sub>       | I <sub>OCH</sub> = -4μA  | V <sub>DD</sub> - V <sub>5</sub> = 5V<br>Note 1                           | V <sub>DD</sub> - 0.3 | —                  | V <sub>DD</sub>      | V  | COM <sub>1</sub> to COM <sub>17</sub>                     |
|   | V <sub>CMH</sub>      | I <sub>OCMH</sub> = ±4μA   |   | V <sub>1</sub> - 0.3  | —                  | V <sub>1</sub> + 0.3 |  |   |
|   | V <sub>CML</sub>      | I <sub>OCML</sub> = ±4μA   |   | V <sub>4</sub> - 0.3  | —                  | V <sub>4</sub> + 0.3 |  |   |
|   | V <sub>CL</sub>       | I <sub>OCL</sub> = +4μA  |   | V <sub>5</sub>        | —                  | V <sub>5</sub> + 0.3 |  |   |
| SEG Voltage Drop  | V <sub>SH</sub>       | I <sub>OSH</sub> = -4μA  | V <sub>DD</sub> - V <sub>5</sub> = 5V<br>Note 1                           | V <sub>DD</sub> - 0.3 | —                  | V <sub>DD</sub>      | V  | SEG <sub>1</sub> to SEG <sub>100</sub>                    |
|   | V <sub>SMH</sub>      | I <sub>OSMH</sub> = ±4μA   |   | V <sub>2</sub> - 0.3  | —                  | V <sub>2</sub> + 0.3 |  |   |
|   | V <sub>SML</sub>      | I <sub>OSML</sub> = ±4μA   |   | V <sub>3</sub> - 0.3  | —                  | V <sub>3</sub> + 0.3 |  |   |
|   | V <sub>SL</sub>       | I <sub>OSL</sub> = +4μA  |   | V <sub>5</sub>        | —                  | V <sub>5</sub> + 0.3 |  |   |
| Input Leakage Current                                     | I <sub>IIL</sub>      | V <sub>DD</sub> = 5V, V <sub>IN</sub> = 5V or 0V   | —   | —                     | 1.0                | μA                   | E, SSR, CSR, BEB,<br>SHT, P/S, CS, SI  |   |
| Input Current 1   | I <sub>I11</sub>      | V <sub>DD</sub> = 5V, V <sub>IN</sub> = GND  | 10  | 25                    | 61                 | μA                   | R/W, RS <sub>0</sub> , RS <sub>1</sub><br>DB <sub>0</sub> to DB <sub>7</sub> , SO  |   |
|   |                       | V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> ,<br>Excluding current flowing<br>through the pull-up resistor<br>and the output driving MOS | —   | —                     | 2.0                |                      |  |   |
| Input Current 2   | I <sub>I21</sub>      | V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub>  | 15  | 45                    | 105                | μA                   | T <sub>1</sub> , T <sub>2</sub> , T <sub>3</sub>   |   |
|   |                       | V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> ,<br>Excluding current flowing<br>through the pull-down resistor                             | —   | —                     | 2.0                |                      |  |   |
| Supply Current  | I <sub>DD</sub>       | V <sub>DD</sub> = 5V   | —   | —                     | 1.2                | mA                   | V <sub>DD</sub> - GND  |   |
| LCD Bias Resistor   | R <sub>LB</sub>       |  |   | 4.0                   |                    | kΩ                   | V <sub>DD</sub> , V <sub>1</sub> , V <sub>2</sub><br>V <sub>3A</sub> , V <sub>3B</sub> , V <sub>4</sub> , V <sub>5</sub> |   |
| Oscillation Frequency of External Resistor R <sub>f</sub> | f <sub>osc1</sub>     | R <sub>f</sub> = 120kΩ±2%  | Note 3  | 175                   | 270                | 350                  | kHz  | OSC <sub>1</sub> , OSC <sub>2</sub>                       |
| Oscillation Frequency of Internal Resistor R <sub>f</sub> | f <sub>osc2</sub>     | OSC <sub>1</sub> : Open<br>OSC <sub>2</sub> and OSC <sub>R</sub> : Short-circuited   | Note 4  | 140                   | 270                | 480                  | kHz  | OSC <sub>1</sub> , OSC <sub>2</sub> ,<br>OSC <sub>R</sub> |
| External Clock  | Clock Input Frequency | f <sub>in</sub>  | OSC <sub>2</sub> , OSC <sub>R</sub> : Open<br>Input from OSC <sub>1</sub> | 125                   |                    | 480                  | kHz  | OSC <sub>1</sub>  |
|   | Input Clock Duty      | f <sub>duty</sub>  | Note 5  | 45                    | 50                 | 55                   | %  |   |
|   | Input Clock Rise Time | f <sub>rf</sub>  | Note 6  | —                     | —                  | 0.2                  | μS   |   |
|   | Input Clock Fall Time | f <sub>ff</sub>  | Note 6  | —                     | —                  | 0.2                  | μS   |   |

(GND = 0V, V<sub>DD</sub> = 2.5V to 5.5V, Ta = -40 to +85°C)

| Parameter  | Symbol               | Condition   |          | Min                                | Typ | Max   | Unit | Applicable pin                    |
|--|----------------------|---|----------|------------------------------------|-----|---|------|-----------------------------------|
| Control Range of LCD Driving Voltage (by internal variable resistor) | V <sub>LCD</sub> MAX | V <sub>DD</sub> = 5V, 1/5 bias<br>V <sub>5IN</sub> = 0V |          | TBD                                | —   |   |      | V <sub>DD</sub> - V <sub>5</sub>  |
|  | V <sub>LCD</sub> MIN | V <sub>DD</sub> = 5V, 1/5 bias<br>V <sub>5IN</sub> = 0V |          |                                    | —   | TBD   |      |                                   |
| Bias Voltage for Driving LCD by External Input                       | V <sub>LCD1</sub>    | V <sub>DD</sub> - V <sub>5</sub>                        | 1/5 bias | 2.8                                | —   | 7.0   | V    | V <sub>5</sub>                    |
|  | V <sub>LCD2</sub>    | Note 7  | 1/4 bias | 2.8                                | —   | 7.0   |      |                                   |
| Voltage Multiplier Output Voltage                                    | V5OUT                | V <sub>DD</sub> = 3V, V <sub>IN</sub> = 0V<br>BEB = H   |          | V <sub>DD</sub> - 2V <sub>IN</sub> | —   | V <sub>DD</sub> - 2V <sub>IN</sub><br>+1.2V | V    | V <sub>5</sub> , V <sub>5IN</sub> |
| Voltage Multiplier Input Voltage                                     | V <sub>IN</sub>      |   |          |                                    |     | V <sub>DD</sub> /2                          | V    | V <sub>IN</sub>                   |

Note 1: Applied to the voltage drop occurring between any of the  $V_{DD}$ ,  $V_1$ ,  $V_4$  and  $V_5$  pins and any of the common pins ( $COM_1$  to  $COM_{17}$ ) when the current of  $4\mu A$  flows in or flows out at one common pin.

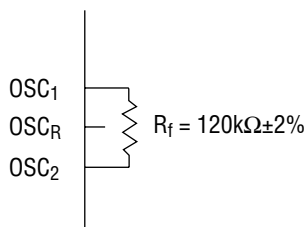
Also applied to the voltage drop occurring between any of the  $V_{DD}$ ,  $V_2$ ,  $V_{3A}$  ( $V_{3B}$ ) and  $V_5$  pins and any of the segment pins ( $SEG_1$  to  $SEG_{100}$ ) when the current of  $4\mu A$  flows in or flows out at one common pin.

The current of  $4\mu A$  flows out when the output level is  $V_{DD}$  or flows in when the output level is  $V_5$ .

Note 2: Applied to the current flowing into the  $V_{DD}$  pin when the external clock ( $f_{osc2} = f_{in} = 270\text{ kHz}$ ) is fed to the internal  $R_f$  oscillation or  $OSC_1$  under the following conditions:

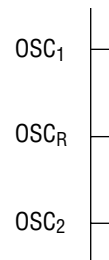
- $V_{DD} = 5V$
- $GND = V_5 = 0V$ ,
- $V_1, V_2, V_{3A}$  ( $V_{3B}$ ) and  $V_4$ : Open
- E, SSR, CSR, and BEB: "L" (fixed)
- Other input pins: "L" or "H" (fixed)
- Other output pins: No load

Note 3:



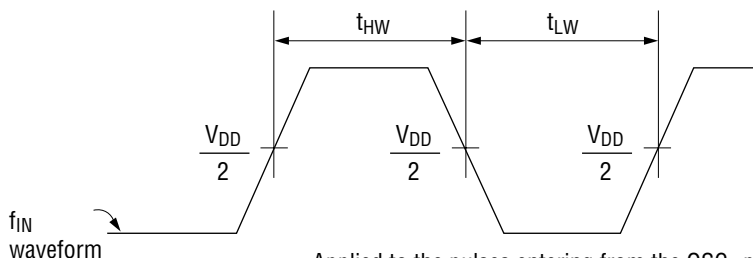
The wire between  $OSC_1$  and  $R_f$  and the wire between  $OSC_2$  and  $R_f$  should be as short as possible. Keep  $OSCR$  open.

Note 4:



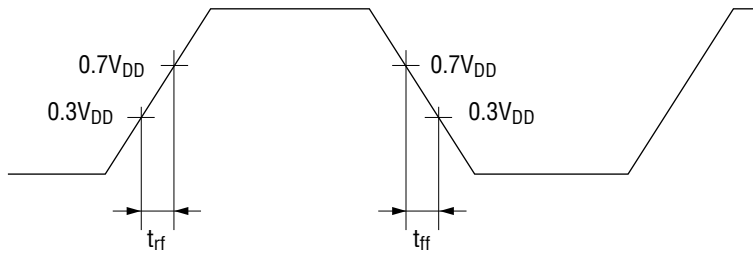
The wire between  $OSC_2$  and  $OSCR$  should be as short as possible. Keep  $OSC_1$  open.

Note 5:



Applied to the pulses entering from the  $OSC_1$  pin  
 $f_{duty} = t_{HW} / (t_{HW} + t_{LW}) \times 100 (\%)$

Note 6:



Applied to the pulses entering from the OSC<sub>1</sub> pin

Note 7: For 1/4 bias, V<sub>2</sub> and V<sub>3B</sub> pins are short-circuited. V<sub>3A</sub> pin is open.  
For 1/5 bias, V<sub>3A</sub> and V<sub>3B</sub> pins are short-circuited. V<sub>2</sub> pin is open.

**Switching Characteristics (The following ratings are subject to change after ES evaluation.)**

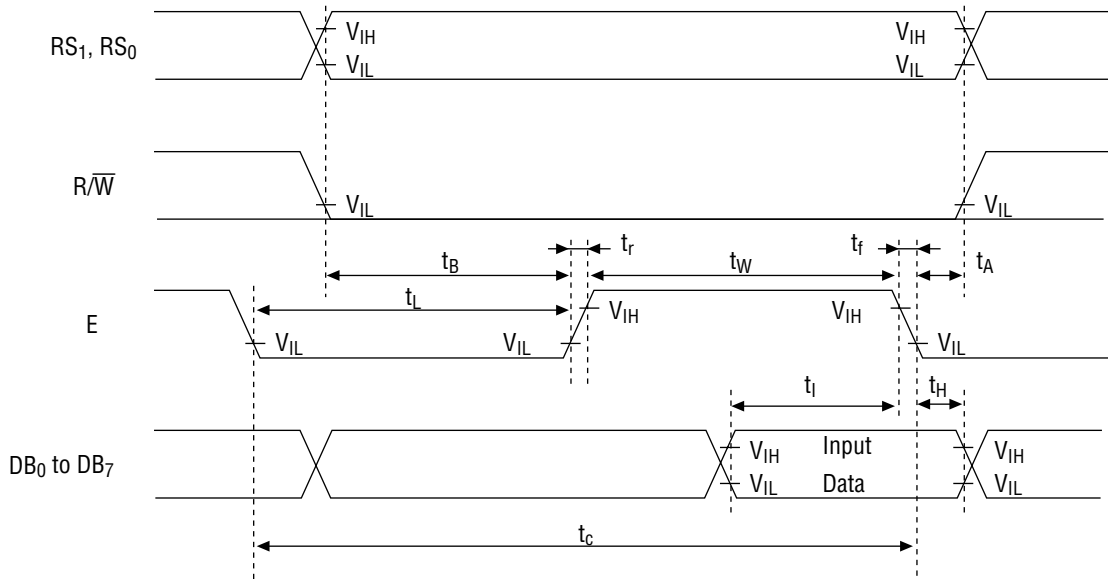
• Parallel Interface Mode

The timing for the input from the CPU (see 1) and the timing for the output to the CPU (see 2) are as shown below:

1) WRITE MODE (Timing for input from the CPU)

( $V_{DD} = 2.5$  to  $5.5V$ ,  $T_a = -40$  to  $+85^\circ C$ )

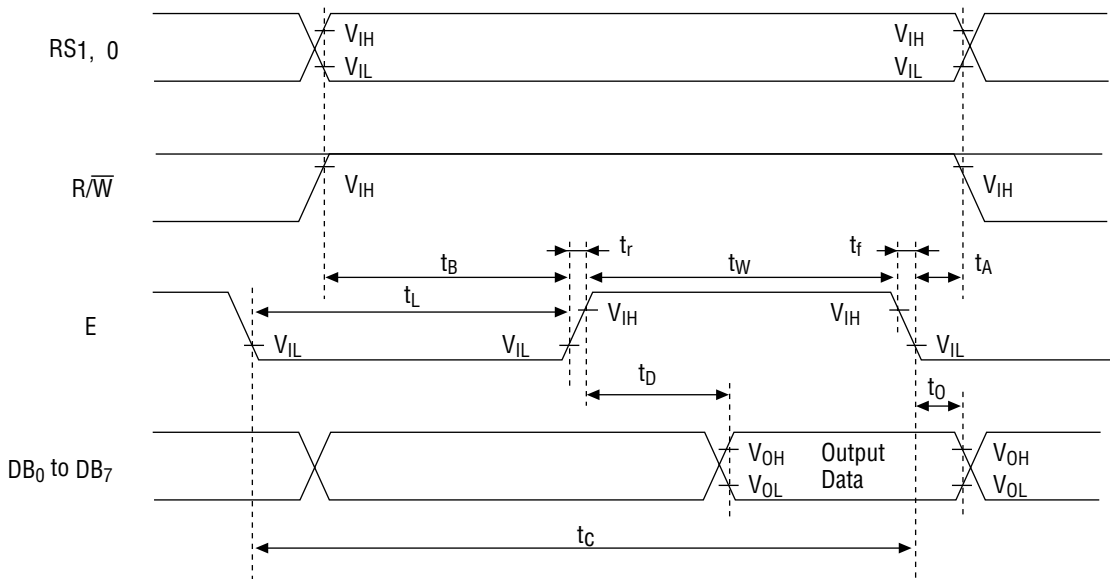
| Parameter                                     | Symbol | Min  | Typ | Max | Unit |
|---|--------|------|-----|-----|------|
| $R/\overline{W}$ , $RS_0$ , $RS_1$ Setup time | $t_B$  | 40   | —   | —   | ns   |
| E Pulse Width                                 | $t_W$  | 450  | —   | —   | ns   |
| $R/\overline{W}$ , $RS_0$ , $RS_1$ Hold time  | $t_A$  | 10   | —   | —   | ns   |
| E Rise Time                                   | $t_r$  | —    | —   | 25  | ns   |
| E Fall Time                                   | $t_f$  | —    | —   | 25  | ns   |
| E Pulse Width                                 | $t_L$  | 430  | —   | —   | ns   |
| E Cycle Time                                  | $t_C$  | 1000 | —   | —   | ns   |
| $DB_0$ to $DB_7$ Input Data Hold time         | $t_I$  | 195  | —   | —   | ns   |
| $DB_0$ to $DB_7$ Input Data Setup time        | $t_H$  | 10   | —   | —   | ns   |



2) READ MODE (Timing for output to the CPU)

( $V_{DD} = 2.5$  to  $5.5V$ ,  $T_a = -40$  to  $+85^{\circ}C$ )

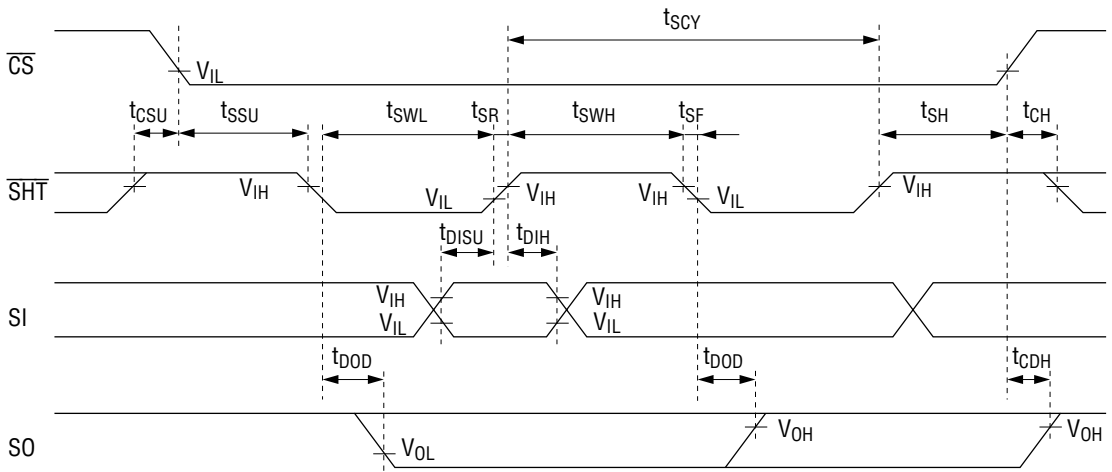
| Parameter   | Symbol | Min  | Typ | Max | Unit |
|---|--------|------|-----|-----|------|
| R/W, RS <sub>1</sub> , RS <sub>0</sub> Setup Time         | $t_B$  | 40   | —   | —   | ns   |
| E Pulse Width   | $t_W$  | 450  | —   | —   | ns   |
| R/W, RS <sub>1</sub> , RS <sub>0</sub> Hold Time          | $t_A$  | 10   | —   | —   | ns   |
| E Rise Time   | $t_r$  | —    | —   | 25  | ns   |
| E Fall Time   | $t_f$  | —    | —   | 25  | ns   |
| E Pulse Width   | $t_L$  | 430  | —   | —   | ns   |
| E Cycle Time  | $t_C$  | 1000 | —   | —   | ns   |
| DB <sub>0</sub> to DB <sub>7</sub> Output Data Delay Time | $t_D$  | —    | —   | 350 | ns   |
| DB <sub>0</sub> to DB <sub>7</sub> Output Data Hold Time  | $t_O$  | 20   | —   | —   | ns   |



• Serial Interface Mode

( $V_{DD} = 2.5$  to  $5.5V$ ,  $T_a = -40$  to  $+85^{\circ}C$ )

| Parameter                        | Symbol     | Min | Typ | Max | Unit |
|----------------------------------|------------|-----|-----|-----|------|
| $\overline{SHT}$ Cycle Time      | $t_{SCY}$  | 500 | —   | —   | ns   |
| $\overline{CS}$ Setup Time       | $t_{CSU}$  | 100 | —   | —   | ns   |
| $\overline{CS}$ Hold Time        | $t_{CH}$   | 100 | —   | —   | ns   |
| $\overline{SHT}$ Setup Time      | $t_{SSU}$  | 60  | —   | —   | ns   |
| $\overline{SHT}$ Hold Time       | $t_{SH}$   | 200 | —   | —   | ns   |
| $\overline{SHT}$ "H" Pulse Width | $t_{SWH}$  | 200 | —   | —   | ns   |
| $\overline{SHT}$ "L" Pulse Width | $t_{SWL}$  | 200 | —   | —   | ns   |
| $\overline{SHT}$ Rise Time       | $t_{SR}$   | —   | —   | 50  | ns   |
| $\overline{SHT}$ Fall Time       | $t_{SF}$   | —   | —   | 50  | ns   |
| SI Setup Time                    | $t_{DISU}$ | 100 | —   | —   | ns   |
| SI Hold Time                     | $t_{DIH}$  | 100 | —   | —   | ns   |
| Data Output Delay Time           | $t_{DOD}$  | —   | —   | 160 | ns   |
| Data Output Hold Time            | $t_{CDH}$  | 0   | —   | —   | ns   |



## FUNCTIONAL DESCRIPTION

### Instruction Register (IR), Data Register (DR), and Expansion Instruction Register (ER)

These registers are selected by setting the level of the Register Selection input pins RS<sub>0</sub> and RS<sub>1</sub>. The DR is selected when both RS<sub>0</sub> and RS<sub>1</sub> are "H". The IR is selected when RS<sub>0</sub> is "L" and RS<sub>1</sub> is "H". The ER is selected when both RS<sub>0</sub> and RS<sub>1</sub> are "L". (When RS<sub>0</sub> is "H" and RS<sub>1</sub> is "L", the ML9041 is not selected.)

The IR stores an instruction code and the address code of the display data RAM (DDRAM) or the character generator RAM (CGRAM).

The microcontroller (CPU) can write to the IR but cannot read from the IR.

The ER stores a contrast adjusting code and the address code of the arbitrator RAM (ABRAM).

The CPU can write to or read from the ER.

The DR stores data to be written in the DDRAM, ABRAM and CGRAM and also stores data read from the DDRAM, AMRAM and CGRAM.

The data written in the DR by the CPU is automatically written in the DDRAM, ABRAM or CGRAM.

When an address code is written in the IR or ER, the data of the specified address is automatically transferred from the DDRAM, ABRAM or CGRAM to the DR. The data of the DDRAM, ABRAM and CGRAM can be checked by allowing the CPU to read the data stored in the DR.

After the CPU writes data in the DR, the data of the next address in the DDRAM, ABRAM or CGRAM is selected to be ready for the next writing by the CPU. Similarly, after the CPU reads the data in the DR, the data of the next address in the DDRAM, ABRAM or CGRAM is set in the DR to be ready for the next reading by the CPU.

Writing in or reading from these 3 registers is controlled by changing the status of the R/ $\overline{W}$  (Read/Write) pin.

**Table 1 R/ $\overline{W}$  pin status and register operation**

| R/ $\overline{W}$ | RS <sub>0</sub> | RS <sub>1</sub> | Operation  |
|-------------------|-----------------|-----------------|--|
| L                 | L               | H               | Writing in the IR  |
| H                 | L               | H               | Reading the Busy flag (BF) and the address counter (ADC) |
| L                 | H               | H               | Writing in the DR  |
| H                 | H               | H               | Reading from the DR                                      |
| L                 | L               | L               | Writing in the ER  |
| H                 | L               | L               | Reading the contrast code                                |

### Busy Flag (BF)

The status "1" of the Busy Flag (BF) indicates that the ML9041 is carrying out internal operation. When the BF is "1", any new instruction is ignored.

When R/ $\overline{W}$  = "H", RS<sub>0</sub> = "L" and RS<sub>1</sub> = "H", the data in the BF is output to the DB<sub>7</sub>.

New instructions should be input when the BF is "0".

When the BF is "1", the output code of the address counter (ADC) is undefined.

**Address Counter (ADC)**

The address counter provides a read/write address for the DDRAM, ABRAM or CGRAM and also provides a cursor display address.

When an instruction code specifying DDRAM, ABRAM or CGRAM address setting is input to the pre-defined register, the register selects the specified DDRAM, ABRAM or CGRAM and transfers the address code to the ADC. The address data in the ADC is automatically incremented (or decremented) by 1 after the display data is written in or read from the DDRAM, ABRAM or CGRAM.

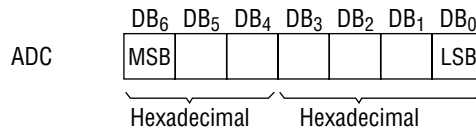
The data in the ADC is output to DB<sub>0</sub> to DB<sub>6</sub> when  $R/\overline{W} = "H"$ , RS<sub>0</sub> = "L", RS<sub>1</sub> = "H" and BF = "0".

**Timing Generator**

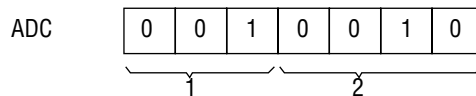
The timing generator generates timing signals for the internal operation of the ML9041 activated by the instruction sent from the CPU or for the operation of the internal circuits of the ML9041 such as DDRAM, ABRAM, CGRAM and CGROM. Timing signals are generated so that the internal operation carried out for LCD displaying will not be interfered by the internal operation initiated by accessing from the CPU. For example, when the CPU writes data in the DDRAM, the display of the LCD not corresponding to the written data is not affected.

**Display Data RAM (DDRAM)**

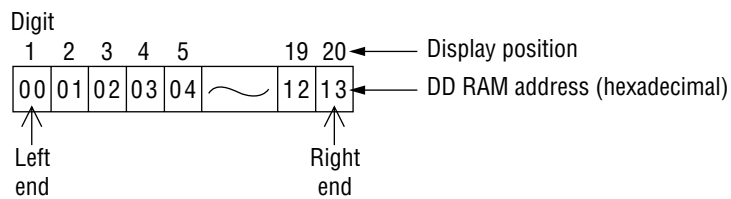
This RAM stores the display data represented in 8-bit character coding (see Table 2). The DDRAM addresses correspond to the display positions (digits) of the LCD as shown below. The DDRAM addresses (to be set in the ADC) are represented in hexadecimal.



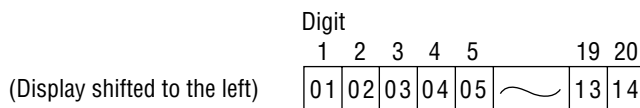
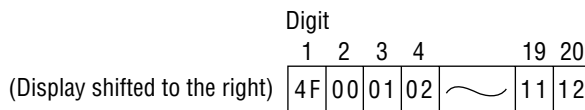
(Example) Representation of DDRAM address = 12



1) Relationship between DDRAM addresses and display positions (1-line display mode)



In the 1-line display mode, the ML9041 can display up to 20 characters from digit 1 to digit 20. While the DDRAM has addresses "00" to "4F" for up to 80 character codes, the area not used for display can be used as a RAM area for general data. When the display is shifted by instruction, the relationship between the LCD display and the DDRAM address changes as shown below:



2) Relationship between DDRAM addresses and display positions (2-line display mode)

In the 2-line mode, the ML9041 can display up to 40 characters (20 characters per line) from digit 1 to digit 20.

|        |  | Digit |    |    |    |    |    |    |                    |                                   |
|--------|--|-------|----|----|----|----|----|----|--------------------|-----------------------------------|
|        |  | 1     | 2  | 3  | 4  | 5  | 19 | 20 | ← Display position |                                   |
| Line 1 |  | 00    | 01 | 02 | 03 | 04 | ~  | 12 | 13                 | ← DD RAM<br>address (hexadecimal) |
| Line 2 |  | 40    | 41 | 42 | 43 | 44 | ~  | 52 | 53                 |                                   |

Note:

The DDRAM address at digit 20 in the first line is not consecutive to the DDRAM address at digit 1 in the second line.

When the display is shifted by instruction, the relationship between the LCD display and the DDRAM address changes as shown below:

(Display shifted to the right)

|        |  | Digit |    |    |    |    |    |    |    |  |
|--------|--|-------|----|----|----|----|----|----|----|--|
|        |  | 1     | 2  | 3  | 4  | 5  | 19 | 20 |    |  |
| Line 1 |  | 27    | 00 | 01 | 02 | 03 | ~  | 11 | 12 |  |
| Line 2 |  | 67    | 40 | 41 | 42 | 43 | ~  | 51 | 52 |  |

(Display shifted to the left)

|        |  | Digit |    |    |    |    |    |    |    |  |
|--------|--|-------|----|----|----|----|----|----|----|--|
|        |  | 1     | 2  | 3  | 4  | 5  | 19 | 20 |    |  |
| Line 1 |  | 01    | 02 | 03 | 04 | 05 | ~  | 13 | 14 |  |
| Line 2 |  | 41    | 42 | 43 | 44 | 45 | ~  | 53 | 54 |  |

**Character Generator ROM (CGROM)**

The CGROM generates small character patterns ( $5 \times 7$  dots, 160 patterns) or large character patterns ( $5 \times 10$  dots, 32 patterns) from the 8-bit character code signals in the DDRAM. See Table 2 for the relationship between the 8-bit character codes and the character patterns.

When the 8-bit character code corresponding to a character pattern in the CGROM is written in the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address.

## Character Generator RAM (CGRAM)

The CGRAM is used to generate user-specific character patterns that are not in the CGROM. CGRAM (64 bytes = 512 bits) can store up to 8 small character patterns (5 × 8 dots) or up to 4 large character patterns (5 × 11 dots).

When displaying a character pattern stored in the CGRAM, write an 8-bit character code (00 to 07 or 08 to 0F; hex.) assigned in Table 2 to the DDRAM. This enables outputting the character pattern to the LCD display position corresponding to the DDRAM address.

The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.

The following describes how character patterns are written in and read from the CGRAM.

### 1) Small character patterns (5 × 8 dots) (See Table 3-1.)

#### (1) A method of writing character patterns to the CGRAM from the CPU

The three CGRAM address bits 0 to 2 select one of the lines constituting a character pattern. First, set the mode to increment or decrement from the CPU, and then input the CGRAM address. Write each line of the character pattern code in the CGRAM through DB<sub>0</sub> to DB<sub>7</sub>.

The data lines DB<sub>0</sub> to DB<sub>7</sub> correspond to the CGRAM data bits 0 to 7, respectively (see Table 3.1). Input data "1" represents the ON status of an LCD dot and "0" represents the OFF status. Since the ADC is automatically incremented or decremented by 1 after the data is written to the CGRAM, it is not necessary to set the CGRAM address again.

The bottom line of a character pattern (the CGRAM address bits 0 to 2 are all "1", which means 7 in hexadecimal) is the cursor line. The ON/OFF pattern of this line is ORed with the cursor pattern for displaying on the LCD. Therefore, the pattern data for the cursor position should be all zeros to display the cursor.

Whereas the data given by the CGRAM data bits 0 to 4 is output to the LCD as display data, the data given by the CGRAM data bits 5 to 7 is not. Therefore, the CGRAM data bits 5 to 7 can be used as a RAM area.

#### (2) A method of displaying CGRAM character patterns on the LCD

The CGRAM is selected when the higher-order 4 bits of a character code are all zeros. Since bit 3 of a character code is not used, the character pattern "0" in Table 3-1 can be selected using the character code "00" or "08" in hexadecimal.

When the 8-bit character code corresponding to a character pattern in the CGRAM is written to the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address. (The DDRAM data bits 0 to 2 correspond to the CGRAM address bits 3 to 5, respectively.)

## 2) Large character patterns (5 × 11 dots) (See Table 3–2.)

### (1) A method of writing character patterns to the CGRAM from the CPU

The four CGRAM address bits 0 to 3 select one of the lines constituting a character pattern. First, set the mode to increment or decrement from the CPU, and then input the CGRAM address. Write each line of the character pattern code in the CGRAM through DB<sub>0</sub> to DB<sub>7</sub>.

The data lines DB<sub>0</sub> to DB<sub>7</sub> correspond to the CGRAM data bits 0 to 7, respectively (see Table 3–2). Input data “1” represents the ON status of an LCD dot and “0” represents the OFF status. Since the ADC is automatically incremented or decremented by 1 after the data is written to the CGRAM, it is not necessary to set the CGRAM address again.

The bottom line of a character pattern (the CGRAM address bits 0 to 3 are all “1”, which means A in hexadecimal) is a cursor line. The ON/OFF pattern of this line is ORed with the cursor pattern for displaying on the LCD. Therefore, the pattern data for the cursor position should be all zeros to display the cursor.

Whereas the data given by the CGRAM data bits 0 to 4 with the CGRAM addresses 0 to A in hexadecimal (set by the CGRAM address bits 0 to 3) is output as display data to the LCD, the data given by the CGRAM data bits 5 to 7 or the CGRAM addresses B to F in hexadecimal is not. These bits can be written and read as a RAM area.

### (2) A method of displaying CGRAM character patterns on the LCD

The CGRAM is selected when the higher-order 4 bits of a character code are all zeros. Since bits 0 and 3 of a character code are not used, the character pattern “β” in Table 3–2 can be selected with a character code “00”, “01”, “08” or “09” in hexadecimal.

When the 8-bit character code corresponding to a character pattern in the CGRAM is written to the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address. (The DDRAM data bits 1 and 2 correspond to the CGRAM address bits 4 and 5, respectively.)

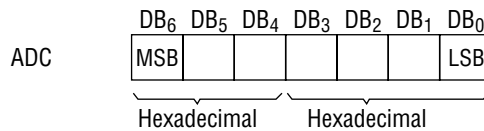
**Arbitrator RAM (ABRAM)**

The arbitrator RAM(ABRAM) stores arbitrator display data.

The ABRAM address is set at the ADC with the relationship illustrated below. Its valid address area is 00 to 19 (00H to 13H).

Although an address exceeding 19 (13H) can be set or the address already set may exceed it due to automatic increment or decrement processing, any address out of the valid address area is ignored.

The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.



The arbitrator RAM can store a maximum of 100 dots of the arbitrator Display-ON data in units of 5 dots.

The arbitrator display is not shifted by any instructions and has the following relationship with the LCD display positions:.

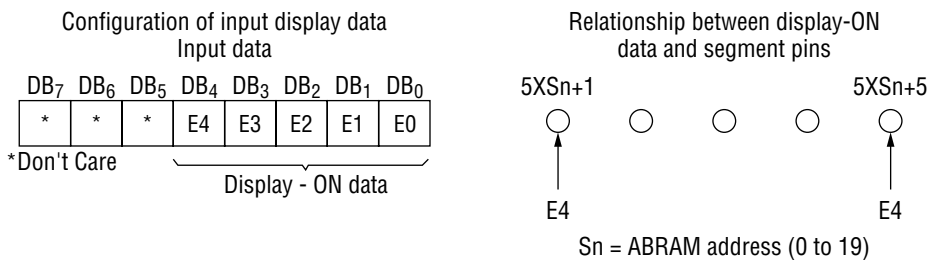


Table 2 Relationship between character codes and character patterns of the ML9041

| Lower 4 bits | Upper 4 bits | MSB 0000   | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |   |   |   |   |   |   |   |   |    |    |   |   |
|--------------|--------------|------------|------|------|------|------|------|------|------|------|------|------|------|------|---|---|---|---|---|---|---|---|----|----|---|---|
|              |              | CG RAM (1) |      |      |      |      |      |      |      |      |      |      |      |      |   |   |   |   |   |   |   |   |    |    |   |   |
| 0000         | LSB          |            |      | 0    | 0    | @    | @    | P    | P    | \    | `    | p    | P    |      |   | - | - | タ | タ | ミ | ミ | α | α  | P  | P |   |
| 0001         |              | (2)        | !    | !    | 1    | 1    | A    | A    | Q    | Q    | a    | a    | q    | q    | 。 | 。 | ア | ア | チ | チ | ム | ム | ä  | ä  | q | q |
| 0010         |              | (3)        | "    | "    | 2    | 2    | B    | B    | R    | R    | b    | b    | r    | r    | 「 | 「 | イ | イ | ツ | ツ | メ | メ | β  | β  | θ | θ |
| 0011         |              | (4)        | #    | #    | 3    | 3    | C    | C    | S    | S    | c    | c    | s    | s    | 」 | 」 | ウ | ウ | テ | テ | モ | モ | ε  | ε  | ∞ | ∞ |
| 0100         |              | (5)        | \$   | \$   | 4    | 4    | D    | D    | T    | T    | d    | d    | t    | t    | 、 | 、 | エ | エ | ト | ト | ヤ | ヤ | μ  | μ  | Ω | Ω |
| 0101         |              | (6)        | %    | %    | 5    | 5    | E    | E    | U    | U    | e    | e    | u    | u    | ・ | ・ | オ | オ | ナ | ナ | ユ | ユ | σ  | σ  | ü | ü |
| 0110         |              | (7)        | &    | &    | 6    | 6    | F    | F    | V    | V    | f    | f    | v    | v    | ヲ | ヲ | カ | カ | ニ | ニ | ヨ | ヨ | ρ  | ρ  | Σ | Σ |
| 0111         |              | (8)        | '    | '    | 7    | 7    | G    | G    | W    | W    | g    | g    | w    | w    | ア | ア | キ | キ | ヌ | ヌ | ラ | ラ | g  | g  | π | π |
| 1000         |              | (1)        | (    | (    | 8    | 8    | H    | H    | X    | X    | h    | h    | x    | x    | イ | イ | ク | ク | ネ | ネ | リ | リ | √  | √  | ∞ | ∞ |
| 1001         |              | (2)        | )    | )    | 9    | 9    | I    | I    | Y    | Y    | i    | i    | y    | y    | ウ | ウ | ケ | ケ | ノ | ノ | ル | ル | -1 | -1 | y | y |
| 1010         |              | (3)        | *    | *    | :    | :    | J    | J    | Z    | Z    | j    | j    | z    | z    | エ | エ | コ | コ | ハ | ハ | レ | レ | j  | j  | 千 | 千 |
| 1011         |              | (4)        | +    | +    | ;    | ;    | K    | K    | [    | [    | k    | k    | {    | {    | オ | オ | サ | サ | ヒ | ヒ | ロ | ロ | x  | x  | 万 | 万 |
| 1100         |              | (5)        | ,    | ,    | <    | <    | L    | L    | ¥    | ¥    | l    | l    |      |      | ヤ | ヤ | シ | シ | フ | フ | ワ | ワ | ¢  | ¢  | 円 | 円 |
| 1101         |              | (9)        | -    | -    | =    | =    | M    | M    | ]    | ]    | m    | m    | }    | }    | ユ | ユ | ス | ス | ヘ | ヘ | ン | ン | £  | £  | ÷ | ÷ |
| 1110         |              | (7)        | .    | .    | >    | >    | N    | N    | ^    | ^    | n    | n    | →    | →    | ヨ | ヨ | セ | セ | ホ | ホ | シ | シ | ñ  | ñ  |   |   |
| 1111         |              | (8)        | /    | /    | ?    | ?    | O    | O    | _    | _    | o    | o    | ←    | ←    | ッ | ッ | ソ | ソ | マ | マ | ワ | ワ | ö  | ö  | ■ | ■ |

Table 3-1 Relationship between CGRAM address bits, CGRAM data bits (character pattern) and DDRAM data bits (character code) in 5 × 7 dot character mode. (Examples)

| CG RAM address |   | CG RAM data (Character pattern) |   |     |     | DD RAM data (Character code) |   |   |     |     |   |   |                 |     |
|----------------|---|---------------------------------|---|-----|-----|------------------------------|---|---|-----|-----|---|---|-----------------|-----|
| 5              | 4 | 3                               | 2 | 1   | 7   | 6                            | 5 | 4 | 3   | 2   | 1 | 0 |                 |     |
| MSB            |   |                                 |   | LSB | MSB |                              |   |   | LSB | MSB |   |   |                 | LSB |
| 0              | 0 | 0                               | 0 | 0   | ×   | ×                            | × | 0 | 1   | 1   | 1 | 0 | 0 0 0 0 × 0 0 0 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
| 0              | 0 | 1                               | 0 | 0   | ×   | ×                            | × | 1 | 0   | 0   | 0 | 1 | 0 0 0 0 × 0 0 1 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
| 1              | 1 | 1                               | 0 | 0   | ×   | ×                            | × | 0 | 1   | 1   | 1 | 0 | 0 0 0 0 × 1 1 1 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |
|                |   |                                 |   |     |     |                              |   |   |     |     |   |   |                 |     |

×: Don't Care

Table 3-2 Relationship between CGRAM address bits, CGRAM data bits (character pattern) and DDRAM data bits (character code) in 5 × 10 dot character mode (Examples)

| CG RAM address |   |     |   |   | CG RAM data (Character pattern) |   |     |   |   | DD RAM data (Character code) |   |     |   |                 |   |   |   |   |   |   |   |
|----------------|---|-----|---|---|---------------------------------|---|-----|---|---|------------------------------|---|-----|---|-----------------|---|---|---|---|---|---|---|
| 5              | 4 | 3   | 2 | 1 | 0                               | 7 | 6   | 5 | 4 | 3                            | 2 | 1   | 0 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSB            |   | LSB |   |   | MSB                             |   | LSB |   |   | MSB                          |   | LSB |   |                 |   |   |   |   |   |   |   |
| 0              | 0 | 0   | 0 | 0 | 0                               | × | ×   | × | 0 | 1                            | 0 | 0   | 0 | 0 0 0 0 × 0 0 × |   |   |   |   |   |   |   |
|                | 0 | 0   | 0 | 1 |                                 |   |     |   | 0 | 1                            | 1 | 1   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 0   | 1 | 0 |                                 |   |     |   | 1 | 0                            | 0 | 1   | 0 |                 |   |   |   |   |   |   |   |
|                | 0 | 0   | 1 | 1 |                                 |   |     |   | 0 | 1                            | 1 | 1   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 0 | 0 |                                 |   |     |   | 0 | 1                            | 0 | 1   | 0 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 0 | 1 |                                 |   |     |   | 1 | 1                            | 1 | 1   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 1 | 0 |                                 |   |     |   | 0 | 0                            | 0 | 1   | 0 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 1 | 1 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 0 | 0 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 0 | 1 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 1 | 0 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 1 | 1 |                                 |   |     |   | × | ×                            | × | ×   | × |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 0 | 0 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 0 | 1 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 1 | 0 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 1 | 1 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
| 0              | 0 | 0   | 0 | 0 | 0                               | × | ×   | × | 0 | 0                            | 0 | 0   | 0 | 0 0 0 0 × 0 0 × |   |   |   |   |   |   |   |
|                | 0 | 0   | 0 | 1 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 0 | 0   | 1 | 0 |                                 |   |     |   | 0 | 1                            | 1 | 1   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 0   | 1 | 1 |                                 |   |     |   | 1 | 0                            | 0 | 0   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 0 | 0 |                                 |   |     |   | 1 | 0                            | 0 | 0   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 0 | 1 |                                 |   |     |   | 1 | 0                            | 0 | 0   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 1 | 0 |                                 |   |     |   | 0 | 1                            | 1 | 1   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 1 | 1 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 1 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 0 | 0 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 1 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 0 | 1 |                                 |   |     |   | 0 | 1                            | 1 | 1   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 1 | 0 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 1 | 1 |                                 |   |     |   | × | ×                            | × | ×   | × |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 0 | 0 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 0 | 1 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 1 | 0 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 1 | 1 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
| 0              | 0 | 0   | 0 | 0 | 0                               | × | ×   | × | 0 | 0                            | 0 | 0   | 0 | 0 0 0 0 × 1 1 × |   |   |   |   |   |   |   |
|                | 0 | 0   | 0 | 1 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 0 | 0   | 1 | 0 |                                 |   |     |   | 1 | 1                            | 0 | 1   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 0   | 1 | 1 |                                 |   |     |   | 0 | 1                            | 0 | 1   | 0 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 0 | 0 |                                 |   |     |   | 1 | 0                            | 0 | 0   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 0 | 1 |                                 |   |     |   | 1 | 0                            | 0 | 0   | 1 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 1 | 0 |                                 |   |     |   | 0 | 1                            | 1 | 1   | 0 |                 |   |   |   |   |   |   |   |
|                | 0 | 1   | 1 | 1 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 0 | 0 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 0 | 1 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 1 | 0 |                                 |   |     |   | 0 | 0                            | 0 | 0   | 0 |                 |   |   |   |   |   |   |   |
|                | 1 | 0   | 1 | 1 |                                 |   |     |   | × | ×                            | × | ×   | × |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 0 | 0 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 0 | 1 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 1 | 0 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |
|                | 1 | 1   | 1 | 1 |                                 |   |     |   |   |                              |   |     |   |                 |   |   |   |   |   |   |   |

×: Don't Care

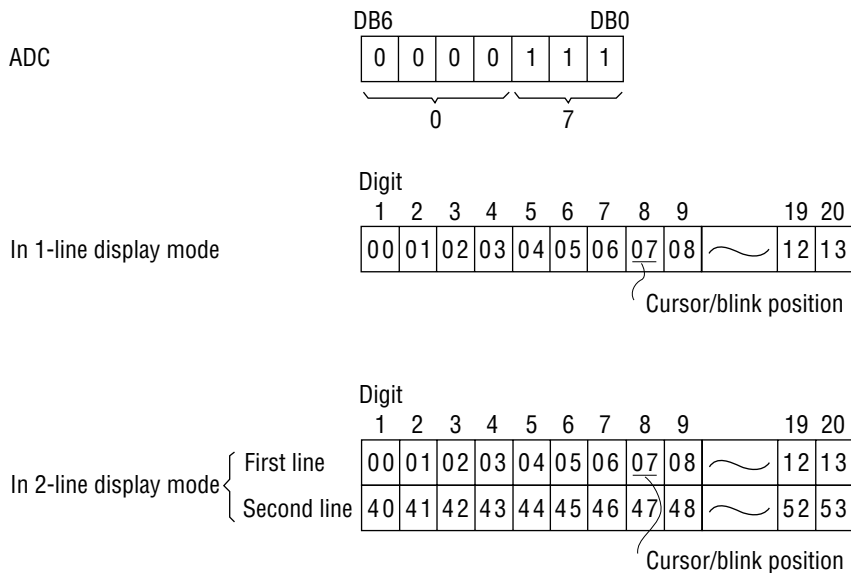
**Cursor/Blink Control Circuit**

This circuit generates the cursor and blink of the LCD.

The operation of this circuit is controlled by the program of the CPU.

The cursor/blink display is carried out in the position corresponding to the DDRAM address set in the ADC (Address Counter).

For example, when the ADC stores a value of "07" (hexadecimal), the cursor or blink is displayed as follows:



**Note:** The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.

### LCD Display Circuit (COM1 to COM17, SEG1 to SEG100, SSR and CSR)

The ML9041 has 17 common signal outputs and 100 segment signal outputs to display 20 characters (in the 1-line display mode) or 40 characters (in the 2-line display mode).

The character pattern is converted into serial data and transferred in series through the shift register.

The transfer direction of serial data is determined by the SSR pin. The shift direction of common signals is determined by the CSR pin. The following tables show the transfer and shift directions:

| SSR | Transfer direction                    |  |  |  |
|-----|---------------------------------------|--|--|--|
| L   | SEG <sub>1</sub> → SEG <sub>100</sub> |  |  |  |
| H   | SEG <sub>100</sub> → SEG <sub>1</sub> |  |  |  |

| CSR | duty | AS bit | Shift direction     | arbitrator's common pin |
|-----|------|--------|---------------------|-------------------------|
| L   | 1/9  | L      | COM1 → COM9         | COM9                    |
| L   | 1/9  | H      | COM2 → COM9, COM1   | COM1                    |
| L   | 1/12 | L      | COM1 → COM12        | COM12                   |
| L   | 1/12 | H      | COM2 → COM12, COM1  | COM1                    |
| L   | 1/17 | L      | COM1 → COM17        | COM17                   |
| L   | 1/17 | H      | COM2 → COM17, COM1  | COM1                    |
| H   | 1/9  | L      | COM9 → COM1         | COM1                    |
| H   | 1/9  | H      | COM8 → COM1, COM9   | COM9                    |
| H   | 1/12 | L      | COM12 → COM1        | COM1                    |
| H   | 1/12 | H      | COM11 → COM1, COM12 | COM12                   |
| H   | 1/17 | L      | COM17 → COM1        | COM1                    |
| H   | 1/17 | H      | COM16 → COM1, COM17 | COM17                   |

\* Refer to the Expansion Instruction Codes section about the AS bit.

Signals to be input to the SSR and CSR pins should be determined at power-on and be kept unchanged.

### Built-in Reset Circuit

The ML9041 is automatically initialized when the power is turned on.

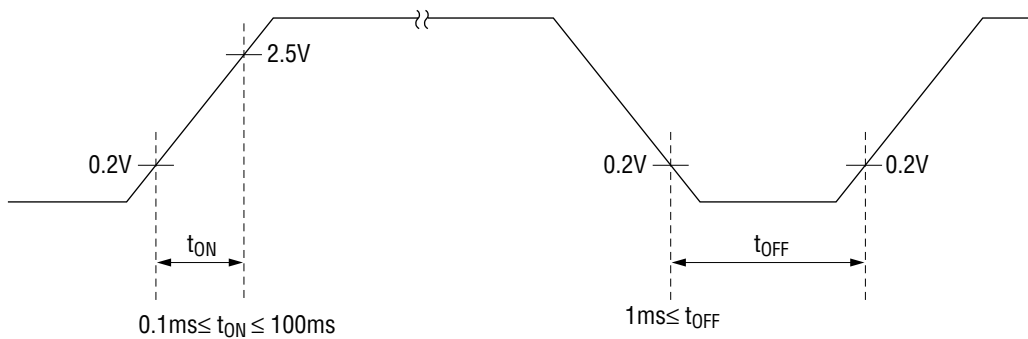
During initialization, the Busy Flag (BF) is "1" and the ML9041 does not accept any instruction from the CPU (other than the Read BF instruction).

The Busy Flag is "1" for about 15 ms after the  $V_{DD}$  becomes 2.5 V or higher.

During this initialization, the ML9041 performs the following instructions:

- 1) Display clearing
- 2) CPU interface data length = 8 bits (DL = "1")
- 3) 1-line LCD display (N = "0")
- 4) Font size =  $5 \times 7$  dots (F = "0")
- 5) ADC counting = Increment (I/D = "1")
- 6) Display shifting = None (S = "0")
- 7) Display = Off (D = "0")
- 8) Cursor = Off (C = "0")
- 9) Blinking = Off (B = "0")
- 10) Arbitrator = Displayed in the lower line (AS = "0")
- 11) Setting 1FH (hexadecimal) to the Contrast Data

To use the built-in reset circuit, the power supply conditions shown below should be satisfied. Otherwise, the built-in reset circuit may not work properly. In such a case, initialize the ML9041 with the instructions from the CPU. The use of a battery always requires such initialization from the CPU. (See "Initial Setting of Instructions")



**Figure 1 Power-on and Power-off Waveform**

## I/F with CPU

### Parallel interface mode

The ML9041 can transfer either 8 bits once or 4 bits twice on the data bus for interfacing with any 8-bit or 4-bit microcontroller (CPU).

#### 1) 8-bit interface data length

The ML9041 uses all of the 8 data bus lines DB0 to DB7 at a time to transfer data to and from the CPU.

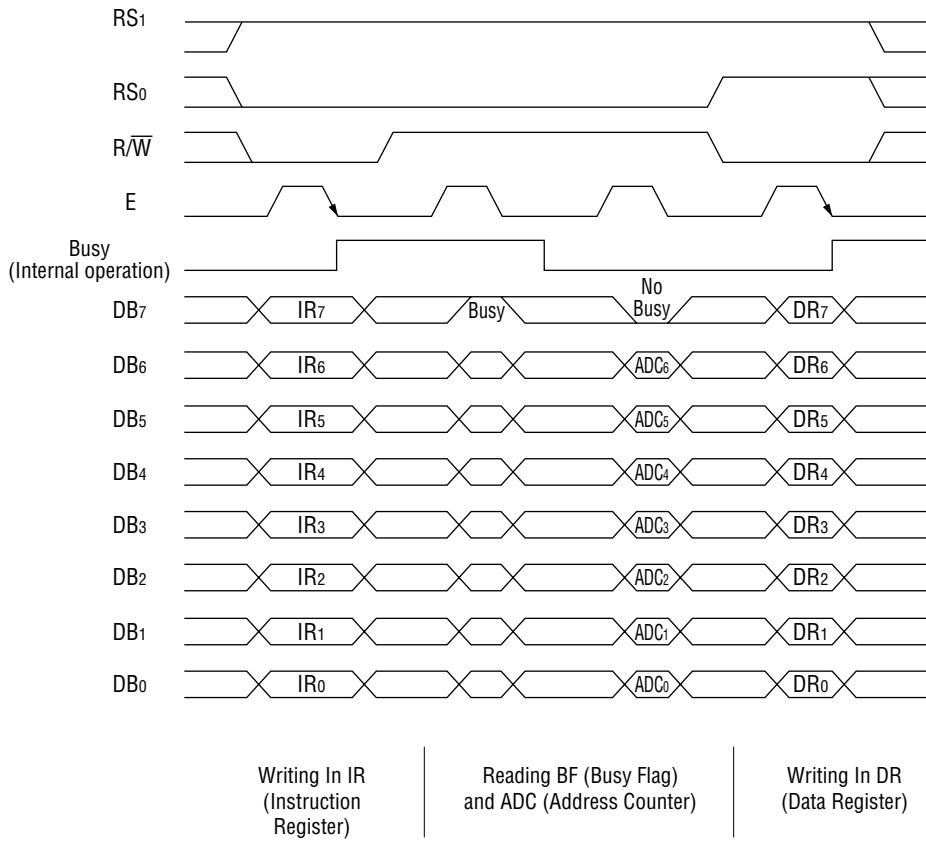
#### 2) 4-bit interface data length

The ML9041 uses only the higher-order 4 data bus lines DB<sub>4</sub> to DB<sub>7</sub> twice to transfer 8-bit data to and from the CPU.

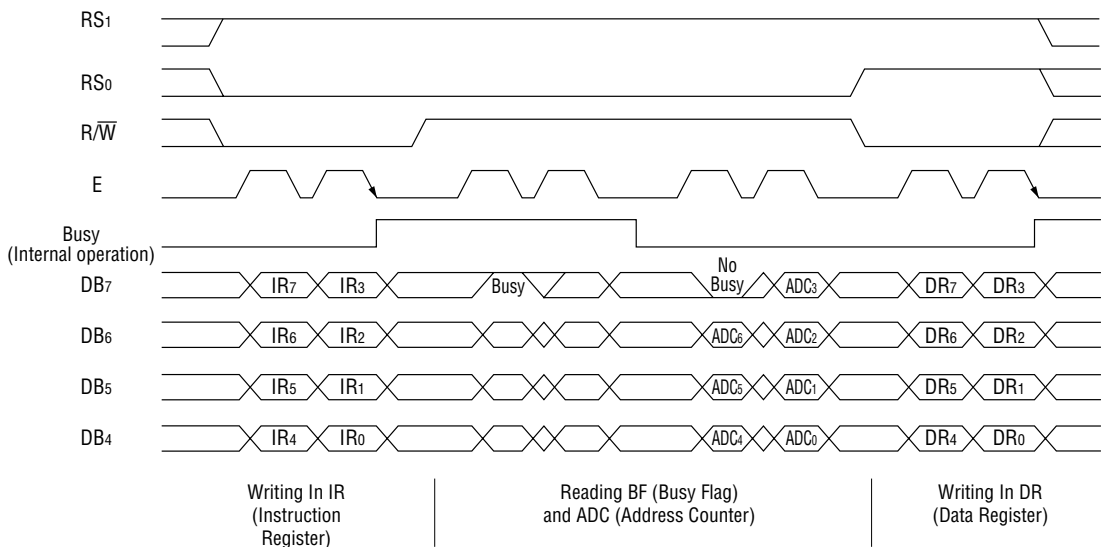
The ML9041 first transfers the higher-order 4 bits of 8-bit data (DB<sub>4</sub> to DB<sub>7</sub> in the case of 8-bit interface data length) and then the lower-order 4 bits of the data (DB<sub>0</sub> to DB<sub>3</sub> in the case of 8-bit interface data length).

The lower-order 4 bits of data should always be transferred even when only the transfer of the higher-order 4 bits of data is required. (Example: Reading the Busy Flag)

Two transfers of 4 bits of data complete the transfer of a set of 8-bit data. Therefore, when only one access is made, the following data transfer cannot be completed properly.



**Figure 2 8-Bit Data Transfer**



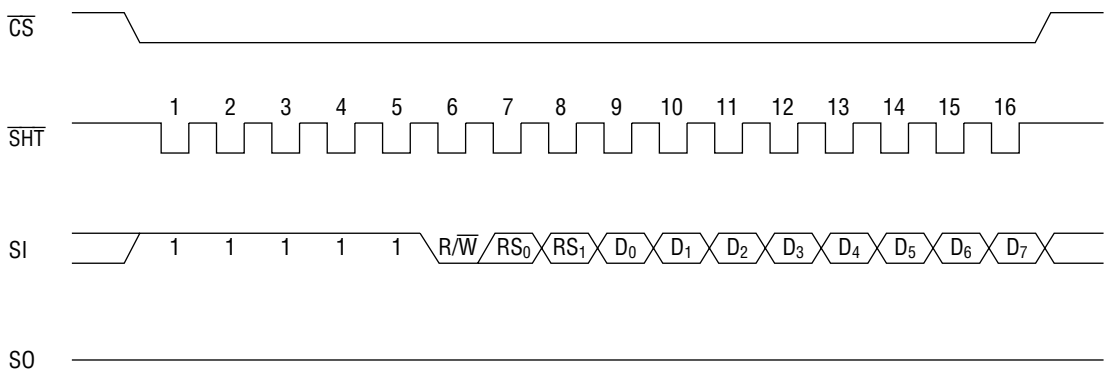
**Figure 3 4-Bit Data Transfer**

**Serial Interface Mode**

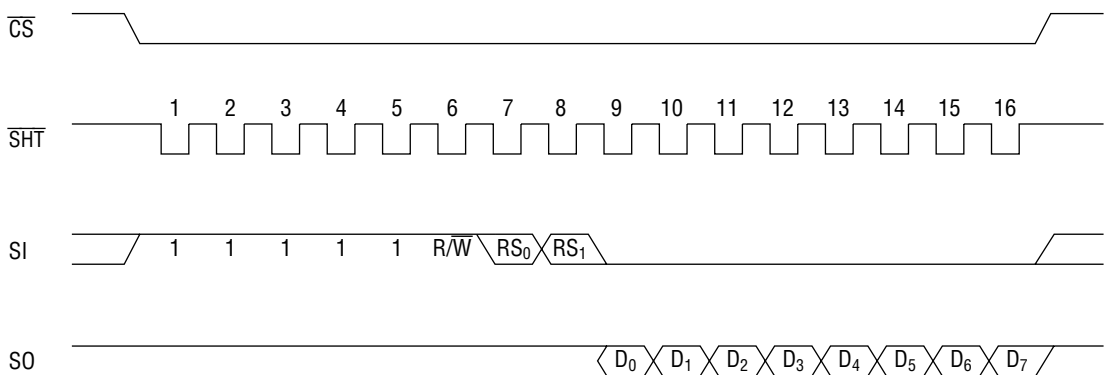
In the Serial I/F Mode, the ML9041 interfaces with the CPU via the  $\overline{CS}$ ,  $\overline{SHT}$ , SI and SO pins. Writing and reading operations are executed in units of 16 bits after the  $\overline{CS}$  signal falls down. If the  $\overline{CS}$  signal rises up before the completion of 16-bit unit access, this access is ignored. When the BF bit is "1", the ML9041 cannot accept any other instructions. Before inputting a new instruction, check that the BF bit is "0". Any access when the BF bit is "1" is ignored. Data format is LSB-first.

Examples of Access in the Serial I/F Mode

1) WRITE MODE



2) READ MODE



Instruction Codes

Table of Instruction Codes

| Instruction                 | Code  |     |     |  |     |     |   |     |     |  |   | Function  | Execution Time<br>f = 270kHz  |         |  |
|-----------------------------|---|-----|-----|--|-----|-----|---|-----|-----|--|---|---|---|---------|--|
|                             | RS1   | RS0 | R/W | DB7  | DB6 | DB5 | DB4   | DB3 | DB2 | DB1                                    | DB0   |   |   |         |  |
| Display Clear               | 1   | 0   | 0   | 0  | 0   | 0   | 0   | 0   | 0   | 0                                      | 1   |   | Clears all the displayed digits of the LCD and sets the DDRAM address 0 in the address counter. The arbitrator data is cleared.   | 1.52 ms |  |
| Cursor Home                 | 1   | 0   | 0   | 0  | 0   | 0   | 0   | 0   | 0   | 0                                      | 1   | *   | Sets the DDRAM address 0 in the address counter and shifts the display back to the original. The content of the DDRAM remains unchanged.  | 1.52 ms |  |
| Entry Mode Setting          | 1   | 0   | 0   | 0  | 0   | 0   | 0   | 0   | 0   | 1                                      | I/D   | S   | Determines the direction of movement of the cursor and whether or not to shift the display. This instruction is executed when data is written or read.  | 37 μs   |  |
| Display ON/OFF Control      | 1   | 0   | 0   | 0  | 0   | 0   | 0   | 0   | 1   | D                                      | C   | B   | Sets LCD display ON/OFF (D), cursor ON/OFF or cursor-position character blinking ON/OFF.  | 37 μs   |  |
| Cursor/Display Shift        | 1   | 0   | 0   | 0  | 0   | 0   | 1   | S/C | R/L | *                                      | *   |   | Moves the cursor or shifts the display without changing the content of the DDRAM.   | 37 μs   |  |
| Function Setting            | 1   | 0   | 0   | 0  | 0   | 1   | DL  | N   | F   | *                                      | *   |   | Sets the interface data length (DL), the number of display lines (N) or the type of character font (F).   | 37 μs   |  |
| CGRAM Address Setting       | 1   | 0   | 0   | 0  | 1   | ACG |   |     |     |  |   | Sets on CGRAM address. After that, CGRAM data is transferred to and from the CPU. | 37 μs   |         |  |
| DDRAM Address Setting       | 1   | 0   | 0   | 1  | ADD |     |   |     |     |  | Sets a DDRAM address. After that DDRAM data is transferred to and from the CPU.                       | 37 μs   |   |         |  |
| Busy Flag/Address Read      | 1   | 0   | 1   | BF   | ADC |     |   |     |     |  | Reads the Busy Flag (indicating that the ML9041 is operating) and the content of the address counter. | 0 μs  |   |         |  |
| RAM Data Write              | 1   | 1   | 0   | WRITE DATA   |     |     |   |     |     | Writes data in DDRAM, ABRAM or CGRAM.  | 37 μs   |   |   |         |  |
| RAM Data Read               | 1   | 1   | 1   | READ DATA  |     |     |   |     |     | Reads data from DDRAM, ABRAM or CGRAM. | 37 μs   |   |   |         |  |
| Arbitrator Display Line Set | 0   | 0   | 0   | 0  | 0   | 0   | 0   | 0   | 0   | 1                                      | AS  |   | Sets the arbitrator display line.   | 37 μs   |  |
| Contrast Control Data Write | 0   | 0   | 0   | 0  | 0   | 1   | WRITE (Contrast Data) DATA  |     |     |  |   |   | Writes data to control the contrast of the LCD.   | 37 μs   |  |
| Contrast Control Data Read  | 0   | 0   | 1   | 0  | 0   | 0   | READ (Contrast Data) DATA   |     |     |  |   |   | Reads data to control the contrast of the LCD.  | 37 μs   |  |
| ABRAM address setting       | 0   | 0   | 0   | 0  | 1   | 1   | AAB   |     |     |  |   |   | Sets an ABRAM address. After that ABRAM data is transferred to and from the CPU.  | 37 μs   |  |
| —                           | I/D = "1" (Increment)<br>S = "1" (Shifts the display.)<br>S/C = "1" (Shifts display.)<br>R/L = "1" (Right shift)<br>D/L = "1" (8-bit data)<br>N = "1" (2 lines)<br>F = "1" (5 × 10 dots)<br>BF = "1" (Busy) |     |     | I/D = "0" (Decrement)<br>S/C = "0" (Moves the cursor.)<br>R/L = "0" (Left shift)<br>DL = "0" (4-bit data)<br>N = "0" (1 line)<br>F = "0" (5 × 7 dots)<br>BF = "0" (Ready to accept an instruction) |     |     | B = "1" (Enables blinking.)<br>C = "1" (Displays the cursor.)<br>D = "1" (Displays a character pattern.)<br>AS = "1" (Arbitrator Displays arbitrator on the upper line) |     |     |  |   |   | DD RAM : Display data RAM<br>CG RAM : Character generator RAM<br>ABRAM : Arbitrator data RAM<br>ACG : CGRAM address<br>ADD : DDRAM address (Corresponds to the cursor address)<br>AAB : ABRAM address<br>ADC : Address counter (Used by DDRAM, ABRAM and CGRAM) |         | The execution time is dependent upon frequencies |

×: Don't Care

**Instruction Codes**

An instruction code is a signal sent from the CPU to access the ML9041. The ML9041 starts operation as instructed by the code received. The busy status of the ML9041 is rather longer than the cycle time of the CPU, since the internal processing of the ML9041 starts at a timing which does not affect the display on the LCD. In the busy status (Busy Flag is "1"), the ML9041 executes the Busy Flag Read instruction only. Therefore, the CPU should ensure that the Busy Flag is "0" before sending an instruction code to the ML9041.

1) Display Clear

|                    | RS <sub>1</sub> | RS <sub>0</sub> | R/W | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|--------------------|-----------------|-----------------|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction Code : | 1               | 0               | 0   | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               |

When this instruction is executed, the LCD display including arbitrator display is cleared and the I/D entry mode is set to "Increment". The value of "S" (Display shifting) remains unchanged. The position of the cursor or blink being displayed moves to the left end of the LCD (or the left end of the line 1 in the 2-line display mode).

Note: All DDRAM and ABRAM data turn to "20" and "00" in hexadecimal, respectively. The value of the address counter (ADC) turns to the one corresponding to the address "00" (hexadecimal) of the DDRAM.

The execution time of this instruction is 1.52 ms (maximum) at an oscillation frequency of 270 kHz.

2) Cursor Home

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R/W | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 0               | 0   | 0               | 0               | 0               | 0               | 0               | 0               | 1               | ×               |

×: Don't Care

When this instruction is executed, the cursor or blink position moves to the left end of the LCD (or the left end of line 1 in the 2-line display mode). If the display has been shifted, the display returns to the original display position before shifting.

Note: The value of the address counter (ADC) goes to the one corresponding to the address "00" (hexadecimal) of the DDRAM.

The execution time of this instruction is 1.52 ms (maximum) at an oscillation frequency of 270 kHz.

3) Entry Mode Setting

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 0               | 0           | 0               | 0               | 0               | 0               | 0               | 1               | I/D             | S               |

(1) When the I/D is set, the cursor or blink shifts to the right by 1 character position (I/D = "1"; increment) or to the left by 1 character position (I/D = "0"; decrement) after an 8-bit character code is written to or read from the DDRAM. At the same time, the address counter (ADC) is also incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement). After a character pattern code is written to or read from the CGRAM, the address counter (ADC) is incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement).

Also after data is written to or read from the ABRAM, the address counter (ADC) is incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement).

(2) When S = "1", the cursor or blink stops and the entire display shifts to the left (I/D = "1") or to the right (I/D = "0") by 1 character position after a character code is written to the DDRAM. In the case of S = "1", when a character code is read from the DDRAM, when a character pattern data is written to or read from the CGRAM or when data is written to or read from the ABRAM, normal read/write is carried out without shifting of the entire display. (The entire display does not shift, but the cursor or blink shifts to the right (I/D = "1") or to the left (I/D = "0") by 1 character position.)

When S = "0", the display does not shift, but normal write/read is performed.

Note: The execution time of this instruction is 37 μs (maximum) at an oscillation frequency of 270 kHz.

4) Display Mode Setting

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 0               | 0           | 0               | 0               | 0               | 0               | 1               | D               | C               | B               |

(1) The "D" bit (DB2) of this instruction determines whether or not to display character patterns on the LCD.

When the "D" bit is "1", character patterns are displayed on the LCD.

When the "D" bit is "0", character patterns are not displayed on the LCD and the cursor/blink setting is also canceled.

Note: Unlike the Display Clear instruction, this instruction does not change the character code in the DDRAM and ABRAM.

(2) When the "C" bit (DB1) is "0", the cursor turns off. When both the "C" and "D" bits are "1", the cursor turns on.

(3) When the "B" bit (DB0) is "0", blinking is canceled. When both the "B" and "D" bits are "1", blinking is performed.

In the Blinking mode, all dots including those of the cursor, the character pattern and the cursor are alternately displayed.

Note: The execution time of this instruction is 37 μs (maximum) at an oscillation frequency of 270kHz.

5) Cursor/Display Shift

|                   |                 |                 |              |                 |                 |                 |                 |                 |                 |                 |                 |
|-------------------|-----------------|-----------------|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|                   | RS <sub>1</sub> | RS <sub>0</sub> | R/ $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
| Instruction code: | 1               | 0               | 0            | 0               | 0               | 0               | 1               | S/C             | R/L             | ×               | ×               |

×: FDon't Care

S/C = "0", R/L = "0" This instruction shifts left the cursor and blink positions by 1 (decrements the content of the ADC by 1).

S/C = "0", R/L = "1" This instruction shifts right the cursor and blink positions by 1 (increments the content of the ADC by 1).

S/C = "1", R/L = "0" This instruction shifts left the entire display by 1 character position. The cursor and blink positions move to the left together with the entire display. The Arbitrator display is not shifted. (The content of the ADC remains unchanged.)

S/C = "1", R/L = "1" This instruction shifts right the entire display by 1 character position. The cursor and blink positions move to the right together with the entire display. The Arbitrator display is not shifted. (The content of the ADC remains unchanged.)

In the 2-line mode, the cursor or blink moves from the first line to the second line when the cursor at digit 40 (27; hex) of the first line is shifted right.

When the entire display is shifted, the character pattern, cursor or blink will not move between the lines (from line 1 to line 2 or vice versa).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

6) Function Setting

|                   |                 |                 |              |                 |                 |                 |                 |                 |                 |                 |                 |
|-------------------|-----------------|-----------------|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|                   | RS <sub>1</sub> | RS <sub>0</sub> | R/ $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
| Instruction code: | 1               | 0               | 0            | 0               | 0               | 1               | DL              | N               | F               | ×               | ×               |

×: Don't Care

(1) When the "DL" bit (DB4) of this instruction is "1", the data transfer to and from the CPU is performed once by the use of 8 bits DB<sub>7</sub> to DB<sub>0</sub>.

When the "DL" bit (DB4) of this instruction is "0", the data transfer to and from the CPU is performed twice by the use of 4 bits DB<sub>7</sub> to DB<sub>4</sub>.

(2) The 2-line display mode is selected when the "N" bit (DB3) of this instruction is "1". The 1-line display mode is selected when the "N" bit is "0".

(3) The character font represented by 5 × 7 dots is selected when the "F" bit (DB2) of this instruction is "1". The character font represented by 5 × 10 dots is selected when the "F" bit is "1" and the "N" bit is "0".

After the ML9041 is powered on, this initial setting should be carried out before execution of any instruction except the Busy Flag Read. After this initial setting, no instructions other than the DL Set instruction can be executed. In the Serial I/F Mode, DL setting is ignored.

| N | F | Number of display lines | Font size | Duty | Number of biases | Number of common signals |
|---|---|-------------------------|-----------|------|------------------|--------------------------|
| 0 | 0 | 1                       | 5×7       | 1/9  | 4                | 9                        |
| 0 | 1 | 1                       | 5×10      | 1/12 | 4                | 12                       |
| 1 | 0 | 2                       | 5×7       | 1/17 | 5                | 17                       |
| 1 | 1 | 2                       | 5×7       | 1/17 | 5                | 17                       |

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

7) CGRAM Address Setting

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R $\overline{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 0               | 0                | 0               | 1               | C <sub>5</sub>  | C <sub>4</sub>  | C <sub>3</sub>  | C <sub>2</sub>  | C <sub>1</sub>  | C <sub>0</sub>  |

This instruction sets the character data corresponding to the CGRAM address represented by the bits C5 to C0 (binary).

The CGRAM addresses are valid until DDRAM or ABRAM addresses are set.

The CPU writes or reads character patterns starting from the one represented by the CGRAM address bits C<sub>5</sub> to C<sub>0</sub> set in the instruction code at that time.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

8) DDRAM Address Setting

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R $\overline{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 0               | 0                | 1               | D <sub>6</sub>  | D <sub>5</sub>  | D <sub>4</sub>  | D <sub>3</sub>  | D <sub>2</sub>  | D <sub>1</sub>  | D <sub>0</sub>  |

This instruction sets the character data corresponding to the DDRAM address represented by the bits D6 to D0 (binary).

The DDRAM addresses are valid until CGRAM or ABRAM addresses are set.

The CPU writes or reads character patterns starting from the one represented by the DDRAM address bits D6 to D0 set in the instruction code at that time.

In the 1–line mode (the “N” bit is “1”), the DDRAM address represented by bits D6 to D0 (binary) should be in the range “00” to “4F” in hexadecimal.

In the 2–line mode (the “N” bit is “2”), the DDRAM address represented by bits D6 to D0 (binary) should be in the range “00” to “27” or “40” to “67” in hexadecimal.

If an address other than above is input, the ML9041 cannot properly write a character code in or read it from the DDRAM.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

9) DDRAM/ABRAM/CGRAM Data Write

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R $\overline{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 1               | 0                | E <sub>7</sub>  | E <sub>6</sub>  | E <sub>5</sub>  | E <sub>4</sub>  | E <sub>3</sub>  | E <sub>2</sub>  | E <sub>1</sub>  | E <sub>0</sub>  |

This instruction writes data represented by bits E7 to E0 (binary) to DDRAM, ABRAM or CGRAM.

After data is written, the cursor, blink or display shifts according to the Cursor/Display Shift instruction (see 5)).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

10) Busy Flag/Address Counter Read (Execution time: 1  $\mu$ s)

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 0               | 1           | BF              | O <sub>6</sub>  | O <sub>5</sub>  | O <sub>4</sub>  | O <sub>3</sub>  | O <sub>2</sub>  | O <sub>1</sub>  | O <sub>0</sub>  |

The “BF” bit (DB7) of this instruction tells whether the ML9041 is busy in internal operation (BF = “1”) or not (BF = “0”).

When the “BF” bit is “1”, the ML9041 cannot accept any other instructions. Before inputting a new instruction, check that the “BF” bit is “0”.

When the “BF” bit is “0”, the ML9041 outputs the correct value of the address counter. The value of the address counter is equal to the DDRAM, ABRAM or CGRAM address. Which of the DDRAM, ABRAM and CGRAM addresses is set in the counter is determined by the preceding address setting.

When the “BF” bit is “1”, the value of the address counter is not always correct because it may have been incremented or decremented by 1 during internal operation.

11) DDRAM/ABRAM/CGRAM Data Read

|                   | RS <sub>1</sub> | RS <sub>0</sub> | R $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-------------------|-----------------|-----------------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Instruction code: | 1               | 1               | 1           | P <sub>7</sub>  | P <sub>6</sub>  | P <sub>5</sub>  | P <sub>4</sub>  | P <sub>3</sub>  | P <sub>2</sub>  | P <sub>1</sub>  | P <sub>0</sub>  |

A character code (P<sub>7</sub> to P<sub>0</sub>) is read from the DDRAM, Display-ON data (P<sub>7</sub> to P<sub>0</sub>) from the ABRAM or a character pattern (P<sub>7</sub> to P<sub>0</sub>) from the CGRAM.

The DDRAM, ABRAM or CGRAM is selected at the preceding address setting.

After data is read, the address counter (ADC) is incremented or decremented as set by the Transfer Mode Setting instruction (see 3).

Note: Conditions for reading correct data

(1) The DDRAM, ABRAM or CGRAM Setting instruction is input before this data read instruction is input.

(2) When reading a character code from the DDRAM, the Cursor/Display Shift instruction (see 5) is input before this Data Read instruction is input.

(3) When two or more consecutive RAM Data Read instructions are executed, the following read data is correct.

Correct data is not output under conditions other than the cases (1), (2) and (3) above.

Note: The execution time of this instruction is 37  $\mu$ s at an oscillation frequency (OSC) of 270 kHz.

**Expansion Instruction Codes**

The busy status of the ML9041 is rather longer than the cycle time of the CPU, since the internal processing of the ML9041 starts at a timing which does not affect the display on the LCD. In the busy status (Busy Flag is "1"), the ML9041 executes the Busy Flag Read instruction only. Therefore, the CPU should ensure that the Busy Flag is "0" before sending an expansion instruction code to the ML9041.

1) Arbitrator Display Line Set

|                              |                 |                 |     |                 |                 |                 |                 |                 |                 |                 |                 |
|------------------------------|-----------------|-----------------|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|                              | RS <sub>1</sub> | RS <sub>0</sub> | R/W | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
| Expansion Instruction codes: | 0               | 0               | 0   | 0               | 0               | 0               | 0               | 0               | 0               | 1               | AS              |

This expansion instruction code sets the Arbitrator display line. The relationship between the status of this bit and the common outputs is as follows:

| CSR | duty | AS bit | Shift direction     | Arbitrator's comon pin |
|-----|------|--------|---------------------|------------------------|
| L   | 1/9  | L      | COM1 → COM9         | COM9                   |
| L   | 1/9  | H      | COM2 → COM9, COM1   | COM1                   |
| L   | 1/12 | L      | COM1 → COM12        | COM12                  |
| L   | 1/12 | H      | COM2 → COM12, COM1  | COM1                   |
| L   | 1/17 | L      | COM1 → COM17        | COM17                  |
| L   | 1/17 | H      | COM2 → COM17, COM1  | COM1                   |
| H   | 1/9  | L      | COM9 → COM1         | COM1                   |
| H   | 1/9  | H      | COM8 → COM1, COM9   | COM9                   |
| H   | 1/12 | L      | COM12 → COM1        | COM1                   |
| H   | 1/12 | H      | COM11 → COM1, COM12 | COM12                  |
| H   | 1/17 | L      | COM17 → COM1        | COM1                   |
| H   | 1/17 | H      | COM16 → COM1, COM17 | COM17                  |

2) Contrast Adjusting Data Write

|                              |                 |                 |     |                 |                 |                 |                 |                 |                 |                 |                 |
|------------------------------|-----------------|-----------------|-----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|                              | RS <sub>1</sub> | RS <sub>0</sub> | R/W | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
| Expansion Instruction codes: | 0               | 0               | 0   | 0               | 0               | 1               | F <sub>4</sub>  | F <sub>3</sub>  | F <sub>2</sub>  | F <sub>1</sub>  | F <sub>0</sub>  |

This instruction writes contrast adjusting data (F<sub>4</sub> to F<sub>0</sub>) to the contrast register. After contrast adjusting data is written in the register, the potential (VLCD) output to the V<sub>5</sub> pin varies according to the data written. The VLCD becomes maximum when the content of the contrast register is "1F" (hexadecimal) and becomes minimum when it is "00" (hexadecimal).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

## 3) Contrast Adjusting Data Read

|                             | RS <sub>1</sub> | RS <sub>0</sub> | R/ $\overline{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-----------------------------|-----------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Expansion Instruction code: | 0               | 0               | 1                 | 0               | 0               | 0               | G <sub>4</sub>  | G <sub>3</sub>  | G <sub>2</sub>  | G <sub>1</sub>  | G <sub>0</sub>  |

This instruction reads contrast adjusting data (G<sub>4</sub> to G<sub>0</sub>) from the contrast register.

Note: The execution time of this instruction is 37  $\mu$ s at an oscillation frequency (OSC) of 270 kHz.

## 4) ABRAM Address Setting

|                             | RS <sub>1</sub> | RS <sub>0</sub> | R/ $\overline{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-----------------------------|-----------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Expansion Instruction code: | 0               | 0               | 1                 | 0               | 1               | 1               | H <sub>4</sub>  | H <sub>3</sub>  | H <sub>2</sub>  | H <sub>1</sub>  | H <sub>0</sub>  |

This instruction sets the character data corresponding to the ABRAM address represented by the bits H<sub>4</sub> to H<sub>0</sub> (binary).

The ABRAM addresses are valid until CGRAM or DDRAM addresses are set.

The CPU writes or reads character patterns starting from the one represented by the ABRAM address bits H<sub>4</sub> to H<sub>0</sub> set in the instruction code at that time.

The ABRAM address represented by bits H<sub>4</sub> to H<sub>0</sub> (binary) should be in the range "00" to "13" in hexadecimal.

If an address other than above is input, the ML9041 cannot properly write a character code in or read it from the DDRAM.

Note: The execution time of this instruction is 37  $\mu$ s at an oscillation frequency (OSC) of 270 kHz.

**LCD Drive Waveforms**

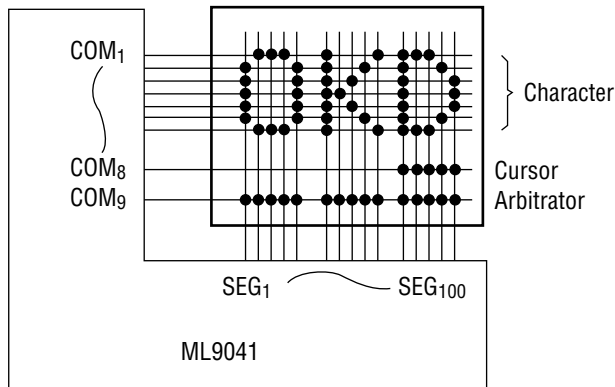
The COM and SEG waveforms (AC signal waveforms for display) vary according to the duty (1/9, 1/12 and 1/17 duties). See 1) to 3) below.

The relationship between the duty ratio and the frame frequency is as follows:

| Duty ratio | Frame Frequency |
|------------|-----------------|
| 1/9        | 75.0Hz          |
| 1/12       | 56.3Hz          |
| 1/17       | 79.4Hz          |

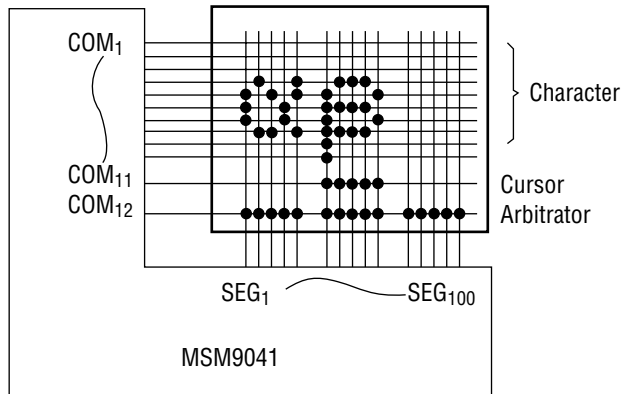
Note: At an oscillation frequency (OSC) of 270 kHz

(1) Driving the LCD of one 20-character line (1/9 duty, CSR = L, AS = 0) under the conditions of the 1-line display mode and the character font of 5 × 7 dots



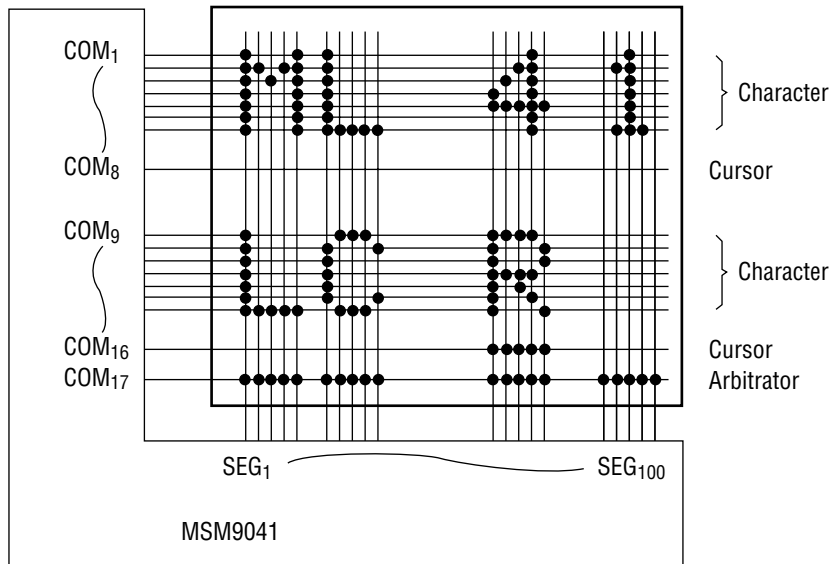
- COM<sub>10</sub> to COM<sub>17</sub> output Display-OFF common signals.

(2) Driving the LCD of one 20-character line (1/12 duty, CSR = L, AS = 0) under the conditions of the 1-line display mode and the character font of 5 × 10 dots



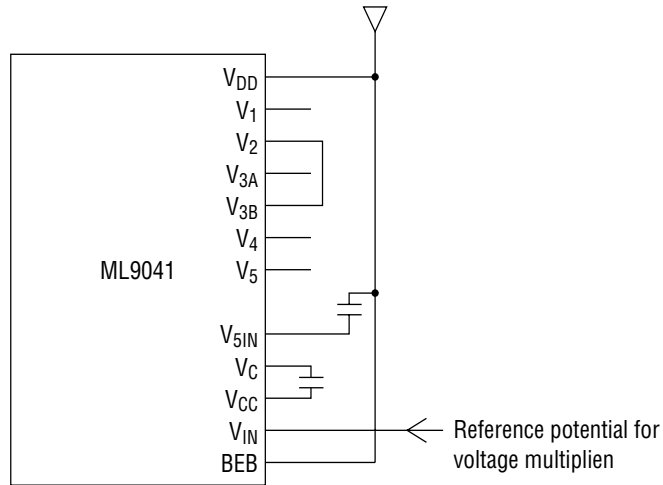
- COM<sub>13</sub> to COM<sub>17</sub> output Display-OFF common signals.

(3) Driving the LCD of two 20-character line (1/17 duty, CSR = L, AS = 0) under the conditions of the 2-line display mode and the character font of 5 × 7 dots

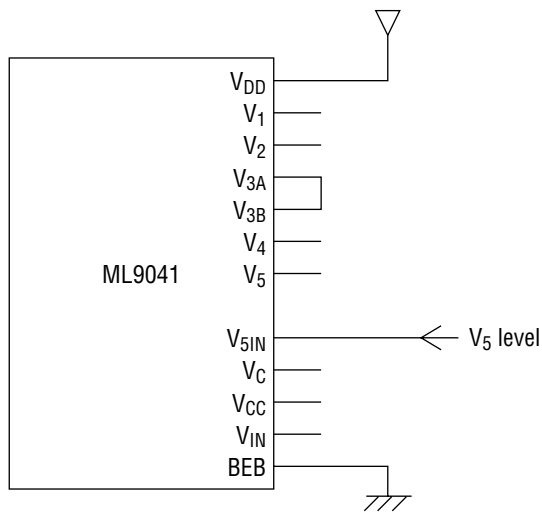


**EXAMPLES OF VLCD GENERATION CIRCUITS**

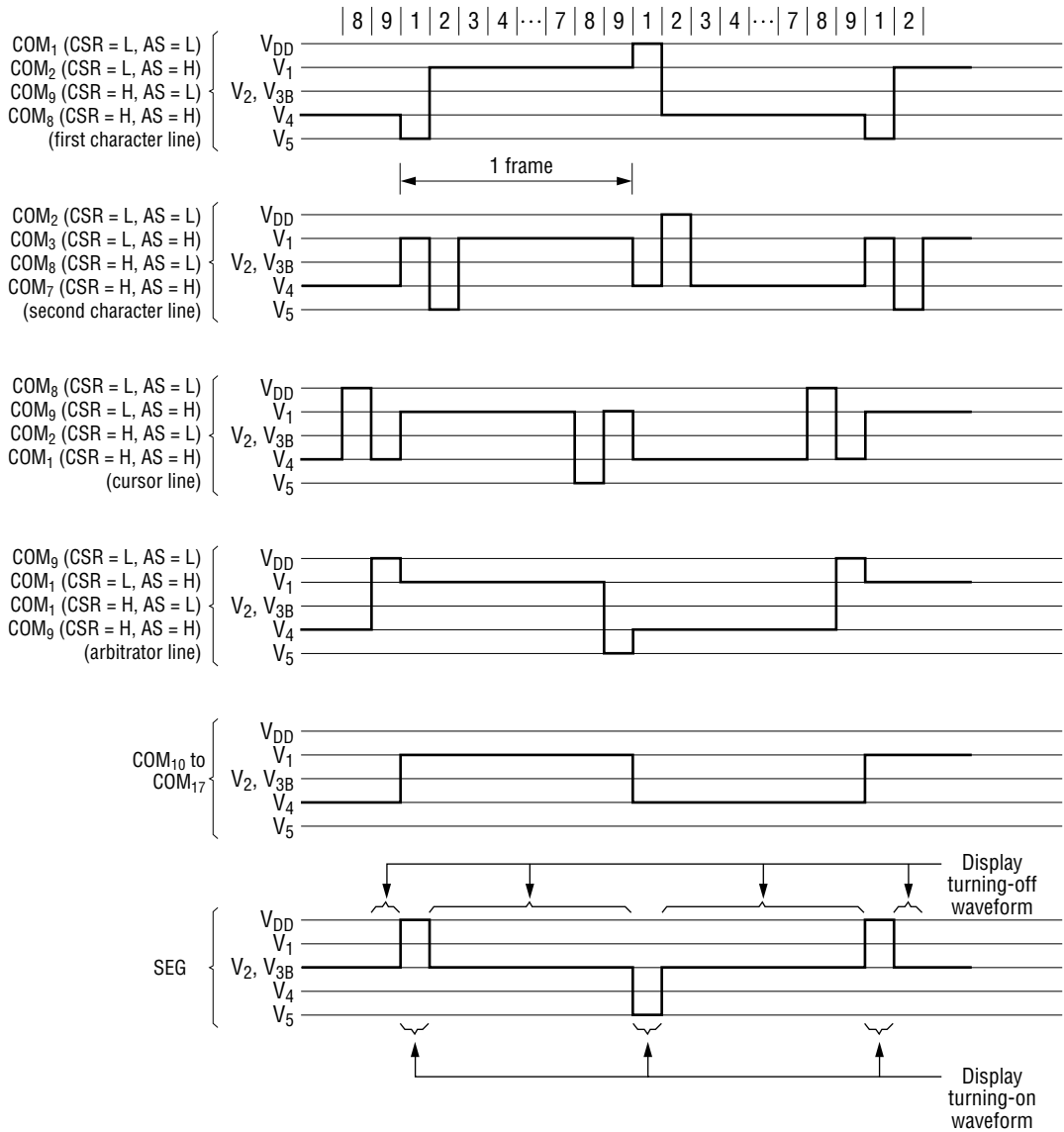
- With 1/4bias, a built-in contrast adjusting circuit and a voltage multiplier



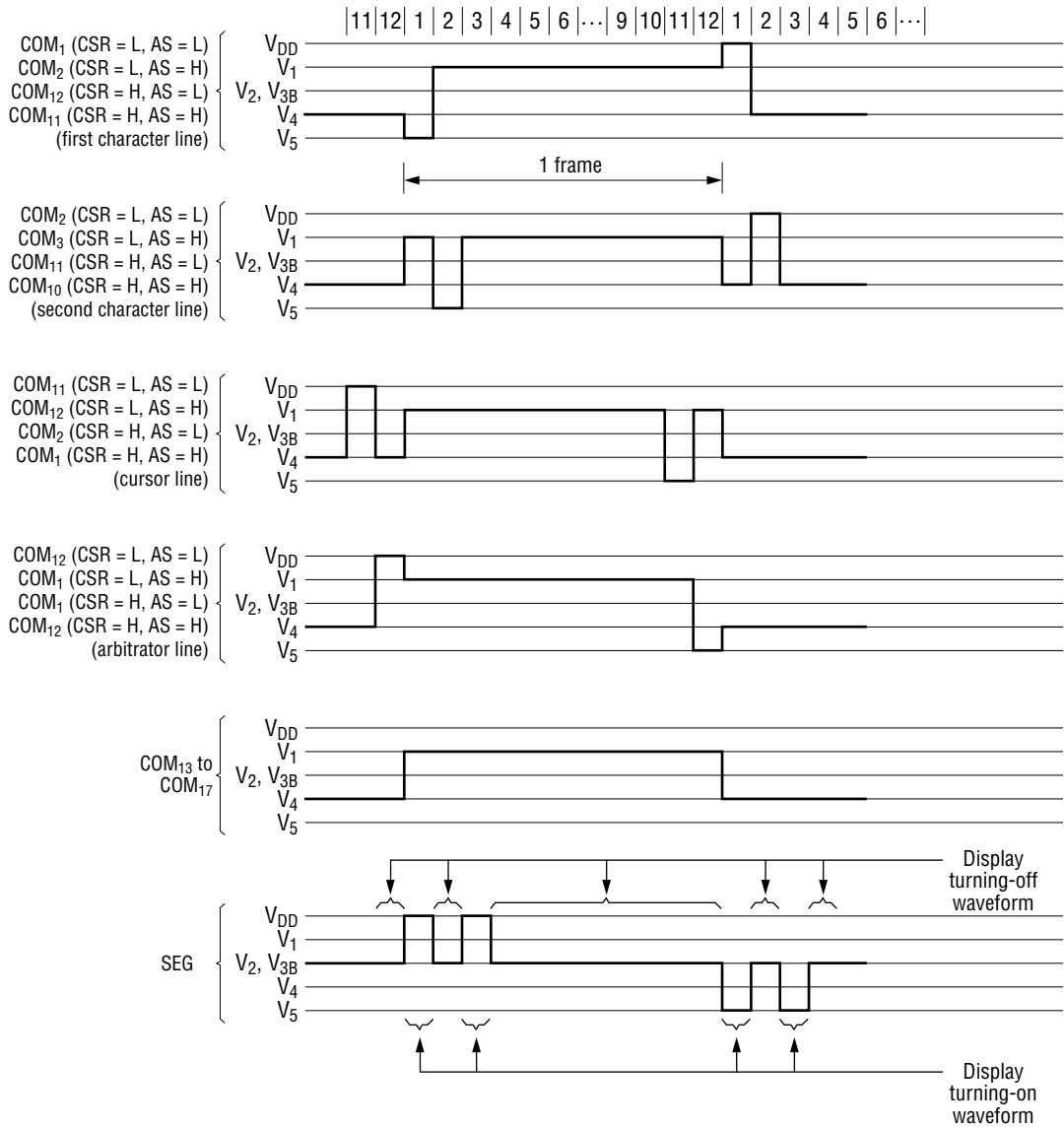
- With 1/5 bias, a built-in contrast adjusting circuit and the V5 level input from an external circuit



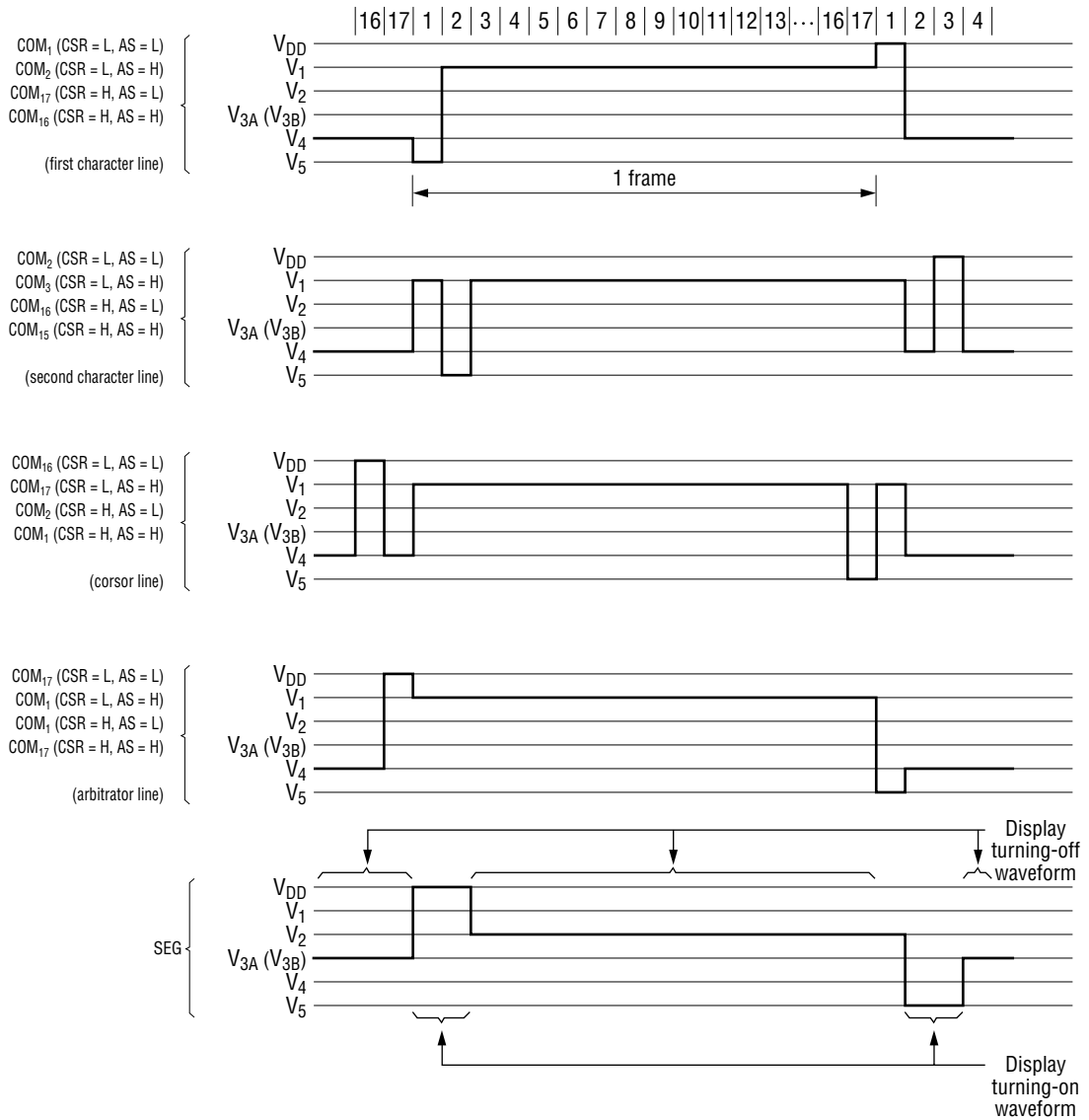
1) COM and SEG Waveforms on 1/9 Duty



2) COM and SEG Waveforms on 1/12 Duty



3) COM and SEG Waveforms on 1/17 Duty



**Initial Setting of Instructions**

(a) Data transfer from and to the CPU using 8 bits of DB0 to DB7

- 1) Turn on the power.
- 2) Wait for 15 ms or more after  $V_{DD}$  has reached 2.5V or higher.
- 3) Set "8 bits" with the Function Setting instruction.
- 4) Wait for 4.1 ms or more.
- 5) Set "8 bits" with the Function Setting instruction.
- 6) Wait for 100  $\mu$ s or more.
- 7) Set "8 bits" with the Function Setting instruction.
- 8) Check the Busy Flag for No Busy (or wait for 100  $\mu$ s or more).
- 9) Set "8 bits", "Number of LCD lines" and "Font size" with the Function Setting instruction. (After this, the number of LCD lines and the font size cannot be changed.)
- 10) Check the Busy Flag for No Busy.
- 11) Execute the Display Mode Setting Instruction, Display Clear Instruction, Entry Mode Setting instruction and Arbitrator Display Line Setting Instruction.
- 12) Check the Busy Flag for No Busy.
- 13) Initialization is completed.

An example of instruction code for 3), 5) and 7)

| RS <sub>1</sub> | RS <sub>0</sub> | R $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> | DB <sub>3</sub> | DB <sub>2</sub> | DB <sub>1</sub> | DB <sub>0</sub> |
|-----------------|-----------------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 1               | 0               | 0           | 0               | 0               | 1               | 1               | ×               | ×               | ×               | ×               |

× : Don't Care

(b) Data transfer from and to the CPU using 8 bits of DB4 to DB7

- 1) Turn on the power.
- 2) Wait for 15 ms or more after  $V_{DD}$  has reached 2.5V or higher.
- 3) Set "8 bits" with the Function Setting instruction.
- 4) Wait for 4.1 ms or more.
- 5) Set "8 bits" with the Function Setting instruction.
- 6) Wait for 100  $\mu$ s or more.
- 7) Set "8 bits" with the Function Setting instruction.
- 8) Check the Busy Flag for No Busy (or wait for 100  $\mu$ s or longer).
- 9) Set "4 bits" with the Function Setting instruction.
- 10) Wait for 100  $\mu$ s or longer.
- 11) Set "4 bits", "Number of LCD lines" and "Font size" with the Initial Setting instruction. (After this, the number of LCD lines and the font size cannot be changed.)
- 12) Check the Busy Flag for No Busy.
- 13) Execute the Display Mode Setting Instruction, Display Clear Instruction, Entry Mode Setting instruction and Arbitrator Display Line Setting Instruction
- 14) Check the Busy Flag for No Busy.
- 15) Initialization is completed.

An example of instruction code for 3), 5) and 7)

| RS <sub>1</sub> | RS <sub>0</sub> | R $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> |
|-----------------|-----------------|-------------|-----------------|-----------------|-----------------|-----------------|
| 1               | 0               | 0           | 0               | 0               | 1               | 1               |

An example of instruction code for 9)

| RS <sub>1</sub> | RS <sub>0</sub> | R/ $\bar{W}$ | DB <sub>7</sub> | DB <sub>6</sub> | DB <sub>5</sub> | DB <sub>4</sub> |
|-----------------|-----------------|--------------|-----------------|-----------------|-----------------|-----------------|
| 1               | 0               | 0            | 0               | 0               | 1               | 0               |

\*: In 13), check the Busy Flag for No Busy before executing each instruction.

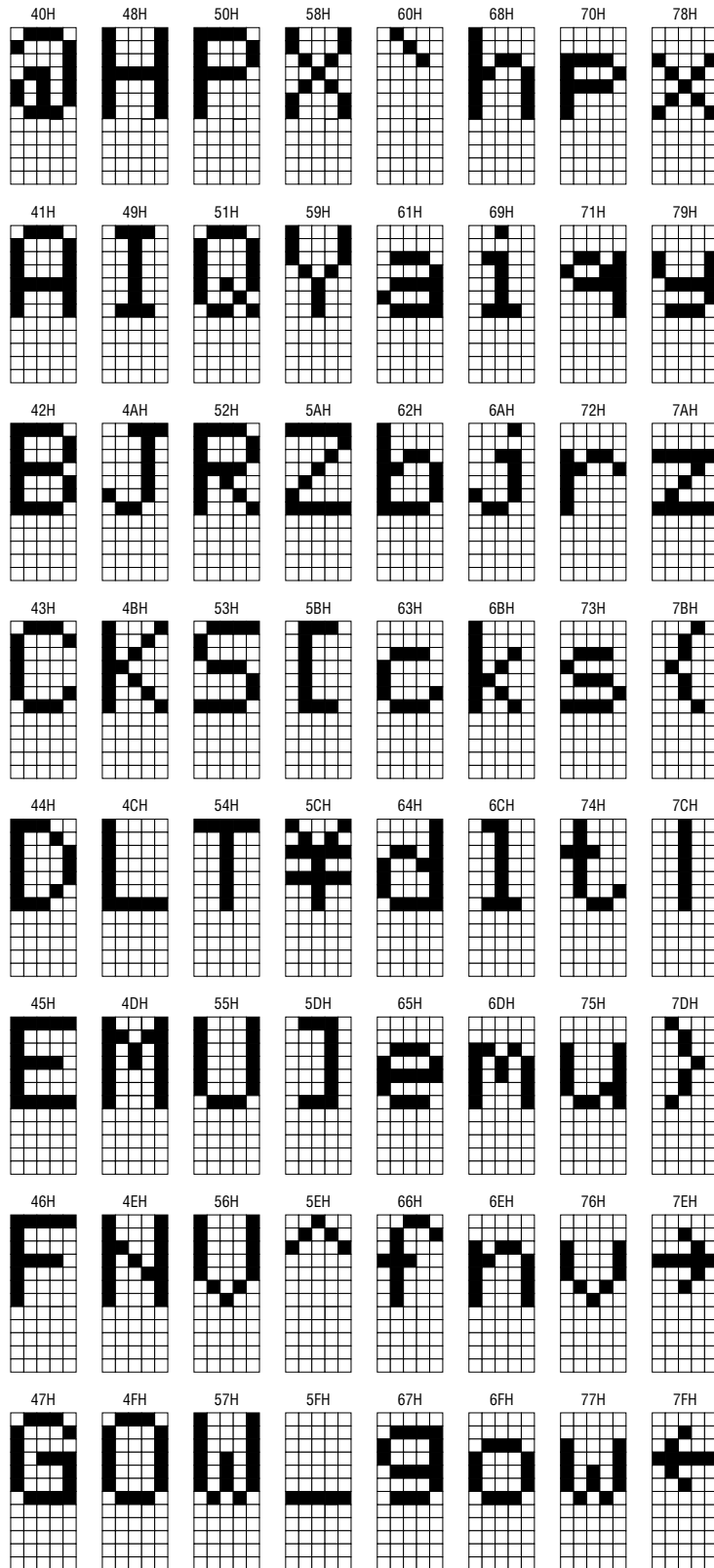
(c) Data transfer from and to the CPU using the serial I/F

- 1) Turn on the power.
- 2) Wait for 15 ms or more after VDD has reached 2.5V or higher.
- 3) Set "Number of LCD lines" and "Font size" with the Function Setting Instruction.
- 4) Execute the Display Mode Setting Instruction, the Display Clear Instruction, the Entry Mode Instruction and the Arbitrator Display Line Setting Instruction.
- 5) Check the busy flag for No Busy.
- 6) Initialization is completed.

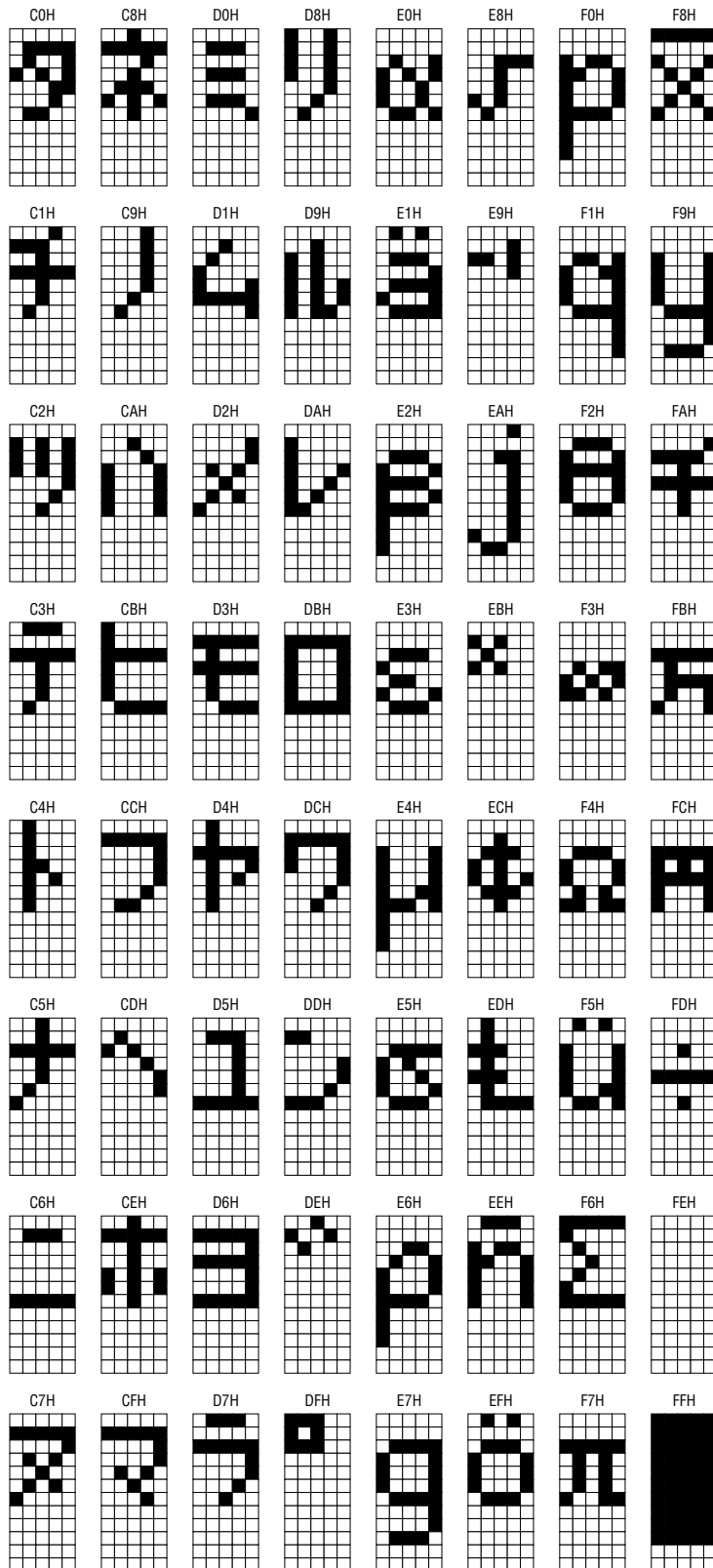
\*: In 3) and 4), check the Busy Flag for No Busy before executing each instruction.

Relationship Between Character Codes and Character patterns

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 00H | 08H | 10H | 18H | 20H | 28H | 30H | 38H |
|     |     |     |     |     |     |     |     |
| 01H | 09H | 11H | 19H | 21H | 29H | 31H | 39H |
|     |     |     |     |     |     |     |     |
| 02H | 0AH | 12H | 1AH | 22H | 2AH | 32H | 3AH |
|     |     |     |     |     |     |     |     |
| 03H | 0BH | 13H | 1BH | 23H | 2BH | 33H | 3BH |
|     |     |     |     |     |     |     |     |
| 04H | 0CH | 14H | 1CH | 24H | 2CH | 34H | 3CH |
|     |     |     |     |     |     |     |     |
| 05H | 0DH | 15H | 1DH | 25H | 2DH | 35H | 3DH |
|     |     |     |     |     |     |     |     |
| 06H | 0EH | 16H | 1EH | 26H | 2EH | 36H | 3EH |
|     |     |     |     |     |     |     |     |
| 07H | 0FH | 17H | 1FH | 27H | 2FH | 37H | 3FH |
|     |     |     |     |     |     |     |     |



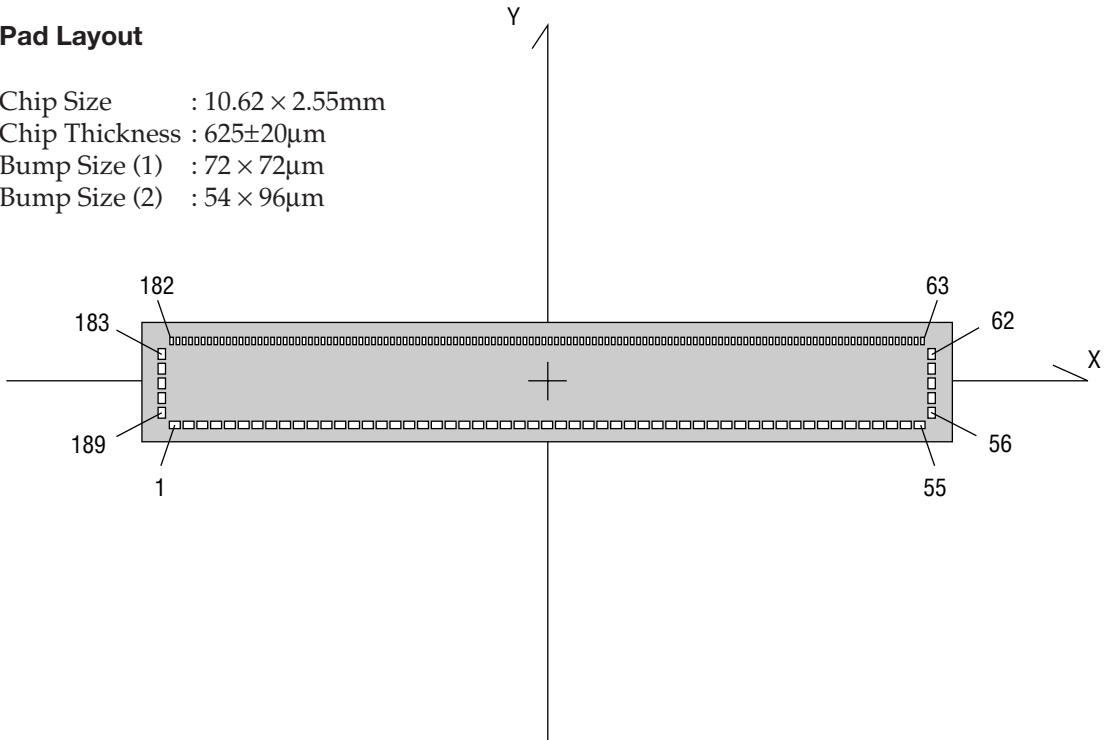
|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 80H | 88H | 90H | 98H | A0H | A8H | B0H | B8H |
| 81H | 89H | 91H | 99H | A1H | A9H | B1H | B9H |
| 82H | 8AH | 92H | 9AH | A2H | AAH | B2H | BAH |
| 83H | 8BH | 93H | 9BH | A3H | ABH | B3H | BBH |
| 84H | 8CH | 94H | 9CH | A4H | ACH | B4H | BCH |
| 85H | 8DH | 95H | 9DH | A5H | ADH | B5H | BDH |
| 86H | 8EH | 96H | 9EH | A6H | AEH | B6H | BEH |
| 87H | 8FH | 97H | 9FH | A7H | AFH | B7H | BFH |



**PAD CONFIGURATION**

**Pad Layout**

Chip Size : 10.62 × 2.55mm  
 Chip Thickness : 625±20µm  
 Bump Size (1) : 72 × 72µm  
 Bump Size (2) : 54 × 96µm



**Pad Coordinates**

| Pad | Symbol           | X (µm) | Y (µm) | Pad | Symbol           | X (µm) | Y (µm) |
|-----|------------------|--------|--------|-----|------------------|--------|--------|
| 1   | V <sub>1</sub>   | -5103  | -1100  | 21  | DB <sub>3</sub>  | -1323  | -1100  |
| 2   | V <sub>2</sub>   | -4914  | -1100  | 22  | DB <sub>2</sub>  | -1134  | -1100  |
| 3   | V <sub>3A</sub>  | -4725  | -1100  | 23  | DB <sub>1</sub>  | -945   | -1100  |
| 4   | V <sub>3B</sub>  | -4536  | -1100  | 24  | DB <sub>0</sub>  | -756   | -1100  |
| 5   | V <sub>4</sub>   | -4347  | -1100  | 25  | E                | -567   | -1100  |
| 6   | V <sub>5</sub>   | -4158  | -1100  | 26  | R/W              | -378   | -1100  |
| 7   | V <sub>5IN</sub> | -3969  | -1100  | 27  | RS <sub>0</sub>  | -189   | -1100  |
| 8   | V <sub>CC</sub>  | -3780  | -1100  | 28  | RS <sub>1</sub>  | 0      | -1100  |
| 9   | V <sub>C</sub>   | -3591  | -1100  | 29  | SO               | 189    | -1100  |
| 10  | V <sub>IN</sub>  | -3402  | -1100  | 30  | SI               | 378    | -1100  |
| 11  | BEB              | -3213  | -1100  | 31  | SHT              | 567    | -1100  |
| 12  | V <sub>DD</sub>  | -3024  | -1100  | 32  | CS               | 756    | -1100  |
| 13  | CSR              | -2835  | -1100  | 33  | OSC <sub>2</sub> | 945    | -1100  |
| 14  | SSR              | -2646  | -1100  | 34  | OSC <sub>R</sub> | 1134   | -1100  |
| 15  | P/S              | -2457  | -1100  | 35  | OSC <sub>1</sub> | 1323   | -1100  |
| 16  | V <sub>SS</sub>  | -2268  | -1100  | 36  | T <sub>3</sub>   | 1512   | -1100  |
| 17  | DB <sub>7</sub>  | -2079  | -1100  | 37  | T <sub>2</sub>   | 1701   | -1100  |
| 18  | DB <sub>6</sub>  | -1890  | -1100  | 38  | T <sub>1</sub>   | 1890   | -1100  |
| 19  | DB <sub>5</sub>  | -1701  | -1100  | 39  | COM <sub>1</sub> | 2079   | -1100  |
| 20  | DB <sub>4</sub>  | -1512  | -1100  | 40  | COM <sub>2</sub> | 2268   | -1100  |

| Pad | Symbol             | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) | Pad | Symbol            | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) |
|-----|--------------------|---------------------|---------------------|-----|-------------------|---------------------|---------------------|
| 41  | COM <sub>3</sub>   | 2457                | -1100               | 81  | SEG <sub>92</sub> | 3486                | 1088                |
| 42  | COM <sub>4</sub>   | 2646                | -1100               | 82  | SEG <sub>91</sub> | 3402                | 1088                |
| 43  | COM <sub>5</sub>   | 2835                | -1100               | 83  | SEG <sub>90</sub> | 3318                | 1088                |
| 44  | COM <sub>6</sub>   | 3024                | -1100               | 84  | SEG <sub>89</sub> | 3234                | 1088                |
| 45  | COM <sub>7</sub>   | 3213                | -1100               | 85  | SEG <sub>88</sub> | 3150                | 1088                |
| 46  | COM <sub>8</sub>   | 3402                | -1100               | 86  | SEG <sub>87</sub> | 3066                | 1088                |
| 47  | COM <sub>9</sub>   | 3591                | -1100               | 87  | SEG <sub>86</sub> | 2982                | 1088                |
| 48  | COM <sub>10</sub>  | 3780                | -1100               | 88  | SEG <sub>85</sub> | 2898                | 1088                |
| 49  | COM <sub>11</sub>  | 3969                | -1100               | 89  | SEG <sub>84</sub> | 2814                | 1088                |
| 50  | COM <sub>12</sub>  | 4158                | -1100               | 90  | SEG <sub>83</sub> | 2730                | 1088                |
| 51  | COM <sub>13</sub>  | 4347                | -1100               | 91  | SEG <sub>82</sub> | 2646                | 1088                |
| 52  | COM <sub>14</sub>  | 4536                | -1100               | 92  | SEG <sub>81</sub> | 2562                | 1088                |
| 53  | COM <sub>15</sub>  | 4725                | -1100               | 93  | SEG <sub>80</sub> | 2478                | 1088                |
| 54  | COM <sub>16</sub>  | 4914                | -1100               | 94  | SEG <sub>79</sub> | 2394                | 1088                |
| 55  | COM <sub>17</sub>  | 5103                | -1100               | 95  | SEG <sub>78</sub> | 2310                | 1088                |
| 56  | DUMMY              | 5184                | -720                | 96  | SEG <sub>77</sub> | 2226                | 1088                |
| 57  | DUMMY              | 5184                | -480                | 97  | SEG <sub>76</sub> | 2142                | 1088                |
| 58  | DUMMY              | 5184                | -240                | 98  | SEG <sub>75</sub> | 2058                | 1088                |
| 59  | DUMMY              | 5184                | 0                   | 99  | SEG <sub>74</sub> | 1974                | 1088                |
| 60  | DUMMY              | 5184                | 240                 | 100 | SEG <sub>73</sub> | 1890                | 1088                |
| 61  | DUMMY              | 5184                | 480                 | 101 | SEG <sub>72</sub> | 1806                | 1088                |
| 62  | DUMMY              | 5184                | 720                 | 102 | SEG <sub>71</sub> | 1722                | 1088                |
| 63  | DUMMY              | 4998                | 1088                | 103 | SEG <sub>70</sub> | 1638                | 1088                |
| 64  | DUMMY              | 4914                | 1088                | 104 | SEG <sub>69</sub> | 1554                | 1088                |
| 65  | DUMMY              | 4830                | 1088                | 105 | SEG <sub>68</sub> | 1470                | 1088                |
| 66  | DUMMY              | 4746                | 1088                | 106 | SEG <sub>67</sub> | 1386                | 1088                |
| 67  | DUMMY              | 4662                | 1088                | 107 | SEG <sub>66</sub> | 1302                | 1088                |
| 68  | DUMMY              | 4578                | 1088                | 108 | SEG <sub>65</sub> | 1218                | 1088                |
| 69  | DUMMY              | 4494                | 1088                | 109 | SEG <sub>64</sub> | 1134                | 1088                |
| 70  | DUMMY              | 4410                | 1088                | 110 | SEG <sub>63</sub> | 1050                | 1088                |
| 71  | DUMMY              | 4326                | 1088                | 111 | SEG <sub>62</sub> | 966                 | 1088                |
| 72  | DUMMY              | 4242                | 1088                | 112 | SEG <sub>61</sub> | 882                 | 1088                |
| 73  | SEG <sub>100</sub> | 4158                | 1088                | 113 | SEG <sub>60</sub> | 798                 | 1088                |
| 74  | SEG <sub>99</sub>  | 4074                | 1088                | 114 | SEG <sub>59</sub> | 714                 | 1088                |
| 75  | SEG <sub>98</sub>  | 3990                | 1088                | 115 | SEG <sub>58</sub> | 630                 | 1088                |
| 76  | SEG <sub>97</sub>  | 3906                | 1088                | 116 | SEG <sub>57</sub> | 546                 | 1088                |
| 77  | SEG <sub>96</sub>  | 3822                | 1088                | 117 | SEG <sub>56</sub> | 462                 | 1088                |
| 78  | SEG <sub>95</sub>  | 3738                | 1088                | 118 | SEG <sub>55</sub> | 378                 | 1088                |
| 79  | SEG <sub>94</sub>  | 3654                | 1088                | 119 | SEG <sub>54</sub> | 294                 | 1088                |
| 80  | SEG <sub>93</sub>  | 3570                | 1088                | 120 | SEG <sub>53</sub> | 210                 | 1088                |

| Pad | Symbol            | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) | Pad | Symbol            | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) |
|-----|-------------------|---------------------|---------------------|-----|-------------------|---------------------|---------------------|
| 121 | SEG <sub>52</sub> | 126                 | 1088                | 156 | SEG <sub>17</sub> | -2814               | 1088                |
| 122 | SEG <sub>51</sub> | 42                  | 1088                | 157 | SEG <sub>16</sub> | -2898               | 1088                |
| 123 | SEG <sub>50</sub> | -42                 | 1088                | 158 | SEG <sub>15</sub> | -2982               | 1088                |
| 124 | SEG <sub>49</sub> | -126                | 1088                | 159 | SEG <sub>14</sub> | -3066               | 1088                |
| 125 | SEG <sub>48</sub> | -210                | 1088                | 160 | SEG <sub>13</sub> | -3150               | 1088                |
| 126 | SEG <sub>47</sub> | -294                | 1088                | 161 | SEG <sub>12</sub> | -3234               | 1088                |
| 127 | SEG <sub>46</sub> | -378                | 1088                | 162 | SEG <sub>11</sub> | -3318               | 1088                |
| 128 | SEG <sub>45</sub> | -462                | 1088                | 163 | SEG <sub>10</sub> | -3402               | 1088                |
| 129 | SEG <sub>44</sub> | -546                | 1088                | 164 | SEG <sub>9</sub>  | -3486               | 1088                |
| 130 | SEG <sub>43</sub> | -630                | 1088                | 165 | SEG <sub>8</sub>  | -3570               | 1088                |
| 131 | SEG <sub>42</sub> | -714                | 1088                | 166 | SEG <sub>7</sub>  | -3654               | 1088                |
| 132 | SEG <sub>41</sub> | -798                | 1088                | 167 | SEG <sub>6</sub>  | -3738               | 1088                |
| 133 | SEG <sub>40</sub> | -882                | 1088                | 168 | SEG <sub>5</sub>  | -3822               | 1088                |
| 134 | SEG <sub>39</sub> | -966                | 1088                | 169 | SEG <sub>4</sub>  | -3906               | 1088                |
| 135 | SEG <sub>38</sub> | -1050               | 1088                | 170 | SEG <sub>3</sub>  | -3990               | 1088                |
| 136 | SEG <sub>37</sub> | -1134               | 1088                | 171 | SEG <sub>2</sub>  | -4074               | 1088                |
| 137 | SEG <sub>36</sub> | -1218               | 1088                | 172 | SEG <sub>1</sub>  | -4158               | 1088                |
| 138 | SEG <sub>35</sub> | -1302               | 1088                | 173 | DUMMY             | -4242               | 1088                |
| 139 | SEG <sub>34</sub> | -1386               | 1088                | 174 | DUMMY             | -4326               | 1088                |
| 140 | SEG <sub>33</sub> | -1470               | 1088                | 175 | DUMMY             | -4410               | 1088                |
| 141 | SEG <sub>32</sub> | -1554               | 1088                | 176 | DUMMY             | -4494               | 1088                |
| 142 | SEG <sub>31</sub> | -1638               | 1088                | 177 | DUMMY             | -4578               | 1088                |
| 143 | SEG <sub>30</sub> | -1722               | 1088                | 178 | DUMMY             | -4662               | 1088                |
| 144 | SEG <sub>29</sub> | -1806               | 1088                | 179 | DUMMY             | -4746               | 1088                |
| 145 | SEG <sub>28</sub> | -1890               | 1088                | 180 | DUMMY             | -4830               | 1088                |
| 146 | SEG <sub>27</sub> | -1974               | 1088                | 181 | DUMMY             | -4914               | 1088                |
| 147 | SEG <sub>26</sub> | -2058               | 1088                | 182 | DUMMY             | -4998               | 1088                |
| 148 | SEG <sub>25</sub> | -2142               | 1088                | 183 | DUMMY             | -5184               | 720                 |
| 149 | SEG <sub>24</sub> | -2226               | 1088                | 184 | DUMMY             | -5184               | 480                 |
| 150 | SEG <sub>23</sub> | -2310               | 1088                | 185 | DUMMY             | -5184               | 240                 |
| 151 | SEG <sub>22</sub> | -2394               | 1088                | 186 | DUMMY             | -5184               | 0                   |
| 152 | SEG <sub>21</sub> | -2478               | 1088                | 187 | DUMMY             | -5184               | -240                |
| 153 | SEG <sub>20</sub> | -2562               | 1088                | 188 | DUMMY             | -5184               | -480                |
| 154 | SEG <sub>19</sub> | -2646               | 1088                | 189 | DUMMY             | -5184               | -720                |
| 155 | SEG <sub>18</sub> | -2730               | 1088                |     |                   |                     |                     |

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