HB56A18 Series

1,048,576-Word x 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A18 is a 1M x 8 dynamic RAM module, mounted eight 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A18 is 30-pin single in-line package having Lead types (HB56A18A, HB56A18AT), socket type (HB56A18B). Therefore, the HB56A18 makes high density mounting possible without surface mount technology. The HB56A18 provides common data inputs and outputs. Its module board has decoupling capacitors beneath each SOJ.

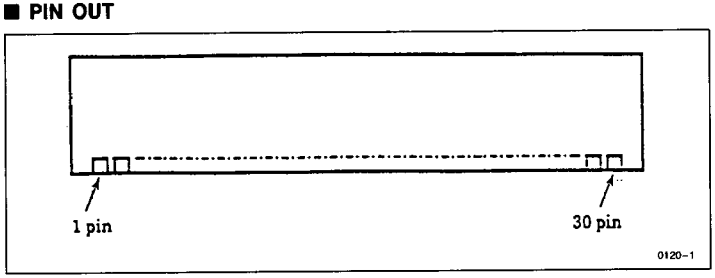
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 3.96 mW/3.52 mW/3.08 mW/2.64 mW/2.20 mW (max)
  - Standby Mode ..... 88 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle ..... (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIMM Socket Type
60 ns	HB56A18A-6H	HB56A18AT-6H	HB56A18B-6H
70 ns	HB56A18A-7H	HB56A18AT-7H	HB56A18B-7H
80 ns	HB56A18A-8A	HB56A18AT-8A	HB56A18B-8A
100 ns	HB56A18A-10A	HB56A18AT-10A	HB56A18B-10A
120 ns	HB56A18A-12A	HB56A18AT-12A	HB56A18B-12A

■ PIN OUT



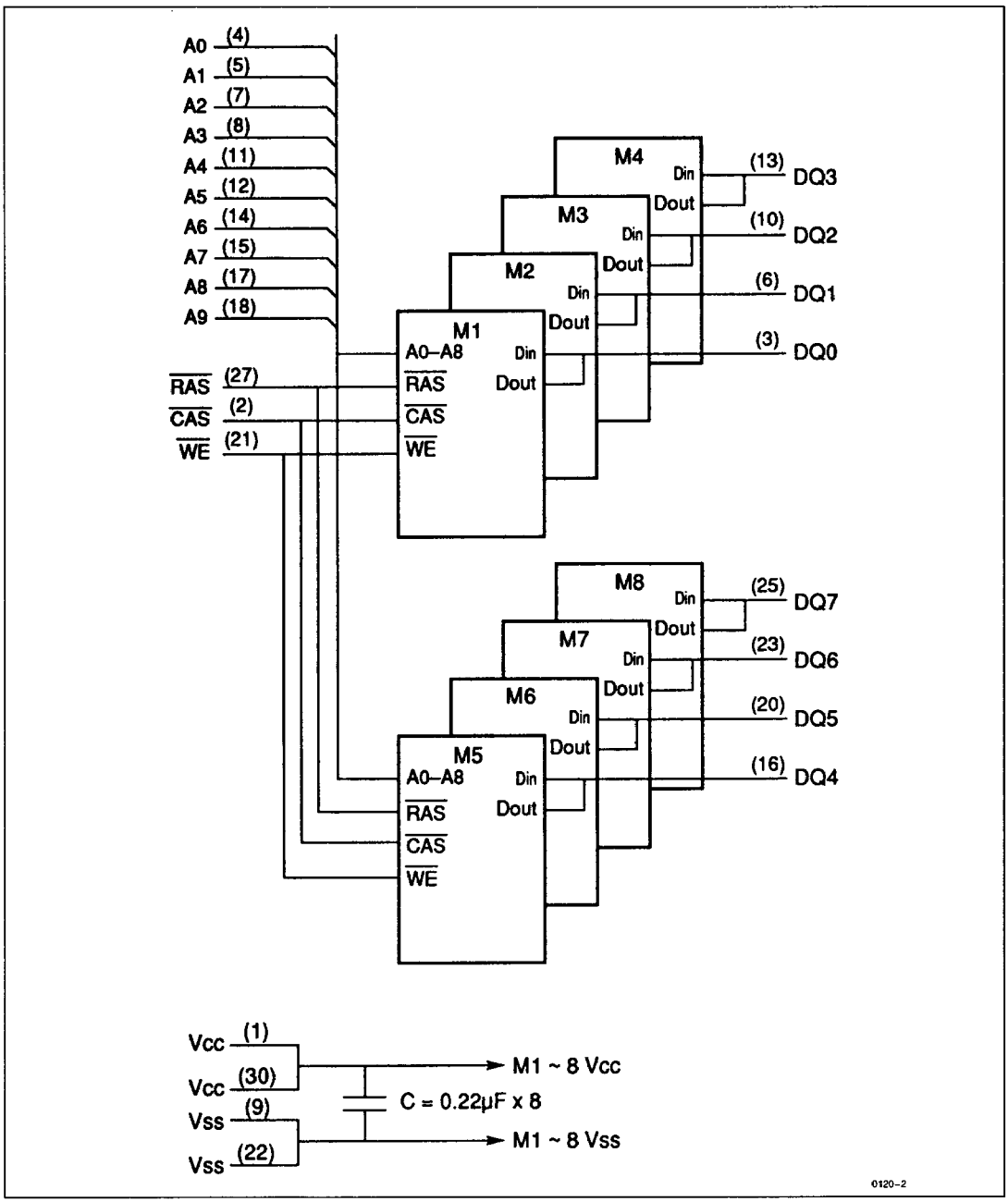
■ PIN DESCRIPTION

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

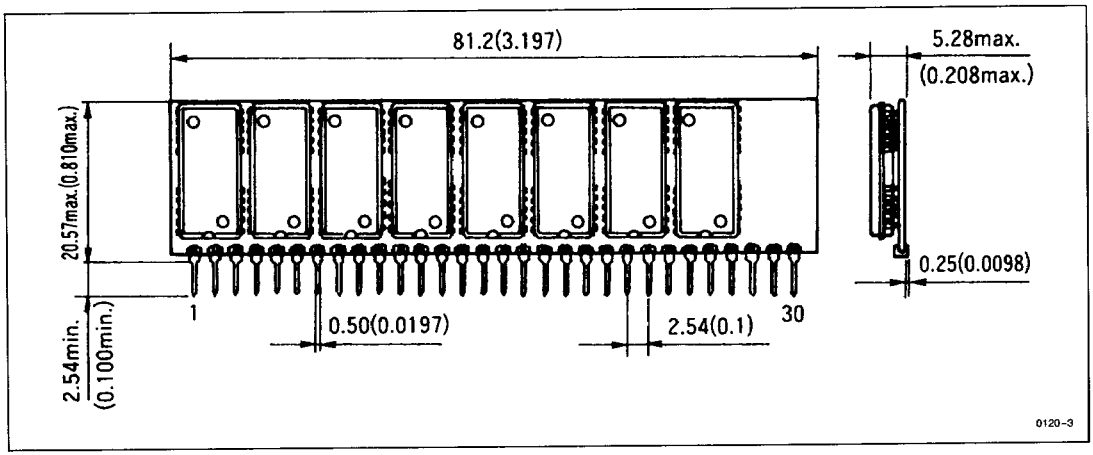
■ BLOCK DIAGRAM



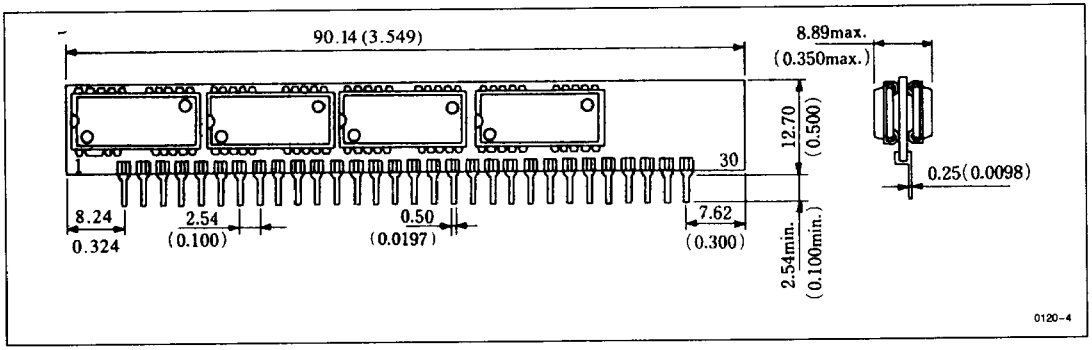
■ PHYSICAL OUTLINE

Unit: mm / inch

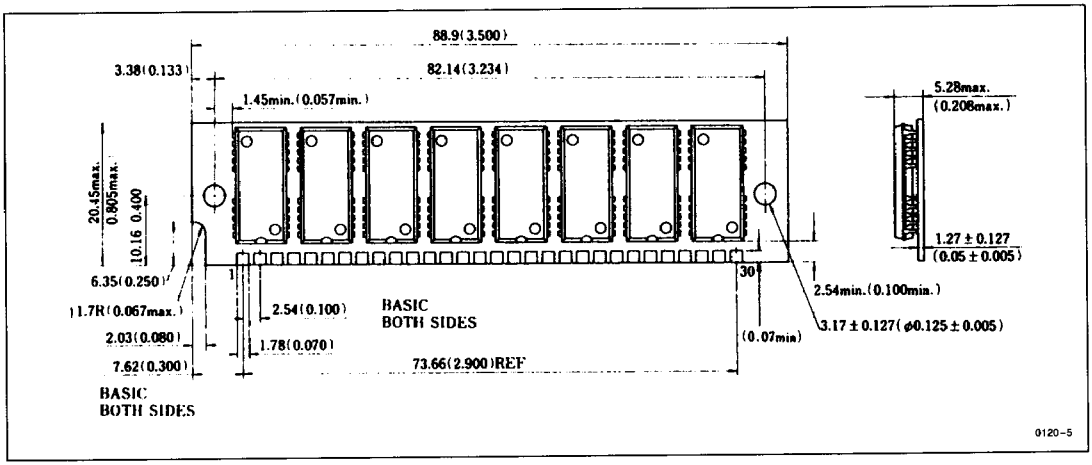
• HB56A18A Series



• HB56A18AT Series



• HB56A18B Series



Note: 1. The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	Input	V_{in}	− 1.0 to + 7.0	V
	Output	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56A18A/AT/B										Unit	Test Conditions	Note
		-6H		-7H		-8A		-10A		-12A				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	720	—	640	—	560	—	480	—	400	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	8	—	8	—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	720	—	640	—	480	—	400	—	360	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	720	—	640	—	480	—	400	—	320	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	720	—	640	—	400	—	400	—	320	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	55	pF	1
Input Capacitance (Clock)	C_{I2}	—	70	pF	1
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics**

Please show at HM511000H series or HM511000A series about AC Characteristics. But don't use by Delayed Write Cycle, because the HB56A18 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}$ (min)).

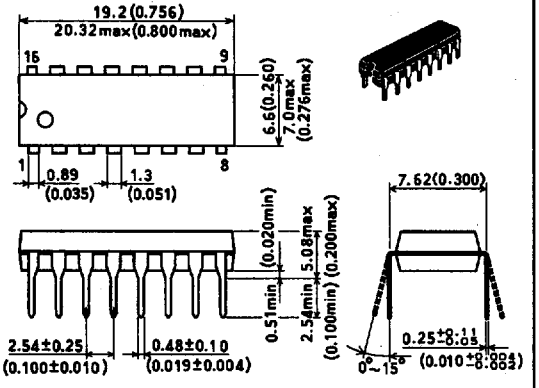
PACKAGE INFORMATION

T-90-20

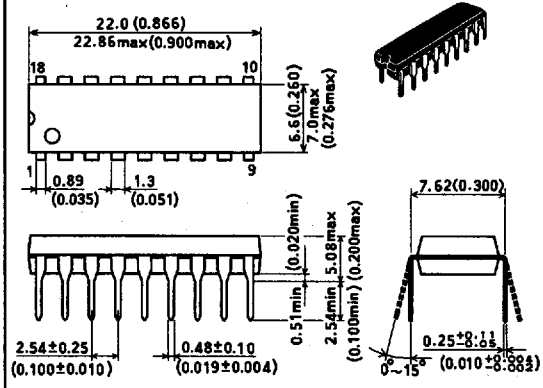
Unit: mm (inch) Scale 3/2

• Dual-in-line Plastic

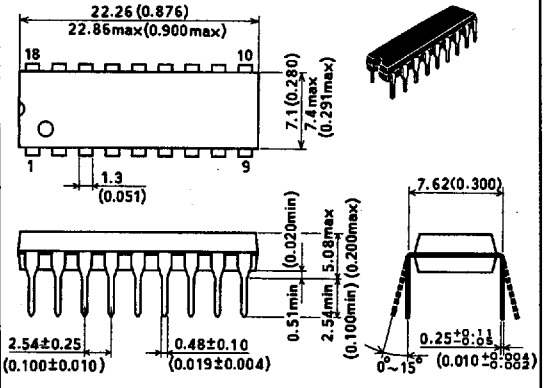
• DP-16B



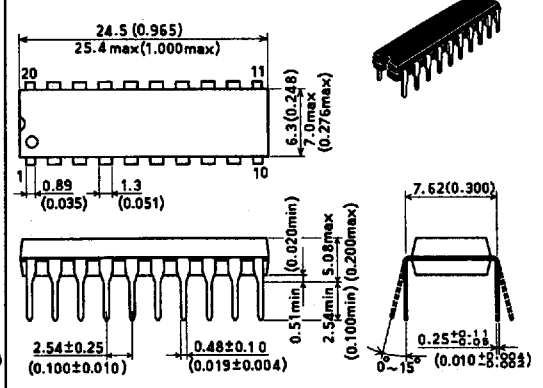
• DP-18B



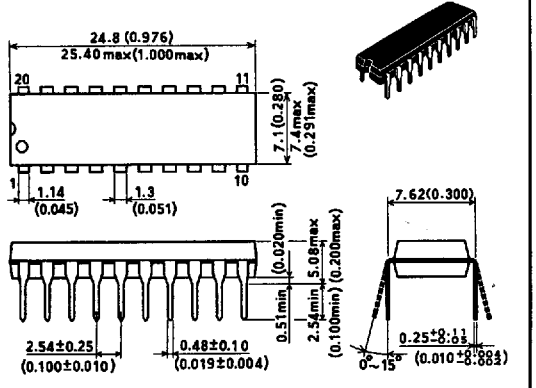
• DP-18C



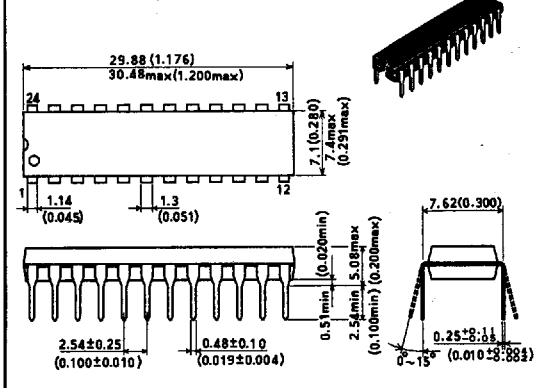
• DP-20N



• DP-20NA



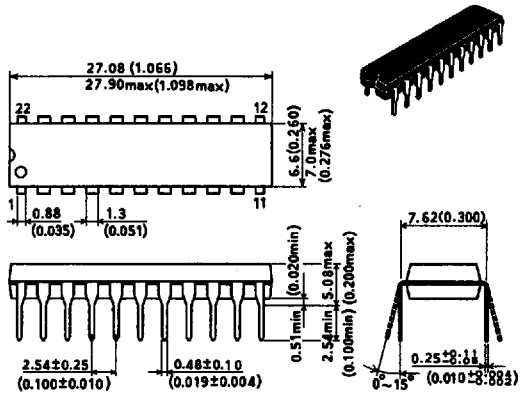
• DP-20NC



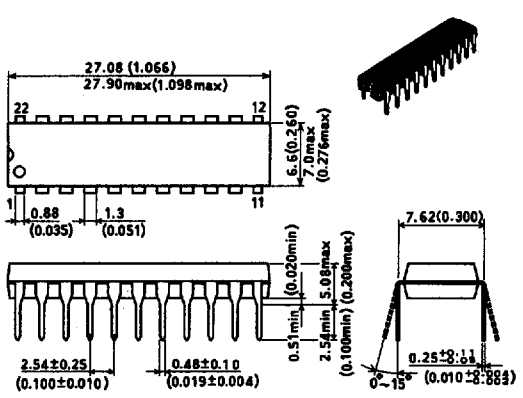
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

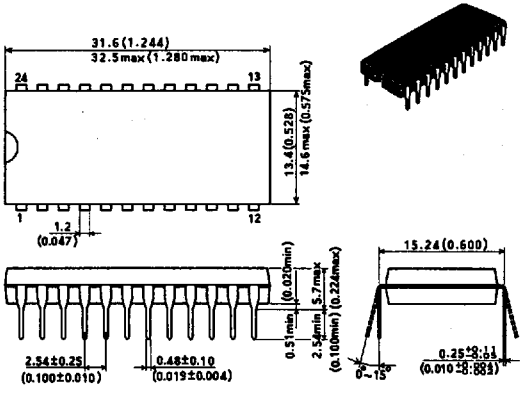
• DP-22N



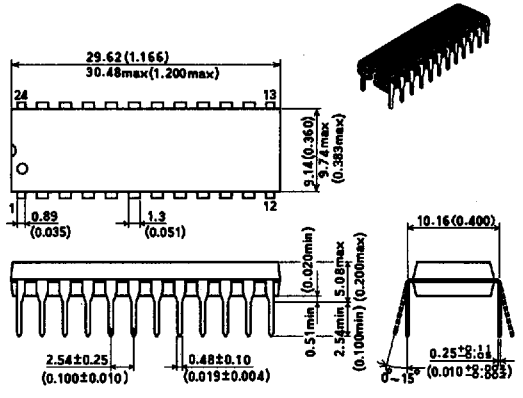
• DP-22NB



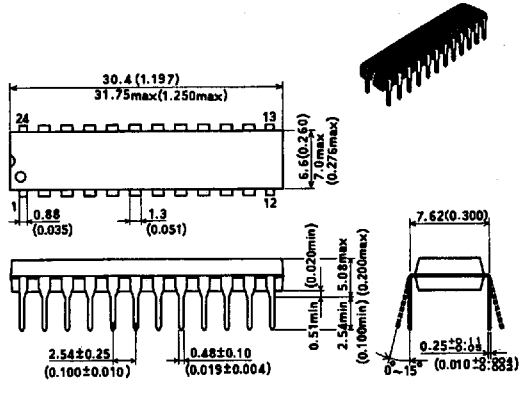
• DP-24



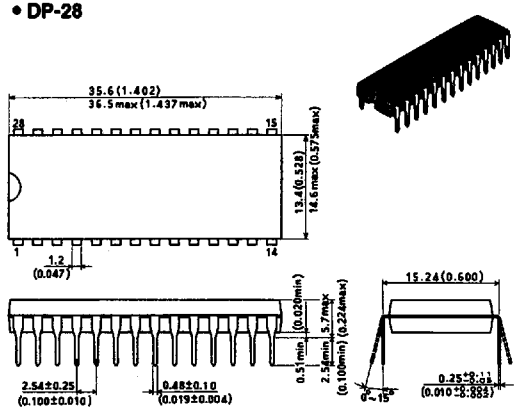
• DP-24A



• DP-24N



• DP-28



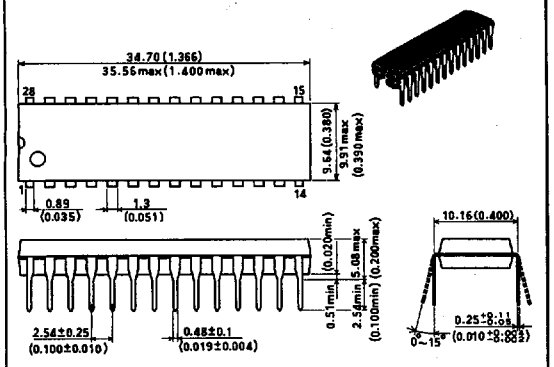
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

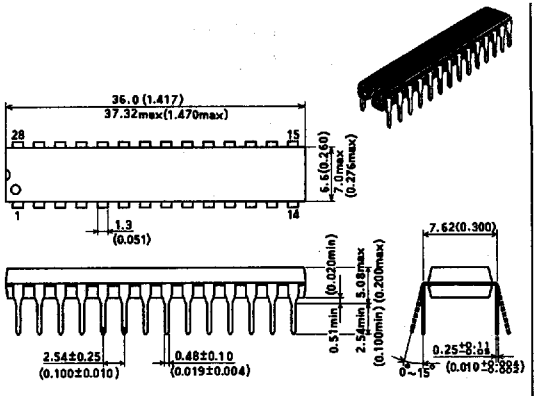
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

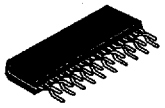


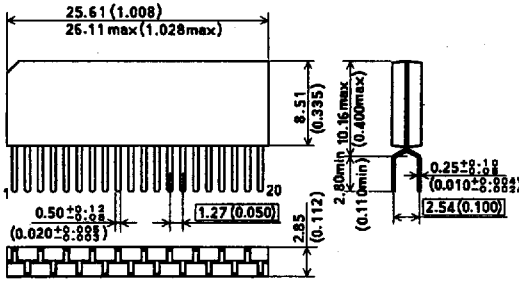
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

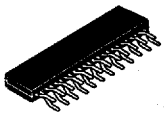
T-90-20

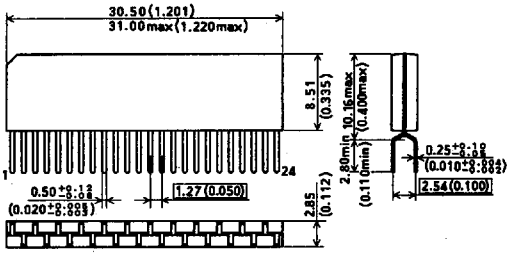
• ZP-20



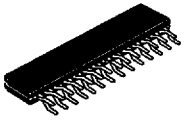


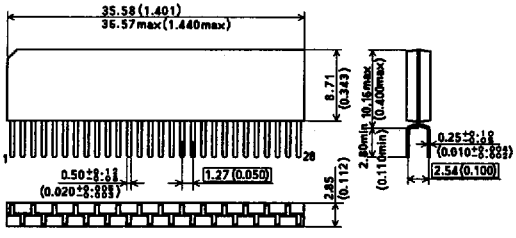
• ZP-24



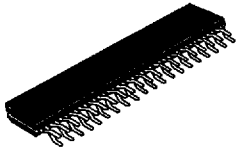


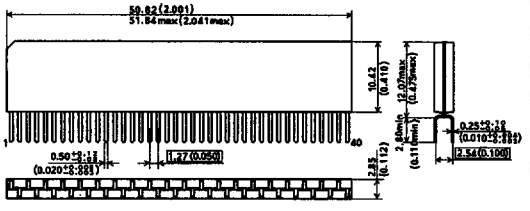
• ZP-28





• ZP-40





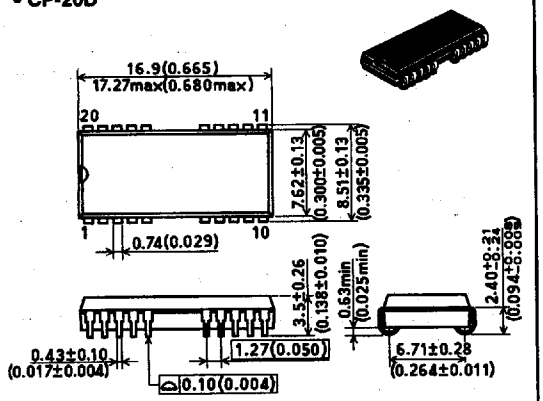
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

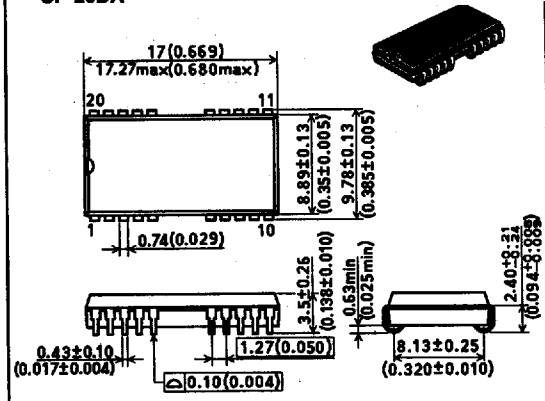
Unit: mm (inch) Scale 3/2

T-90-20

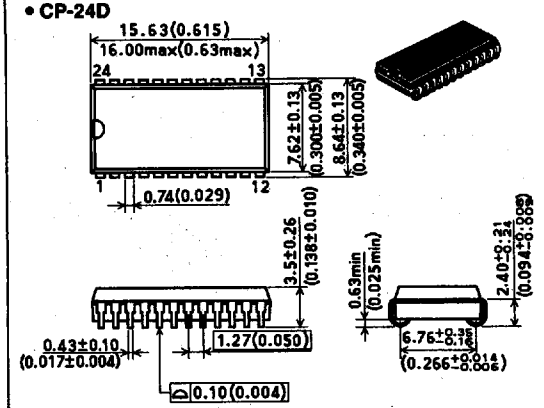
• CP-20D



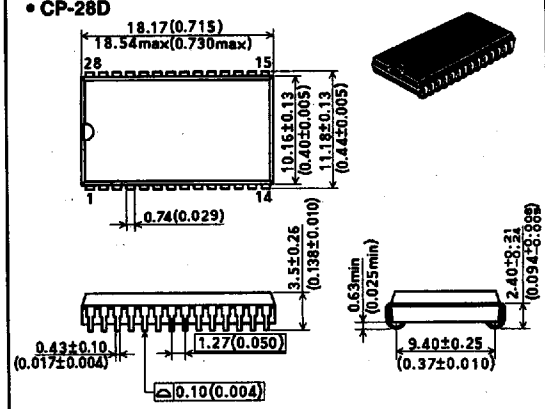
• CP-20DA



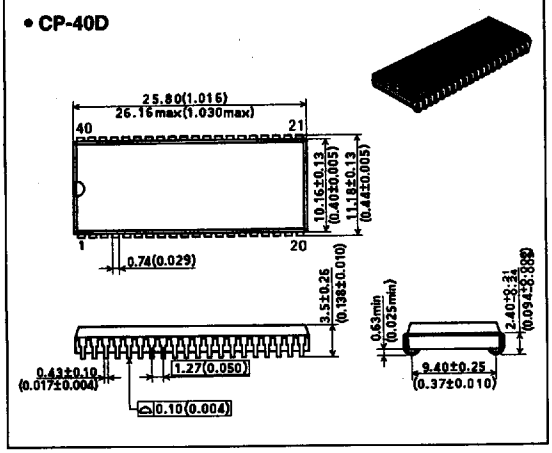
• CP-24D



• CP-28D



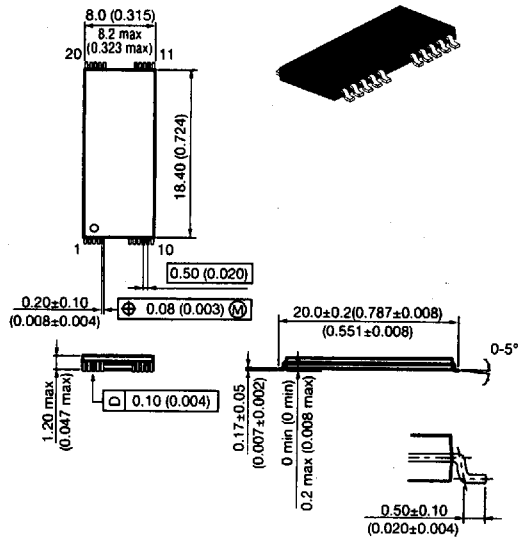
• CP-40D



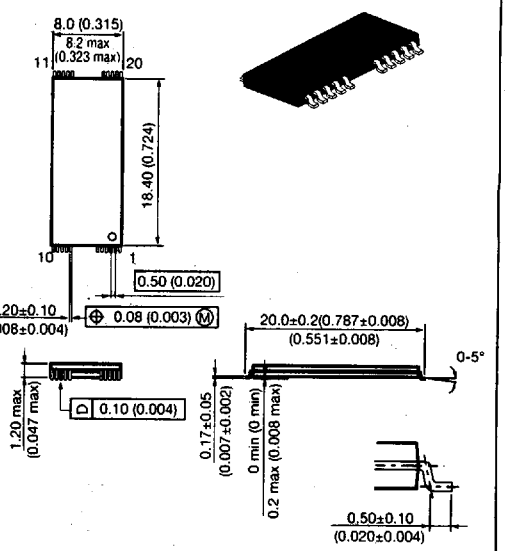
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

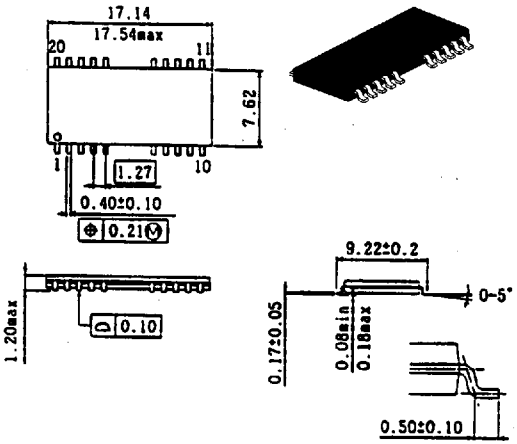
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR