PE45361

Document Category: Advance Information

UltraCMOS® Power Limiter, 10 MHz–6 GHz

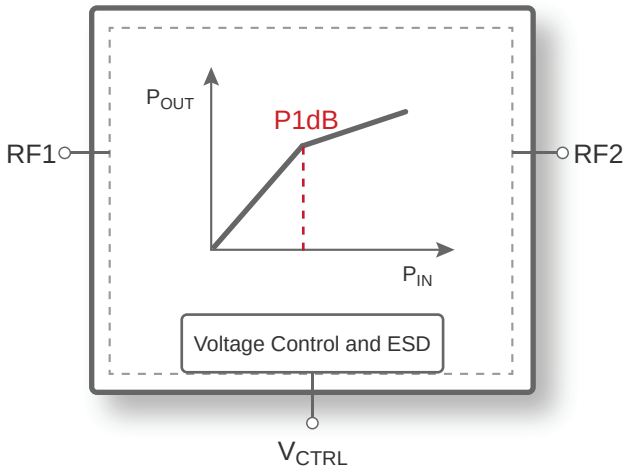
Features

- Monolithic drop-in solution with no external bias components
- Adjustable low power limiting threshold from +5 dBm to +13 dBm
- High maximum power handling of 50 dBm, 100W
- Positive threshold control from +0V to +0.3V
- Fast response time of 1 ns
- Packaging – 12-lead 3 × 3 × 0.5 mm QFN

Applications

- Wireless infrastructure transceivers and antennas
- Test and measurement (T&M)

Figure 1 • *PE45361 Functional Diagram*



Product Description

The PE45361 is a HaRP™ technology-enhanced power limiter designed for use in high performance power limiting applications in test and measurement equipment and wireless infrastructure transceivers and antennas.

Unlike traditional PIN diode solutions, the PE45361 achieves an adjustable input 1 dB compression point or limiting threshold via a low current control voltage (V_{CTRL}), eliminating the need for external bias components such as DC blocking capacitors, RF choke inductors and bias resistors.

It delivers low insertion loss and high linearity under non-limiting power levels and extremely fast response time in a limiting event, ensuring protection of sensitive circuitry. It also offers excellent ESD rating and ESD protection.

The PE45361 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE45361*

Parameter/Condition	Min	Max	Unit
Control voltage, V_{CTRL} • Power limiting mode	0	3.6	V
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(1)		3000	V
ESD voltage CDM, all pins(2)		1000	V

Notes:
1) Human body model (MIL-STD 883 Method 3015).
2) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE45361. Devices should not be operated outside the operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE45361*

Parameter	Min	Typ	Max	Unit
Control voltage, V_{CTRL}				
• Power limiting mode	0		+0.3	V
• Power reflecting mode	0		+3.0	V
RF input power, CW[(1)(4)]			39	dBm
RF input power, pulsed[(2)(4)]			50	dBm
RF input power, unbiased[(2)(3)(4)]			50	dBm
Operating temperature range	–55	+25	+85	°C

Notes:
1) CW, 100% duty cycle, in 10 min, 50Ω @ +25 °C.
2) Pulsed, 1.0% duty cycle of 10 µs pulse width in 1 ms period, 50Ω @ +25 °C.
3) V_{CTRL} = 0V or V_{CTRL} pin left not connected.
4) RF input power handling will begin to degrade below 500 MHz.

Electrical Specifications

Table 3 provides the PE45361 key electrical specifications @ +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3 • *PE45361 Electrical Specifications*

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency		10 MHz		6 GHz	As shown
Power limiting mode					
Insertion loss	10 MHz–3 GHz 3–6 GHz		0.5 0.95	TBD TBD	dB dB
Return loss	10 MHz–3 GHz 3–6 GHz		20 15		dB dB
P1dB/limiting threshold	V_{CTRL} = 0V @ 915 MHz V_{CTRL} = +0.15V @ 915 MHz V_{CTRL} = +0.3V @ 915 MHz		13 10 5		dBm dBm dBm
Leakage power(1)	V_{CTRL} = 0V @ 915 MHz V_{CTRL} = +0.15V @ 915 MHz V_{CTRL} = +0.3V @ 915 MHz		16 14.5 13.5	TBD TBD TBD	dBm dBm dBm
Leakage power slope	V_{CTRL} = 0V @ 915 MHz		0.3		dB/dB
Unbiased leakage power(1)	V_{CTRL} = 0V @ 915 MHz		16	TBD	dBm
Input IP2	V_{CTRL} = 0V @ 915 MHz V_{CTRL} = 0V @ 6 GHz		85 70		dBm dBm
Input IP3	V_{CTRL} = 0V @ 915 MHz V_{CTRL} = 0V @ 6 GHz		37 29		dBm dBm
Response time	1 GHz		1		ns
Recovery time(4)	1 GHz, P_{IN}, Pulse = 30 dBm		20		ns
Power reflecting mode(2)					
Leakage power(1)	V_{CTRL} = +3.0V @ 915 MHz		TBD	TBD	dBm
Switching time(3)	State change to 10% RF		TBD		µs

Notes:

1) Measured with +30 dBm CW applied at input.
2) This mode requires the control voltage to toggle between +3.0V and 0V. At +3.0V the limiter equivalent circuit is a low impedance to ground, reflecting most of the incident power back to the source.
3) State change is V_{CTRL} toggle from 0V to +3.0V.
4) Pulsed, 1% duty cycle of 10 µs pulse width in 1 ms period, 50Ω @ +25 °C.

Dual Mode Operation

Power Limiting Mode

The PE45361 performs as a linear power limiter with adjustable P1dB/limiting threshold. The P1dB/limiting threshold can be adjusted by changing the control voltage between 0V and +0.3V. If unbiased, or if V_{CTRL} = 0V, the PE45361 still offers power limiting protection.

Power Reflecting Mode

Power reflecting mode requires a power detector to sample the RF input power and a microcontroller to toggle the limiter control voltage between +3.0V and 0V based on the system protection requirements. At +3.0V, the limiter impedance to ground is less than 1Ω and most of the incident power will be reflected back to the source. At 0V, the device operates as in power limiting mode.

Pin Information

This section provides pinout information for the PE45361. **Figure 2** shows the pin map of this device for the available package. **Table 4** provides a description for each pin.

Figure 2 • *Pin Configuration (Top View)*

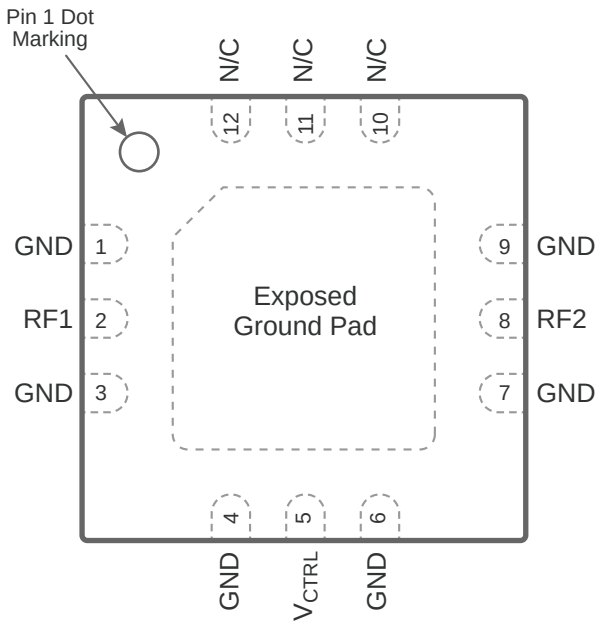


Table 4 • *Pin Descriptions for PE45361*

Pin No.	Pin Name	Description
1, 3, 4, 6, 7, 9	GND	Ground
2	RF1[1][3]	RF port 1
5	V_{CTRL}	Control voltage
8	RF2[1][3]	RF port 2
10–12	N/C[2]	No connect
Pad	GND	Exposed pad: ground for proper operation

Notes:

1) RF pins 2 and 8 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) Pins 10–12 can be grounded if deemed necessary by the customer.
3) The limiter is not bi-directional. RF1 is the RF input and RF2 is the RF output.

Packaging Information

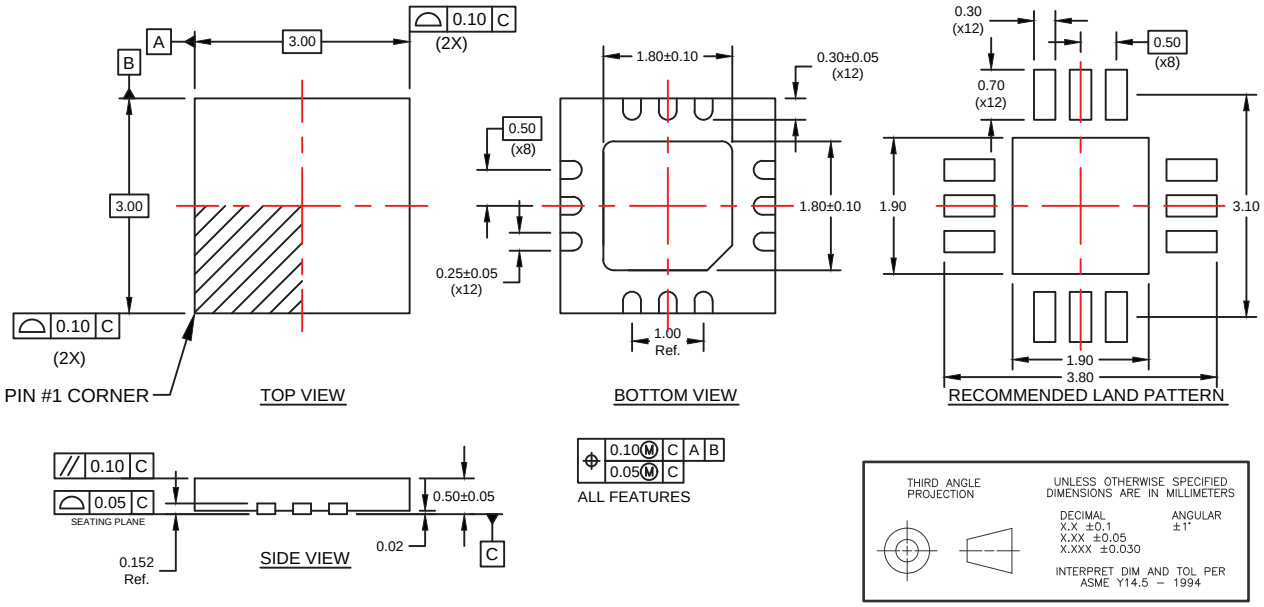
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE45361 in the 12-lead 3 × 3 × 0.5 mm QFN package is MSL1.

Package Drawing

Figure 3 • ***Package Mechanical Drawing for 12-lead 3 × 3 × 0.5 mm QFN***



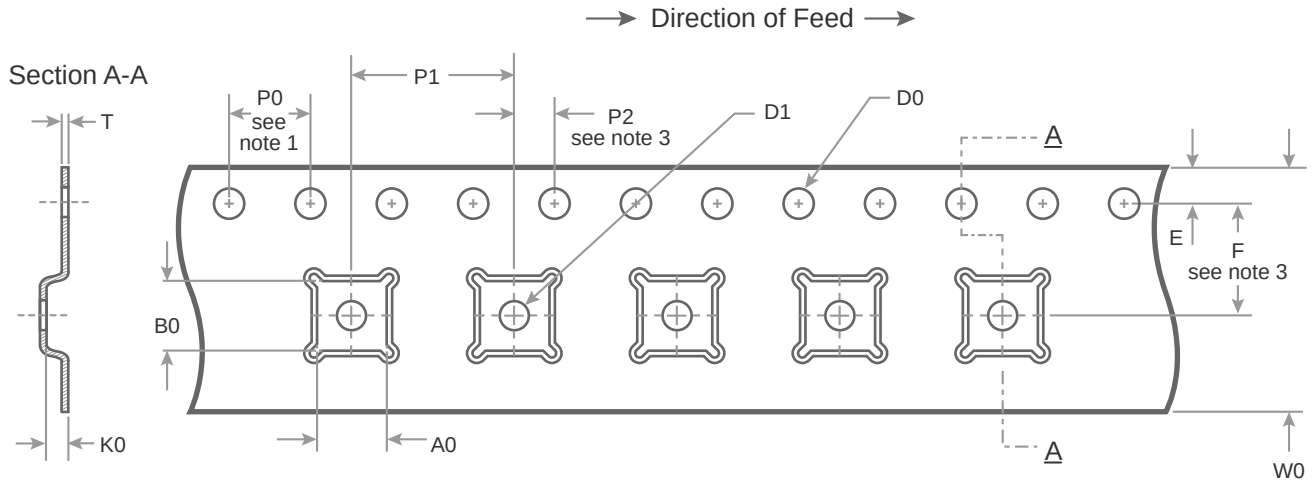
Top-Marking Specification

Figure 4 • ***Package Marking Specifications for PE45361***

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

Figure 5 • ***Tape and Reel Specifications for 12-lead 3 × 3 × 0.5 mm QFN***

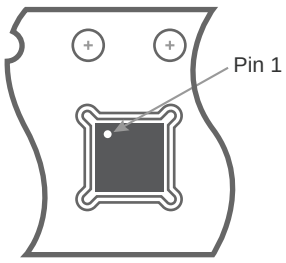


A0	3.3
B0	3.3
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in milimeters unless otherwise specified



Device Orientation in Tape

Ordering Information

Table 5 lists the available ordering codes for the PE45361 as well as available shipping methods.

Table 5 • *Order Codes for PE45361*

Order Codes	Description	Packaging	Shipping Method
PE45361A–G	PE45361 Power limiter	Waffle pack	Waffle pack
EK45361–01	PE45361 Evaluation kit	Evaluation kit	1/box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Not Recommended for New Designs (NRND)

This product is in production but is not recommended for new designs.

End of Life (EOL)

This product is currently going through the EOL process. It has a specific last-time buy date.

Obsolete

This product is discontinued. Orders are no longer accepted for this product.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

Peregrine products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark