# P54/74FCT521/A/B/C (P54/74PCT521/A/B/C) ULTRA-HIGH SPEED CMOS 8-BIT IDENTITY COMPARATORS

## FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-C speed at 4.5ns max. (Com'l) FCT-B speed at 5.5ns max. (Com'l)
- CMOS $V_{OH}$ Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)
- Dsigned for Easy Expansion to Wider Word Widths
- Operational over the Full Commercial and Military Temperature Ranges
- Input Clamp Diode to Limit Bus Reflections
- Manufactured in 0.8 micron PACE Technology™

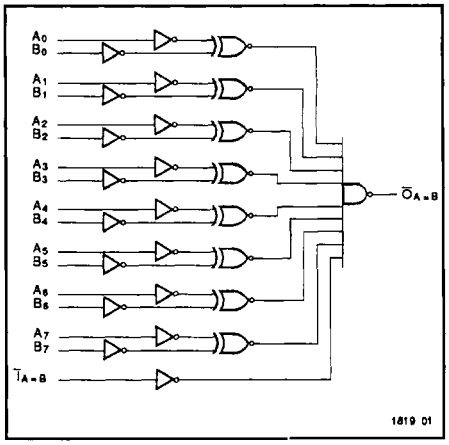
## DESCRIPTION

The 'FCT521 are ultra-fast expandable eight-bit comparators. Each device compares two words of upto 8 bits each. The output goes to a low level when the two words being compared match bitwise. The word width maybe expanded by cascading (i.e., connecting the output of the comparator to the expansion input $\overline{I}_{A=B}$ of another 'FCT521 device) or by logically ORing the outputs of several 'FCT521 devices. If not used for expansion, $\overline{I}_{A=B}$ must be set at CMOS low voltage. The CMOS comparator typically dissipates one-third the power of its slower bipolar equivalents. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without requiring additional components.

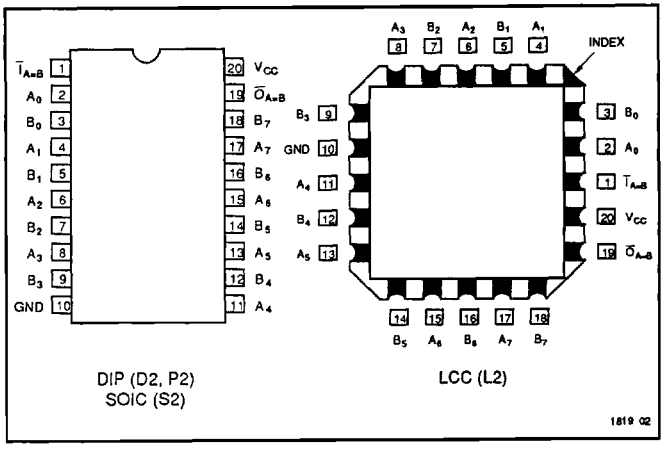
The 'FCT521s are members of the PACE LOGIC™ Family which includes byte-wide bus interface and memory related components. PACE LOGIC is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single-event-upset protection, and is supported by a Class 1 environment facility for volume production.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V supply.

## FUNCTIONAL BLOCK DIAGRAM




## PIN CONFIGURATIONS

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## ABSOLUTE MAXIMUM RATINGS[1,2]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $T_A$ | Ambient Temperature Under Bias | –65 to +135 | °C |
| $V_{CC}$ | $V_{CC}$ Potential to Ground | –0.5 to +7.0 | V |
| $I_{IN}$ | Input Current | –30 to +5.0 | mA |

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| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{OUTPUT}$ | Current Applied to Output | 120 | mA |
| $V_{IN}$ | Input Voltage | –0.5 to $V_{CC}$ + 0.5 | V |
| $V_{OUT}$ | Voltage Applied to Output | –0.5 to $V_{CC}$ + 0.5 | V |

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**Notes:**

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either $V_{CC}$ or ground.

## RECOMMENDED OPERATING CONDITIONS

| Free Air Ambient Temperature | Min | Max |
|---|---|---|
| Military | –55°C | +125°C |
| Commercial | 0°C | +70°C |

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| Supply Voltage ($V_{CC}$) | Min | Max |
|---|---|---|
| Military | +4.5V | +5.5V |
| Commercial | +4.75V | +5.25V |

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## DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

| Symbol | Parameter | | Min | Typ[1] | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | |
| $V_H$ | Hysteresis | | | 0.35 | | V | | All inputs |
| $V_{CD}$ | Input Clamp Diode Voltage | | | –0.7 | –1.2 | V | MIN | $I_{IN}$ = –18mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 3V, $V_{IN}$ = 0.2V, or $V_{CC}$ – 0.2V | $V_{CC}$ – 0.2 | $V_{CC}$ | | V | | $I_{OH}$ = –32µA |
| | | Military/Commercial (CMOS) | $V_{CC}$ – 0.2 | $V_{CC}$ | | V | MIN | $I_{OH}$ = –300µA |
| | | Military (TTL) | 2.4 | 4.3 | | V | MIN | $I_{OH}$ = –12mA |
| | | Commercial (TTL) | 2.4 | 4.3 | | V | MIN | $I_{OH}$ = –15mA |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 3V, $V_{IN}$ = 0.2V, or $V_{CC}$ – 0.2V | | GND | 0.2 | V | | $I_{OL}$ = 300µA |
| | | Military/Commercial (CMOS)[3] | | GND | 0.2 | V | MIN | $I_{OL}$ = 300µA |
| | | Military (TTL) | | 0.3 | 0.5 | V | MIN | $I_{OL}$ = 32mA |
| | | Commercial (TTL) | | 0.3 | 0.5 | V | MIN | $I_{OL}$ = 48mA |
| | | Commercial (TTL) | | 0.3 | 0.5 | V | MIN | $I_{OL}$ = 64mA |
| $I_{IH}$ | Input HIGH Current | | | | 5 | µA | MAX | $V_{IN}$ = $V_{CC}$ |
| $I_{IL}$ | Input LOW Current | | | | –5 | µA | MAX | $V_{IN}$ = GND |
| $I_{IH}$ | Input HIGH Current[3] | | | | 5 | µA | MAX | $V_{OUT}$ = 2.7V |
| $I_{IL}$ | Input LOW Current[3] | | | | –5 | µA | MAX | $V_{OUT}$ = 0.5V |
| $I_{OS}$ | Output Short Circuit Current[2] | | –60 | –120 | | mA | MAX | $V_{OUT}$ = 0.0V |
| $C_{IN}$ | Input Capacitance[3] | | | 5 | 10 | pF | | All inputs |
| $C_{OUT}$ | Output Capacitance[3] | | | 9 | 12 | pF | | All outputs |

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**Notes:**

1. Typical limits are at $V_{CC}$ = 5.0V, $T_A$ = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{os}$ tests should be performed last.
3. This parameter is guaranteed but not tested.

## DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Typ[1] | Max | Units | Conditions |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current (CMOS inputs) | 0.003 | 0.5 | mA | $V_{CC}$ = MAX, $f_1$ = 0, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs) | 0.5 | 2.0 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 3.4V[2], $f_1$ = 0, Outputs Open |
| $I_{CCD}$ | Dynamic Power Supply Current[3] | 0.15 | 0.25 | mA/ mHz | $V_{CC}$ = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| $I_C$ | Total Power Supply Current[5] | 1.7 | 4.0 | mA | $V_{CC}$ = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $f_1$ = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| | | 2.0 | 5.0 | mA | $V_{CC}$ = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $f_1$ = 10MHz, $V_{IN}$ = 3.4V or $V_{IN}$ = GND |

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**Notes:**
1. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
2. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   $I_{CC}$ = Quiescent Current with CMOS input levels
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_0$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_1$ = Input Frequency
   $N_1$ = Number of Inputs at $f_1$
   All currents are in milliamps and all frequencies are in megahertz.

## TRUTH TABLE

| Inputs | | Output |
|---|---|---|
| $\overline{I}_{A=B}$ | A, B | $\overline{O}_{A=B}$ |
| L | A = B* | L |
| L | A ≠ B | H |
| H | A = B* | H |
| H | A ≠ B | H |

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

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## AC CHARACTERISTICS

| Symbol | Parameter | 'FCT521 | | | | 'FCT521A | | | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$A_N$ or $B_N$ to $\overline{O}_{A-B}$ | 1.5 | 15.0 | 1.5 | 11 | 1.5 | 9.5 | 1.5 | 7.2 | ns | 1, 2, 3 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{I}_{A-B}$ to $\overline{O}_{A-B}$ | 1.5 | 8.5 | 1.5 | 7.5 | 1.5 | 7.8 | 1.5 | 6.0 | ns | 1, 3 |

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## AC CHARACTERISTICS

| Symbol | Parameter | 'FCT521B | | | | 'FCT521C | | | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$A_N$ or $B_N$ to $\overline{O}_{A-B}$ | 1.5 | 7.3 | 1.5 | 5.5 | 1.5 | 5.1 | 1.5 | 4.5 | ns | 1, 2, 3 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{I}_{A-B}$ to $\overline{O}_{A-B}$ | 1.5 | 6.0 | 1.5 | 4.6 | 1.5 | 4.5 | 1.5 | 4.1 | ns | 1, 3 |

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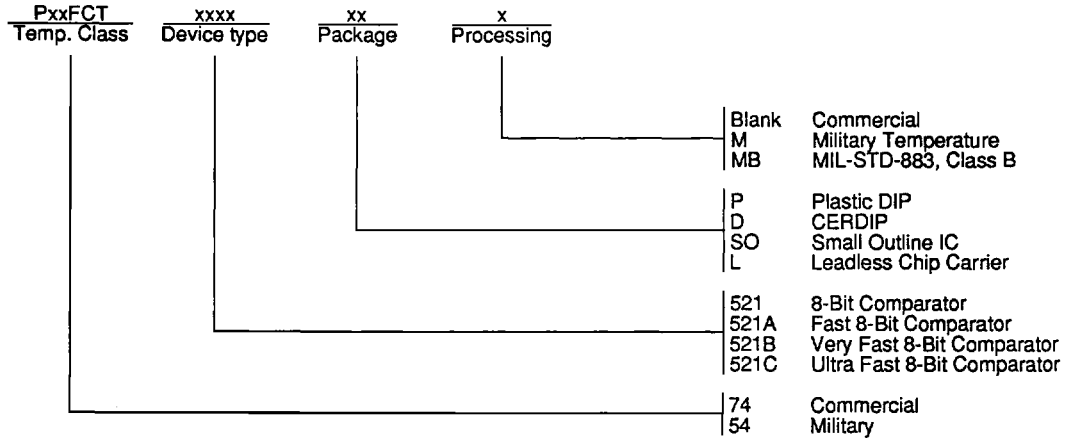
**Note:**
1. AC Characteristics guaranteed with $C_L$ = 50pF. Minimum limits are guaranteed but not tested on Propagation Delays.

## ORDERING INFORMATION

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