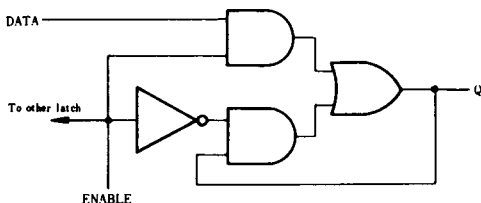


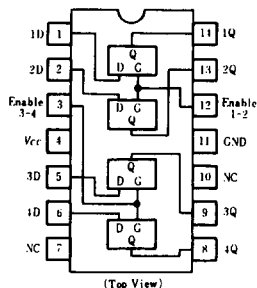
HD74LS77 ● 4-bit Bistable Latches

The HD74LS77 is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data(D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ FUNCTION TABLE

Inputs		Output
D	G	Q
L	H	L
H	H	H
X	L	Q ₀

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Pulse width	t_w	20	—	—	ns
Setup time	t_{sv}	20	—	—	ns
Hold time	t_h	5	—	—	ns

Notes) H; high level, L; low level, X; irrelevant
Q₀; level of Q before the indicated steady-state input conditions were established.

■ ELECTRICAL CHARACTERISTICS (T_a = -20 ~ +75°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V _{IH}		2.0	—	—	V
	V _{IL}		—	—	0.8	V
Output voltage	V _{OH}	V _{CC} = 4.75V, V _{IH} = 2V, V _{IL} = 0.8V, I _{OH} = -400μA	2.7	—	—	V
	V _{OL}	V _{CC} = 4.75V, V _{IH} = 2V, V _{IL} = 0.8V	—	—	0.4	V
		I _{OL} = 4mA	—	—	0.5	
Input current	D	V _{CC} = 5.25V, V _I = 2.7V	—	—	20	μA
	G		I _{IH}	—	—	
	D	V _{CC} = 5.25V, V _I = 0.4V	—	—	-0.4	mA
	G		I _{IL}	—	—	
	D	V _{CC} = 5.25V, V _I = 7V	—	—	0.1	mA
	G		I _I	—	—	
Short-circuit output current	I _{OS}	V _{CC} = 5.25V	-20	—	-100	mA
Supply current **	I _{CC}	V _{CC} = 5.25V	—	6.9	13	mA
Input clamp voltage	V _{IK}	V _{CC} = 4.75V, I _{IN} = -18mA	—	—	-1.5	V

* V_{CC} = 5V, T_a = 25°C

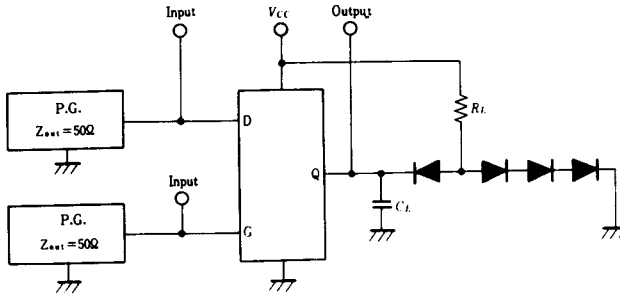
** I_{CC} is measured with all outputs open and all inputs grounded.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	D	Q	$C_L=15pF$ $R_L=2k\Omega$	—	11	19	ns
	t_{PHL}				—	9	17	
	t_{PLH}	G	Q		—	10	18	
	t_{PHL}				—	10	18	

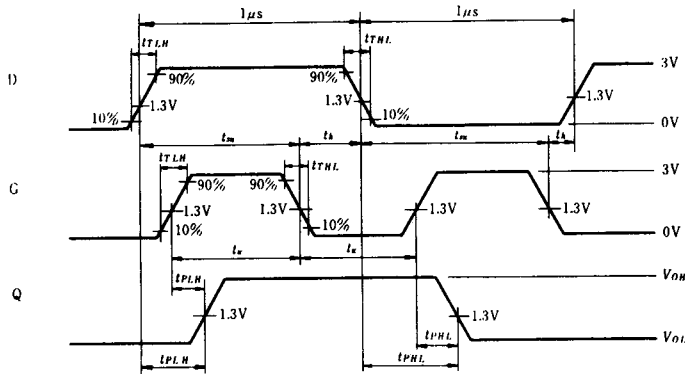
TESTING METHOD

1) Test Circuit



- Notes) 1. Test is put into each latch
 2. All diodes are 1S2074 (S)
 3. C_L includes probe and jig capacitance.

Waveform



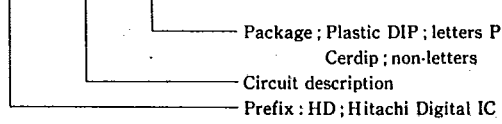
- Notes) 1. Input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$.
 2. When measuring propagation delay times from the D input, the corresponding G input must be held high.

PACKAGING INFORMATIONS

T-90-20

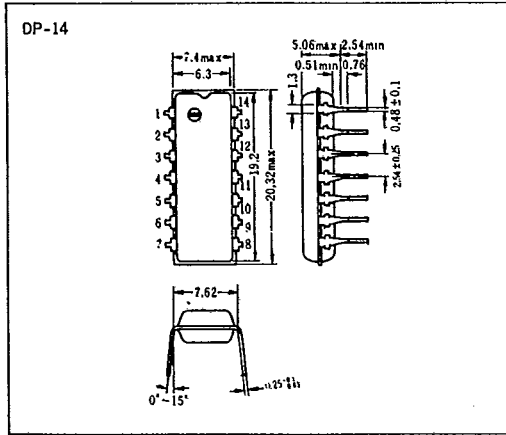
Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

HD 74LS00 P

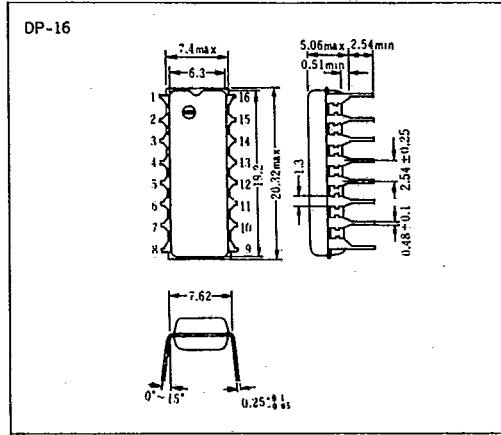


■ Plastic DIP

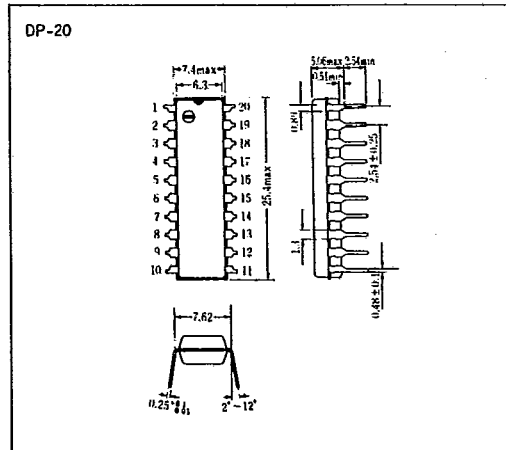
● 14 Pin



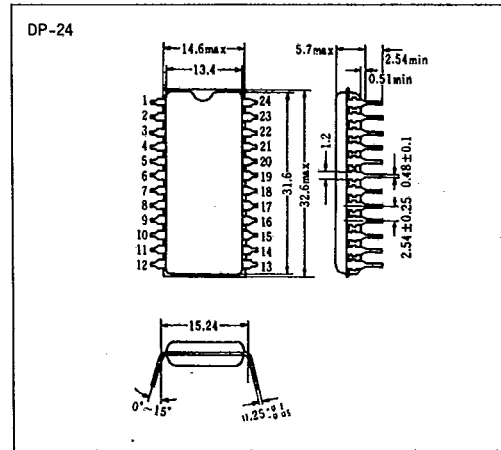
● 16 Pin



● 20 Pin



● 24 Pin

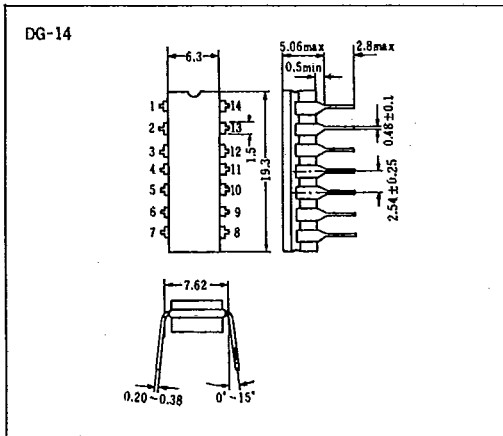


T-90-20

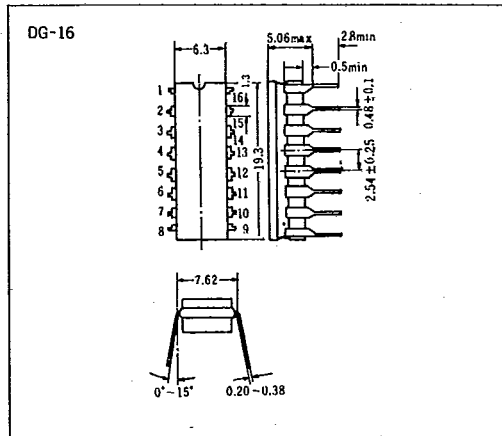
PACKAGING INFORMATIONS

■ Cerdip

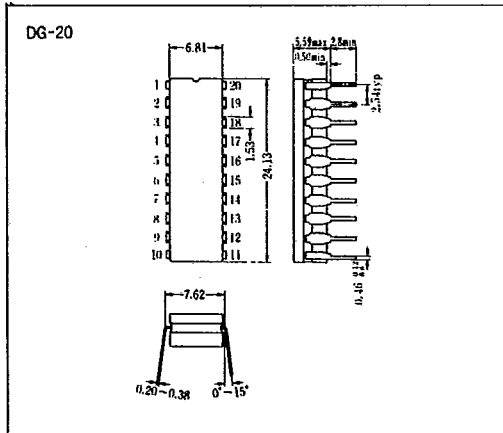
● 14 Pin



● 16 Pin



● 20 Pin



● 24 Pin

