

Low Voltage 1:2 Differential HSTL Clock Fanout Buffer

The MC100ES8011H is a low voltage 1:2 Differential HSTL fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8011H supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:2 differential clock fanout buffer
- 20 ps maximum device skew
- SiGe Technology
- Supports DC to 625 MHz operation
- HSTL compatible differential clock outputs
- HSTL compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 8 lead SOIC package
- 8-lead Pb-free package available

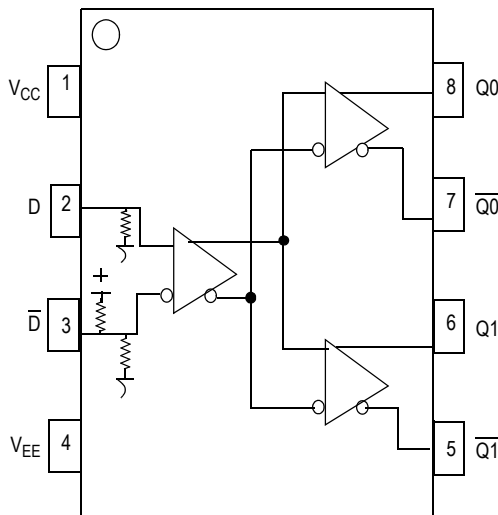


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

MC100ES8011H

1:2 DIFFERENTIAL HSTL CLOCK FANOUT DRIVER



D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-07



EF SUFFIX
8-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751-07

ORDERING INFORMATION

Device	Package
MC100ES8011HD	SO-8
MC100ES8011HDR2	SO-8
MC100ES8011HEF	SO-8 (Pb-Free)
MC100ES8011HEFR2	SO-8 (Pb-Free)

PIN DESCRIPTION

Pin	Function
D, \bar{D}	HSTL Data Inputs
Qn, \bar{Qn}	HSTL Data Outputs
V _{CC}	Positive Supply
V _{EE}	Negative Supply

Table 1. Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Conditions	Rating	Unit
V _{SUPPLY}	Power Supply Voltage	Difference between V _{CC} & V _{EE}	3.9	V
V _{IN}	Input Voltage	V _{CC} - V _{EE} ≤ 3.6V	V _{CC} + 0.3 V _{EE} - 0.3	V V
I _{OUT}	Output Current	Continuous Surge	50 100	mA mA
T _A	Operating Temperature Range		-40 to +85	°C
T _{STG}	Storage Temperature Range		-65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 2. DC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)⁽¹⁾

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (D, \bar{D})						
V _{DIF}	Differential Input Voltage ⁽²⁾	0.2			V	
V _{X, IN}	Differential Cross Point Voltage ⁽³⁾	0.25	0.68 - 0.9	V _{CC} - 1.3	V	
I _{IN}	Input Current			±150	mA	V _{IN} = V _X ± 0.1V
HSTL clock outputs (Q[0:1], \bar{Q} [0:1])						
V _{X, OUT}	Output Differential Crosspoint	0.68	0.75	0.9	V	
V _{OH}	Output High Voltage	1			V	
V _{OL}	Output Low Voltage			0.4	V	
Supply Current						
I _{CC}	Maximum Quiescent Supply Current without output termination current		80	105	mA	V _{CC} pin (core)

1. DC characteristics are design targets and pending characterization.

2. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.

3. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 3. AC Characteristics ($V_{CC} = 3.3\text{ V} \pm 5\%$; $T_J = 0^\circ\text{C}$ to 110°C)(1) (2)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (D, \overline{D})						
V_{DIF}	Differential Input Voltage (peak-to-peak) ⁽³⁾	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage ⁽⁴⁾	0.68		0.9	V	
f_{CLK}	Input Frequency			625	MHz	Differential
t_{PD}	Propagation Delay D to Q[0:1]	700	920	1200	ps	Differential
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Output Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	0.5			V	
$t_{SK(O)}$	Output-to-Output Skew			20	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			500	ps	Differential
$t_{SK(P)}$	Output Pulse Skew			100	ps	
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			1	ps	
t_r / t_f	Output Rise/Fall Times	150		800	ps	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
3. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.

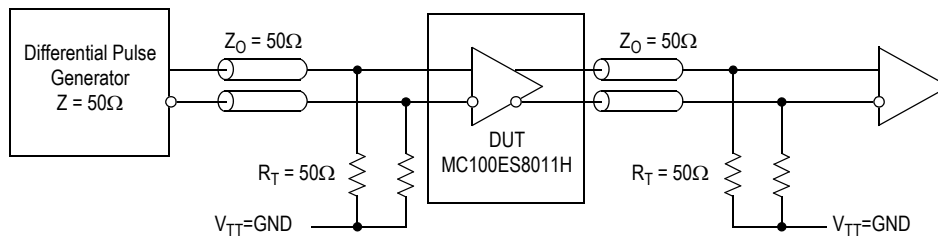


Figure 2. MC100ES8011H AC Test Reference

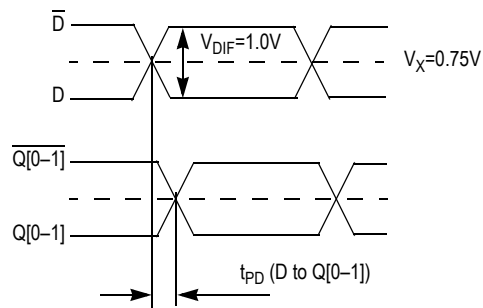
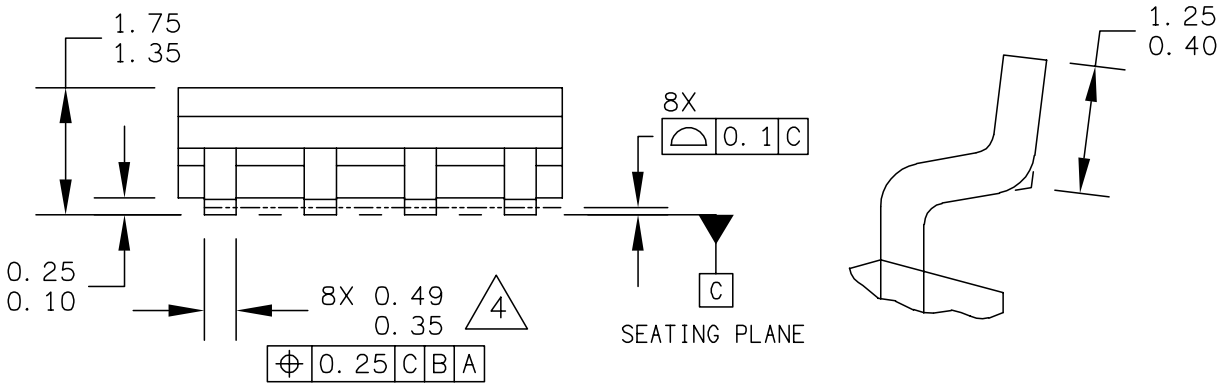
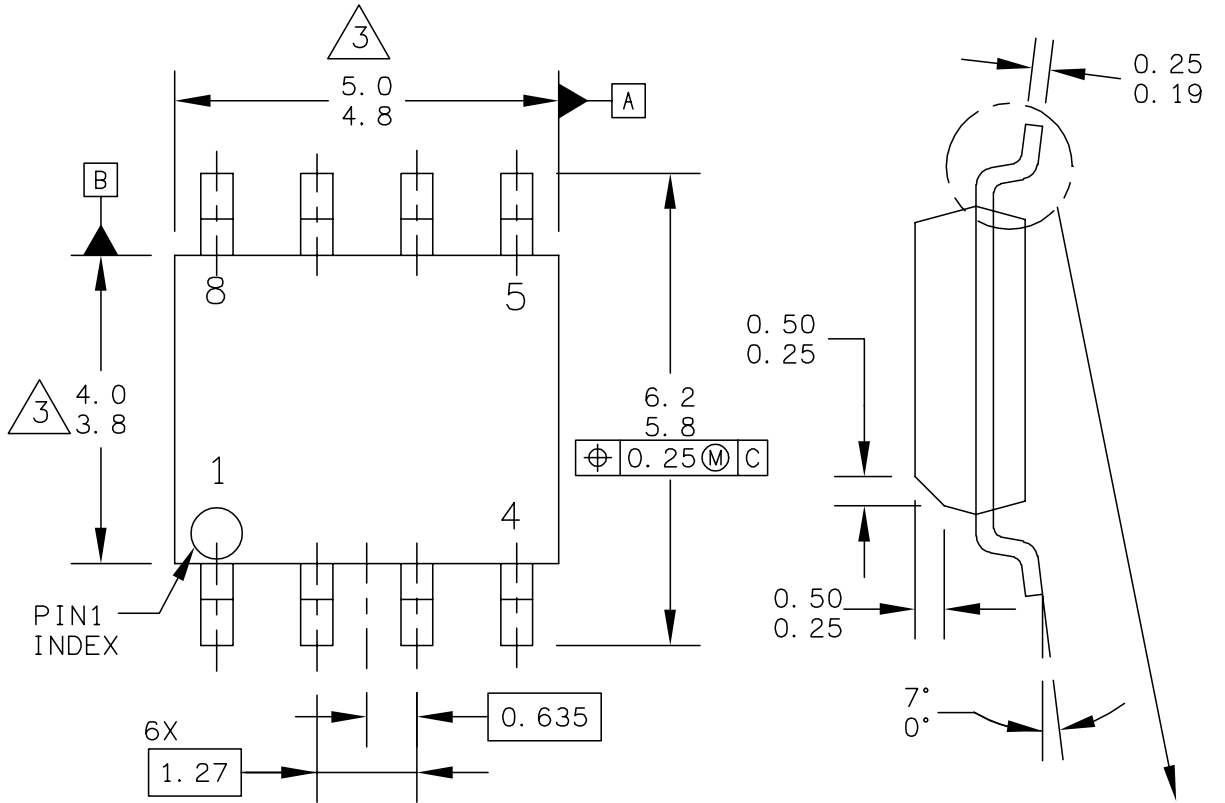


Figure 3. MC100ES8011H AC Reference Measurement Waveform (HSTL Input)

PACKAGE DIMENSIONS



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	CASE NUMBER: 751-07	07 APR 2005	
	STANDARD: JEDEC MS-012AA		

**CASE 751-07
ISSUE U
8-LEAD SOIC PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

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