



# SPECIFICATIONS

## ELECTRICAL

At +25°C, rated power supplies, 1.5µs conversion time, and after 6-minute warm-up unless otherwise noted.

MODEL	ADC806CM			ADC806BM			ADC806SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>RESOLUTION</b>			12			*			*	Bits
<b>INPUTS</b>										
<b>ANALOG</b> Voltage Ranges: Bipolar Unipolar Impedance: -10V to 0V, ±5V ±10V		±5, ±10 0 to -10 1.4 2.4			*			*		V V kΩ kΩ
<b>DIGITAL</b> Convert Command Logic Loading		Negative pulse 50ns wide (min) trailing edge (0 to 1) initiates conversion.								TTL Loads
<b>TRANSFER CHARACTERISTICS</b>										
<b>ACCURACY</b> Gain Error <sup>(1)</sup> Offset Error <sup>(1)</sup> : Unipolar Bipolar Linearity Error: 1.5µs Conversion Time 1.2µs Conversion Time <sup>(3)</sup> Differential Linearity Error: 1.5µs Conversion Time 1.2µs Conversion Time <sup>(3)</sup> Inherent Quantization Error		±0.04 ±0.05 ±0.02 ±0.009 ±0.012 ±0.012 ±0.012 1/2	±0.1 ±0.2 ±0.1 ±0.018 ±0.020 ±0.015 ±0.024		±0.08 ±0.07 * ±0.015 ±0.015 *	±0.2 ±0.3 ±0.2 ±0.020 ±0.020		*	*	% % of FSR <sup>(2)</sup> % of FSR % of FSR % of FSR % of FSR LSB
<b>POWER SUPPLY SENSITIVITY</b> Gain and Offset: +15VDC -15VDC +5VDC Conversion Time: +15VDC -15VDC +5VDC		±0.0036 ±0.0005 ±0.001 ±0.7 None ±0.8			*	*		*	*	% of FSR/%V <sub>CC</sub> % of FSR/%V <sub>CC</sub> % of FSR/%V <sub>DD</sub> %/V <sub>CC</sub> %/V <sub>CC</sub> %/V <sub>DD</sub>
<b>CONVERSION TIME</b> Factory Set Range of Adjustments <sup>(4)</sup>	1.3 0.8		1.5 2.2	*		*	*	*	*	µs µs
<b>DRIFT</b> Gain Offset: Unipolar Bipolar Linearity Error -25°C to +85°C: 1.5µs Conversion Time 1.2µs Conversion Time -55°C to +125°C: 1.7µs Conversion Time, max. <sup>(5)</sup> Differential Linearity Error -25°C to +85°C: 1.5µs Conversion Time 1.2µs Conversion Time -55°C to +125°C: 1.7µs Conversion Time, max. <sup>(5)</sup> Conversion Time No Missing Code Temp. Range: 1.5µs Conversion Time 1.7µs Conversion Time, max. <sup>(5)</sup>		±10 ±2 ±3 ±0.012 ±0.015 ±0.012 ±0.015 ±0.1	±30 ±7 ±10 ±0.018 ±0.020 ±0.018 ±0.024 ±0.024 ±0.1		±15 ±3 ±5 ±0.020 ±0.024 *	*		*	*	ppm/°C ppm of FSR/°C ppm of FSR/°C % of FSR % of FSR % of FSR % of FSR % of FSR % of FSR °C °C
<b>OUTPUT</b>										
<b>DIGITAL DATA</b> Parallel Output Codes: Unipolar Bipolar Output Drive Serial Data Codes (NRZ) Output Drive Status Status Output Drive Internal Clock: Clock Output Drive Frequency (without external clock adjustment)		Complementary Straight Binary Bipolar Offset Binary 6     Same as Parallel (MSB first) 6     Logic "1" during Conversion 6     3     8				*	*	*	*	TTL Loads TTL Loads TTL Loads TTL Loads MHz

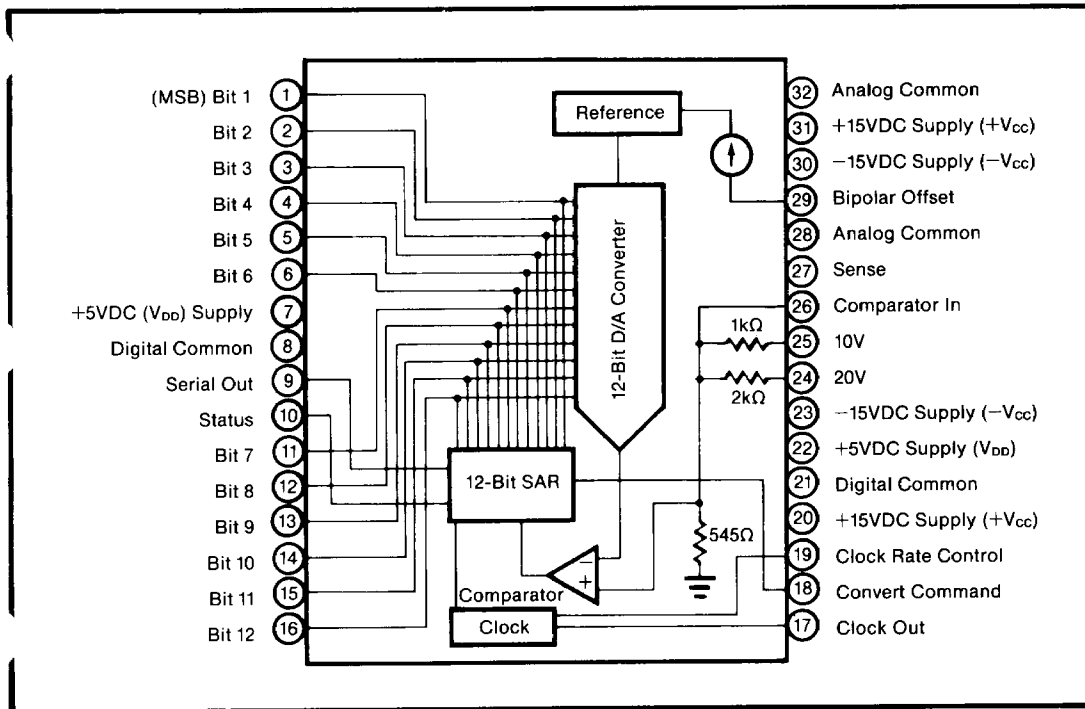
## ELECTRICAL (CONT)

MODEL	ADC806CM			ADC806BM			ADC806SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>POWER SUPPLY REQUIREMENTS</b>										
Power Consumption		1.3		*	*		*	*	*	W
Rated Voltage: Analog ( $\pm V_{CC}$ )	$\pm 14.25$	$\pm 15.0$	$\pm 15.75$	*	*	*	*	*	*	VDC
Digital ( $V_{DD}$ )	+4.75	+5.0	+5.25	*	*	*	*	*	*	VDC
Supply Drain: +15V		13	16		*	*		*	*	mA
-15V		40	58		*	*		*	*	mA
+5V		110	125		*	*		*	*	mA
<b>TEMPERATURE RANGE (AMBIENT)</b>										
Specification	-25		+85	*		*	-55		+125	°C
Storage	-65		+150	*		*	*		*	°C

\*Same specification as for ADC806CM.

NOTES: (1) Adjustable to zero. See Optional Gain and Offset Adjustment section. (2) FSR means Full-Scale Range. For example, unit connected for  $\pm 10V$  has 20V FSR. (3) When adjusted for  $1.2\mu s$  conversions, we guarantee no missing codes at  $+25^\circ C$ . (4) See Optional Clock Rate Control section. For faster conversion time at less resolution, see section on External Short Cycle. (5) Conversion time is factory-set at approximately  $1.5\mu s$  at  $+25^\circ C$ . As temperature increases, the conversion time increases. At  $+125^\circ C$  the conversion time will be no more than  $1.7\mu s$ . No Missing Codes is guaranteed over  $-55^\circ C$  to  $+125^\circ C$  provided the conversion time is allowed to increase with temperature.

## CONNECTION DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

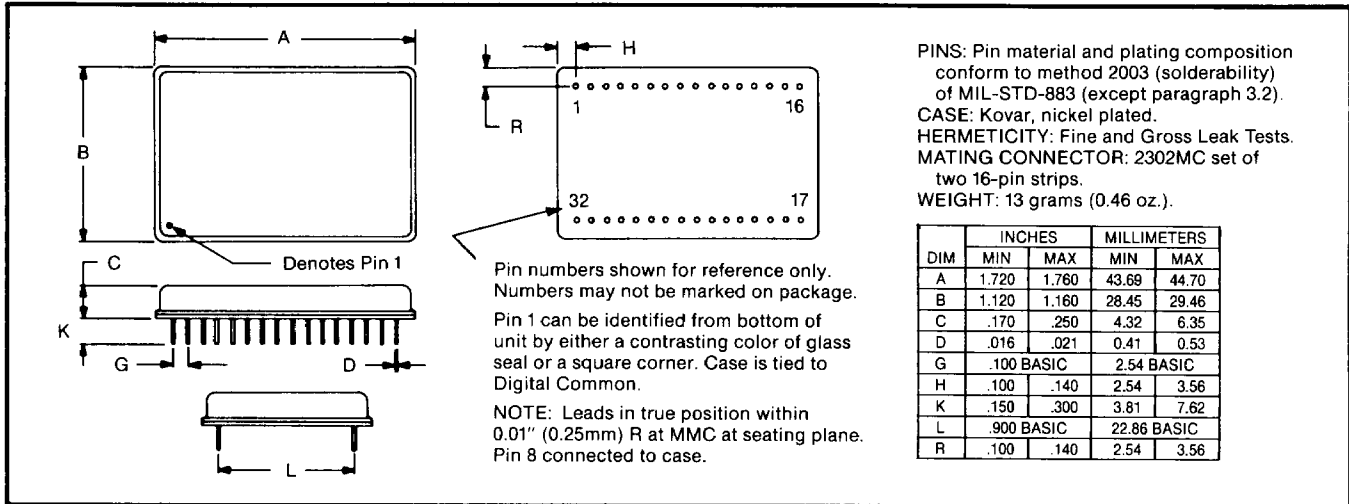
Analog Supply Voltage to Analog Common	$\pm 18V$
Digital Supply Voltage to Digital Common	$+7V$
Digital Controls Inputs	$+5.5V$
Analog Inputs	$\pm 15V$
Operating Temperature: Ambient	$+125^\circ C$
Case	$+135^\circ C$
Storage Temperature	$+125^\circ C$

## ORDERING INFORMATION

Basic Model Number	ADC806	X	M	Q
Performance Grade Code				
B, C:	$-25^\circ C$ to $+85^\circ C$			
S:	$-55^\circ C$ to $+125^\circ C$			
Package Code				
M:	Metal DIP			
Reliability Screening				
Q:	Q-Screened			

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## MECHANICAL



## THEORY OF OPERATION

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of  $\pm 1/2\text{LSB}$ . The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the transfer function (Figure 1) about the zero point and Offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is not adjustable. Differential Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of  $\pm 1/2\text{LSB}$  means that the width of each bit step over the range of

the A/D converter is  $1\text{LSB}$ ,  $\pm 1/2\text{LSB}$ . The ADC806 is guaranteed to have no missing codes over the specified temperature range.

## TIMING CONSIDERATIONS

The timing diagram (Figure 2) shows the relationship between the convert command, clock and outputs. The digital output word is positive true logic for bipolar operation and complementary logic for unipolar operation.

The following are some important notes on the ADC806 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 2.

1. When power is first applied, the status of the ADC806 will be undetermined. A CONVERT COMMAND must be applied to initialize the ADC806.
2. The CONVERT COMMAND must be low at least 30ns prior to the "0" to "1" edge that starts a conversion.
3. The clock runs continuously when the initial CONVERT COMMAND goes high and whenever the CONVERT COMMAND is high thereafter. It does not run when CONVERT COMMAND is low. It may be beneficial to keep CONVERT COMMAND low except during conversions to limit the digital noise induced in the ground and power supply lines.
4. The clock starts 15ns after the "0" to "1" transition of the CONVERT COMMAND.
5. **Parallel Output Data:** The Successive Approximation Register (SAR) is reset 13ns after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 2. Each bit will be valid 11ns after its corresponding clock pulse.

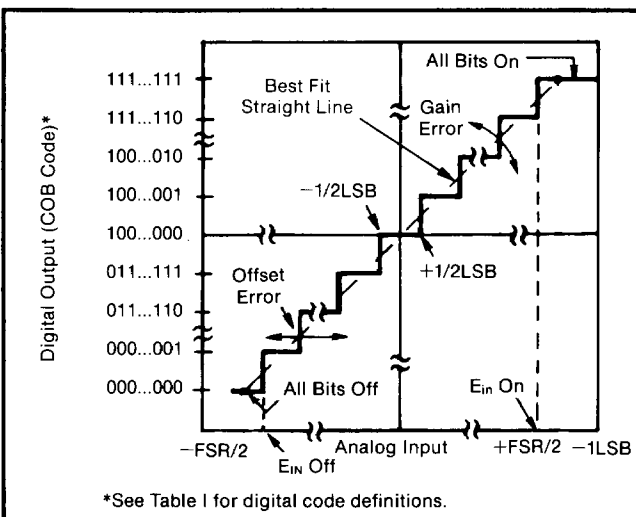


FIGURE 1. Input Versus Output for an Ideal Bipolar A/D Converter.

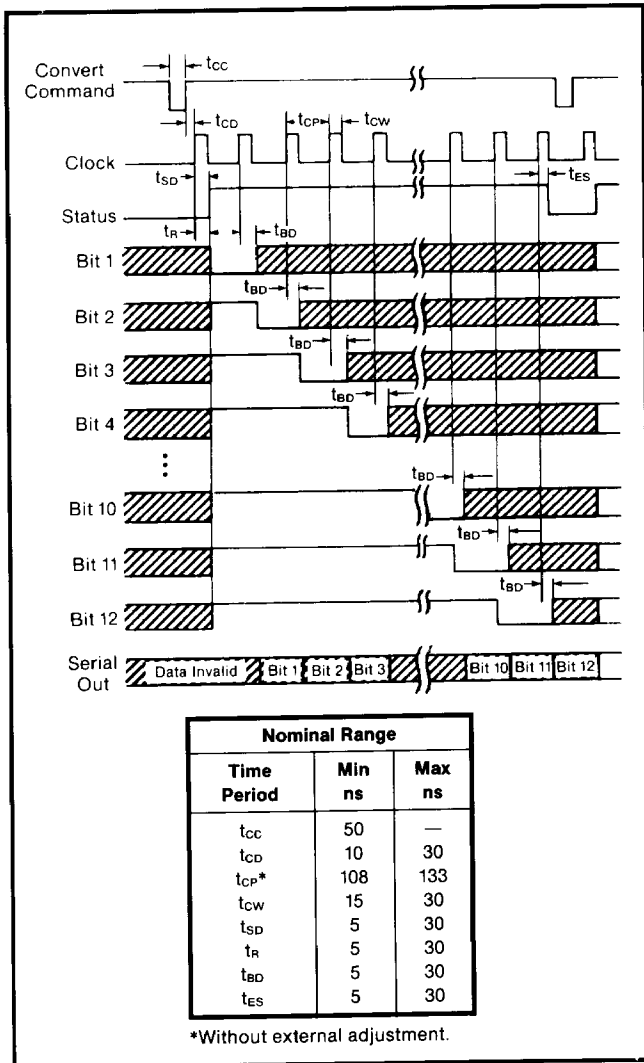


FIGURE 2. ADC806 Timing Diagram.

- Serial Output Data:** The serial output is indeterminate until Bit 1 is valid, which occurs 13ns after the leading edge of the second clock pulse. The remaining bits (Bits 2 through 12) are valid in succession for one clock period each beginning 13ns after the leading edge of each clock pulse.
- STATUS goes high 13ns after the leading edge of the first clock pulse and goes low 11ns after the leading edge of the last clock pulse.
- Bit 12 will become valid at about the same time STATUS goes low and a new conversion can be initiated at any time after the output data has been read.
- The converter may be restarted during a conversion. When CONVERT COMMAND makes a "0" to "1" transition after the minimum set-up time, the SAR will be reset and a new conversion will start regardless of the state of the converter prior to the CONVERT COMMAND being received.

Figures 3, 4, and 5 are photographs of the actual pulse shapes and relationships.

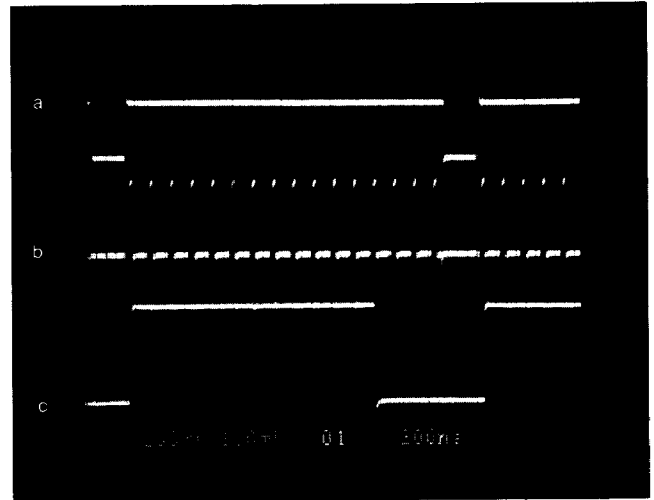


FIGURE 3. Photo of (a) Convert Command, (b) Clock, and (c) Status (200ns/div).

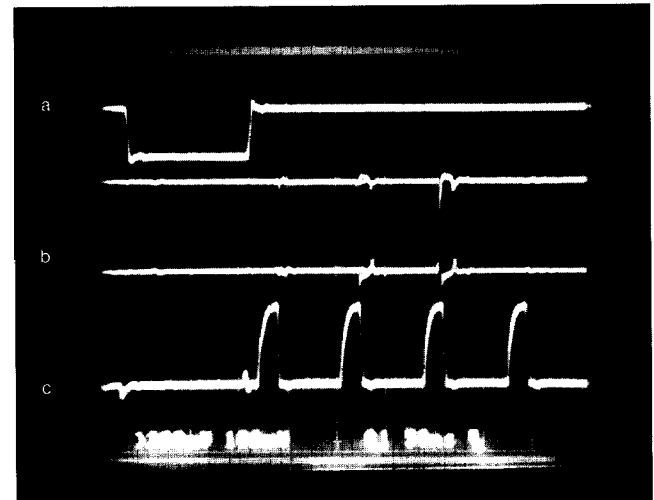


FIGURE 4. Photo of (a) Convert Command, (b) Serial Out, and (c) Clock (50ns/div).

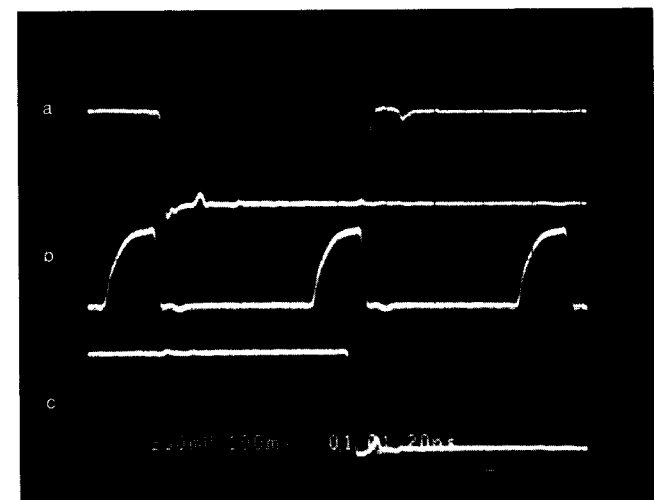


FIGURE 5. Photo of (a) Bit 12 Data, (b) Clock, and (c) Status (20ns/div).

## DIGITAL CODES

### Parallel Data

Two binary codes are available on the ADC806 parallel output: complementary straight binary (Logic "0" true) for unipolar input signal ranges, and bipolar offset binary (Logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges,  $-10V$  is full scale.

Table I shows the LSB, transition values, and code definitions for each possible analog signal range.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Analog Input Voltage Range	$\pm 10V$	$\pm 5V$	0 to $-10V$
Code Designation	BOB <sup>(1)</sup> or BTC <sup>(2)</sup>	BOB or BTC	CSB <sup>(3)</sup>
One Least Significant Bit (LSB)	4.88mV	2.44mV	2.44mV
Transition Values MSB LSB <sup>(4)</sup>			
000...000	$-10V + 1/2LSB$	$-5V + 1/2LSB$	$-10V + 3/2LSB$
000...001			
011...111	$-1/2LSB$	$-1/2LSB$	$-5V + 1/2LSB$
100...000			
111...110	$+10V - 3/2LSB$	$+5V - 3/2LSB$	$-1/2LSB$
111...111			

NOTES: (1) BOB = Bipolar Offset Binary. (2) BTC = Binary Two's Complement (obtained by inverting the most significant bit, pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for the transition from the next lower code.

### Serial Data (NRZ)

Two binary codes are available on the serial output line: complementary straight binary (CSB) for unipolar input ranges, and bipolar offset binary (BOB) for bipolar input signal ranges. The serial data is available only during conversion and appears with the MSB first. See the timing diagram and discussion under Timing Considerations for more detailed information.

The LSB and transition values shown in Table I also apply to the serial data output, except serial output does not have a BTC code.

## DISCUSSION OF SPECIFICATIONS

The ADC806 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are Linearity, Drift, Gain and Offset errors, and Conversion speed effects on accuracy. These ADCs are factory-trimmed and tested for all critical specifications.

### GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10, 11, and 12.

## ACCURACY VERSUS CONVERSION TIME

The conversion time of the ADC806 can be adjusted by an external circuit (see Optional Clock Rate Control) but some linearity degradation will result from increased clock speed. Typical ADC806 performance is illustrated in Figure 6.

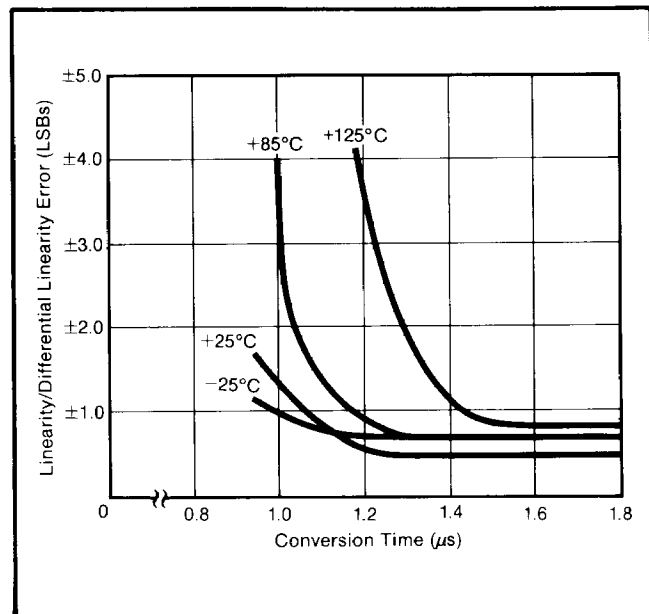


FIGURE 6. Linearity and Differential Linearity Error Versus Conversion Time.

### POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy so regulated power supplies with  $\leq 1\%$  ripple are recommended. See Layout Precautions, Power Supply Decoupling, and Figure 7. Switching power supplies may cause high frequency noise and should be used with caution.

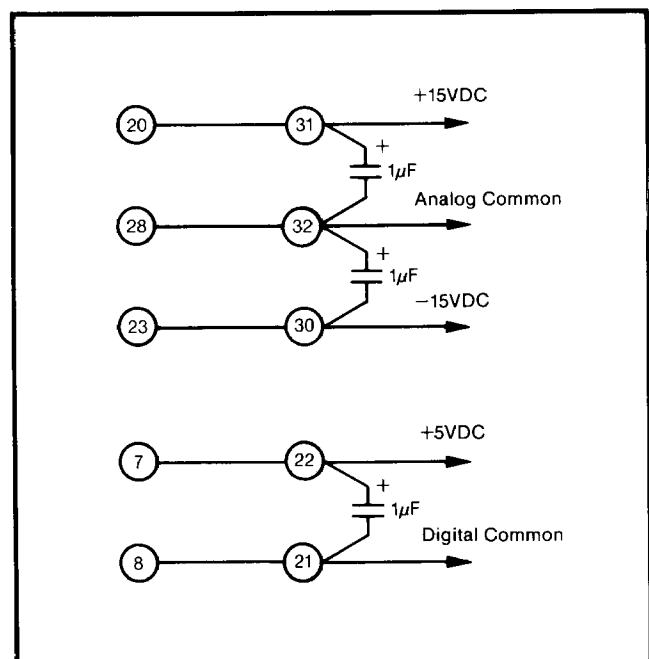


FIGURE 7. Recommended Power Supply Decoupling.

## LINEARITY ERROR

Linearity is the deviation of an actual bit transition from best fit straight line value at any level over the range of the A/D converter.

## DIFFERENTIAL LINEARITY ERROR

Differential Linearity describes the step size between transition values. A Differential Linearity error of  $\pm 1/2\text{LSB}$  indicates that the size of any step may not vary from 1LSB by more than  $\pm 1/2\text{LSB}$ .

## ENVIRONMENTAL SCREENING

High-reliability Q screening is now available for the ADC806. The Q-screened versions have the same specifications as the unscreened versions listed in the Specifications table.

### Q Screening

Burr-Brown Q-screened models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any method of MIL-STD-883 other than those listed below. Burr-Brown's detailed procedures may vary slightly from those of MIL-STD-883.

### ENVIRONMENTAL SCREENING

Screen	Method Burr-Brown or MIL-STD-883	Condition
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008	B (150°C, 24hr)
Temperature Cycling	1010	B (10cy, -55°C to +125°C)
Constant Acceleration	2001	2000G (Y1 axis)
Burn-in ADC806BMQ, CMQ ADC806SMQ	1015	D (160hrs, +85°C) (160 hrs, +125°C)
Electrical Test	Burr-Brown Test Specification	
Hermeticity Fine Leak	1014	A1 or A2 (Helium, $5 \times 10^{-7}$ cc/sec)
Gross Leak	1014	C
Final Electrical	Burr-Brown Test Specification	
External Visual	Burr-Brown QC5150	

# LAYOUT AND OPERATING INSTRUCTIONS

## LAYOUT PRECAUTIONS

The ADC806 is a high-speed analog-to-digital converter which requires more layout precautions than general purpose products.

The ADC806 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC806, but should be connected together externally to a ground plane.

Connecting all commons to a ground plane at the ADC806 is the best method to minimize noise and dissipate heat. Pin 8 (Digital Common) is internally connected to the case.

The ADC806 also has an analog common Sense input (pin 27) for the analog input. This Sense pin must be connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

The Comparator input (pin 26) and Clock Rate Control (pin 19) are extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by the ground plane, analog common, or  $\pm 15\text{VDC}$  supply printed circuit patterns. The Clock Output (pin 17) is sensitive to stray capacitance; capacitance on this pin could alter the clock wave shape.

## POWER SUPPLY DECOUPLING

The power supplies should be bypassed with  $1\mu\text{F}$  tantalum capacitors as shown in Figure 7 to obtain noise-free operation. These capacitors should be located close to the ADC.

## INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signals as shown in Table II. See Figure 8 for circuit details.

## OUTPUT DRIVE

All ADC806 outputs except the clock will drive two TTL loads; the clock will drive three TTL loads. If long digital lines must be driven, external logic buffers are required—particularly for the clock, which is sensitive to capacitive loading.

TABLE II. ADC806 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 29 To	With Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	40Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to -10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal

\*Obtained by inverting MSB (pin 1) externally.

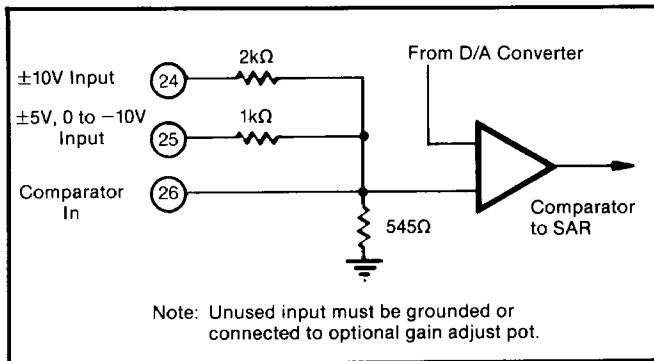


FIGURE 8. Input Scaling Circuit.

**INPUT IMPEDANCE**

The source impedance to the ADC806 should be low, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC806.

If this impedance is not low, a buffer amplifier should be added between the input signal and the ADC806 input as shown in Figure 9.

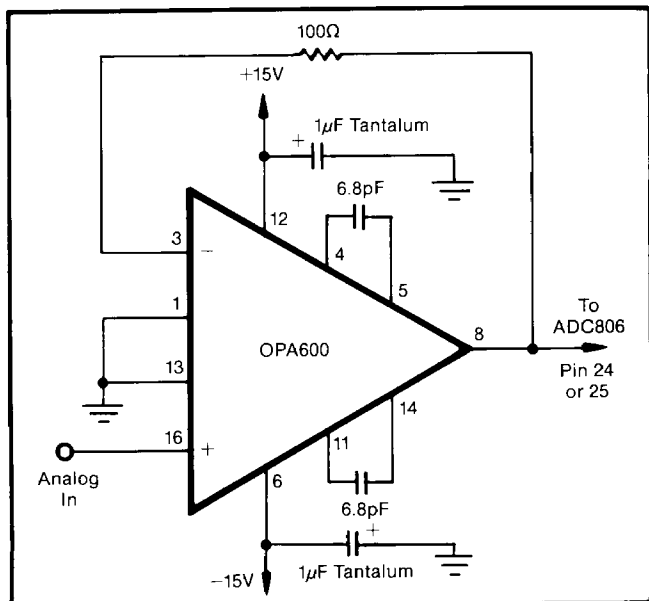


FIGURE 9. Source Impedance Buffering.

A common problem with successive approximation A/D converters is the transients in input current caused by the comparator input being switched back and forth. This requires a fast settling amplifier to drive the input.

The ADC806 comparator is connected in a differential mode (see Figure 8), greatly reducing the size of the input transients. The user, therefore, may use a fast-settling wideband operational amplifier to drive the ADC806. The small signal settling time of the amplifier should be less than 150ns.

**OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS**

Gain and Offset errors may be trimmed to zero using external trim potentiometers connected to the ADC as shown in Figure 10, 11, and 12. For proper gain adjust range, a series resistor must be connected to the analog input pin as specified in Table II and shown in Figures 11 and 12. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. All resistors should be ±1% metal film or better. If the Offset adjust is not used, pin 26 should be left open. If the Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

**Adjustment Procedure**

Refer to Table I for LSB voltages and transition values.

Unipolar Offset—Connect the offset potentiometer and resistors as shown in Figure 10. Sweep the input through the end point transition voltage, from 111...110 to 111...111. Adjust the Offset potentiometer until the actual end point transition voltage occurs at -1/2LSB.

Bipolar Offset—Connect the offset potentiometer and resistors as shown in Figure 10-. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 1111 to 1000 0000 0000 occurs at -1/2LSB.

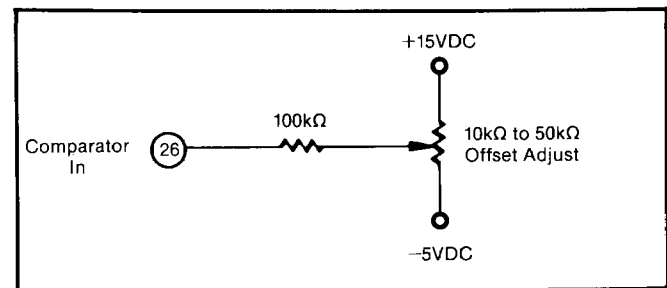


FIGURE 10. Optional Offset Adjust.

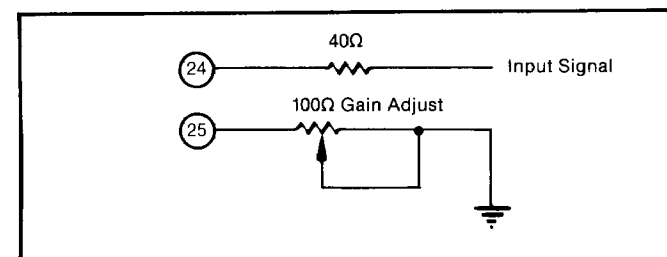


FIGURE 11. Optional Gain Adjust for ±10V Bipolar Operation.

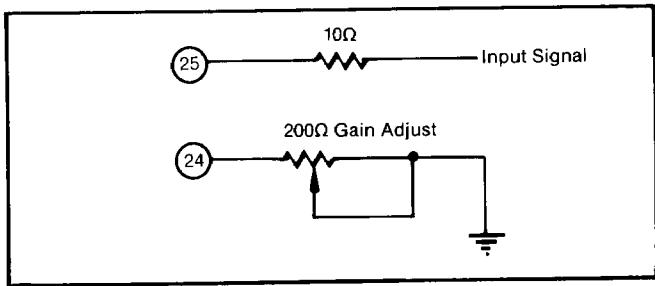


FIGURE 12. Optional Gain Adjust for  $\pm 5V$  Bipolar or 0 to  $-10V$  Unipolar Operation.

Gain—Connect the Gain potentiometer as shown in Figure 11 or 12. Sweep the input through the end point transition voltage that should cause an output transition from 000...000 to 000...001. Adjust the Gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table I.

### OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between  $1.3\mu s$  and  $1.5\mu s$ . By use of the optional Clock Rate Control as shown in Figure 13, the conversion time can be adjusted down to  $1.2\mu s$  for 12-bit resolution. If the optional Clock Rate Control is not used, pin 19 should be shielded from noise pickup. Figure 14 shows Conversion Time versus Clock Rate Control Voltage and Figure 6 shows Differential Linearity Error versus Conversion Time.

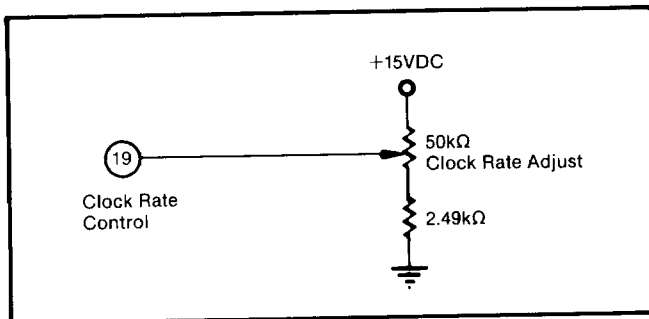


FIGURE 13. Optional Clock Rate Control.

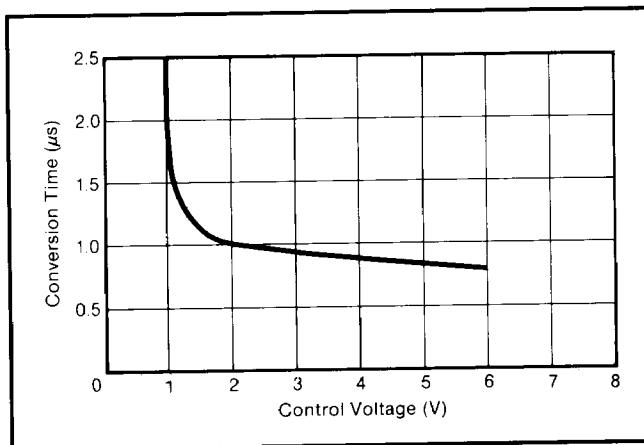


FIGURE 14. Typical Conversion Time versus Clock Rate Control Voltage.

### POWER DISSIPATION

The ADC806 dissipates approximately 1.3W (typical) and the package has a case-to-ambient thermal resistance ( $\theta_{CA}$ ) of  $25^{\circ}C/W$ . For operation above  $+85^{\circ}C$ ,  $\theta_{CA}$  should be lowered by a heat sink or by forced air over the surface of the package. See Figure 15 for  $\theta_{CA}$  requirements above  $+85^{\circ}C$ . Improved thermal contact with the PC card copper ground plane under the case can be achieved using a silicone heat sink compound.

### EXTERNAL SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the ADC806 can be shortened with the addition of two external components as shown in Figure 16. This circuit will create a shortened status signal directly proportional to the reduction of resolution. For  $n$  bits of resolution, the  $n+1$  bit is used to create the falling edge of the shortened status signal. It is possible to obtain the equivalent of a 10-bit converter with 800ns conversion time using this short-cycle technique and the external clock rate control shown in Figure 13. To begin a new conversion, simply give the converter a new convert command pulse. The SAR will reset and a new conversion will begin.

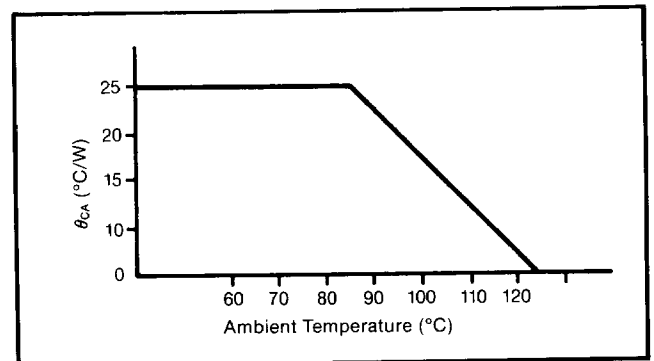


FIGURE 15.  $\theta_{CA}$  Requirement Above  $+85^{\circ}C$ .

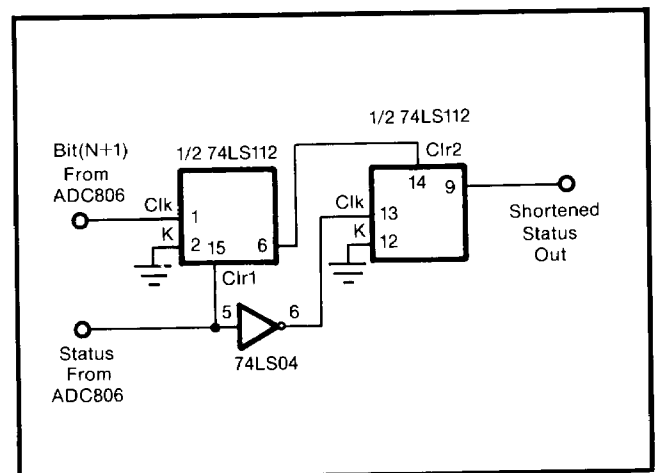


FIGURE 16. External Short Cycle Circuit.

## TESTING THE ADC806

In order to validate the test results of the ADC806 obtained during final test, the customer must take extreme care in the design and layout of test fixtures. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results.

### Analog Ground, Digital Ground, Sense

Figure 17 shows a simplified model of the ADC depicting proper analog and digital grounding. Several analog and digital ground pins have been provided to allow for optimizing the internal layout of the ADC. As will be explained in more detail later, analog and digital grounds should be connected together only at one point by an extremely low resistive and inductive connection (a ground plane is ideal). A special analog ground called "sense" has been provided to eliminate the voltage drop that would otherwise be in the ground return of the R-2R ladder. Measuring the input signal with respect to the sense terminal makes the measurement independent of the impedance that is developed in the connection between the sense terminal and the analog ground, pin 28.

### Analog-to-Digital Converter Test Technique

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." The block diagram of this technique is shown in Figure 18. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. The computer is programmed to place the desired code on the I/O bus which is one set of inputs to the digital comparator. The other set of inputs to this comparator is the digital output of the ADC. Depending upon the result of this comparison, the integrator is directed to change its output until an equilibrium state is achieved. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via

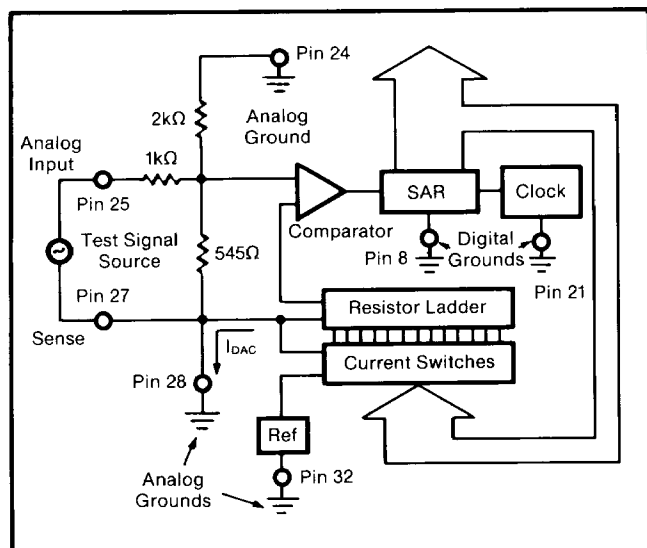


FIGURE 17. Simplified Model of ADC806 Depicting Proper Analog and Digital Ground.

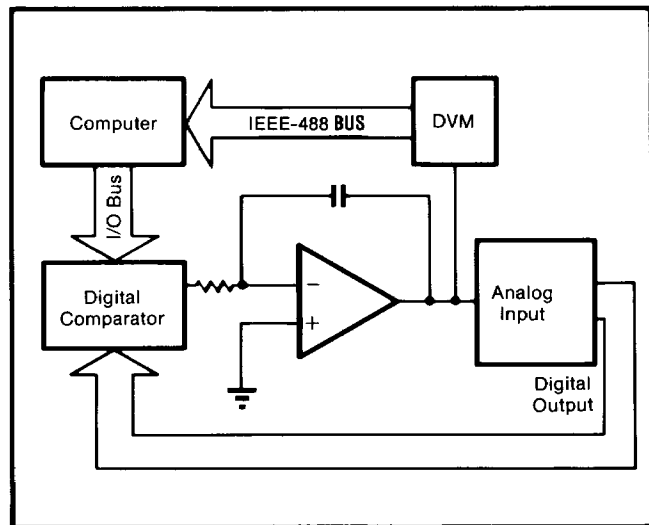


FIGURE 18. Servo Loop Analog-to-Digital Tester.

the IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

### Ground Loops

Figure 19 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit in Figure 19 shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit—in this case, the test signal generator (analog) and the digital circuitry that detect the ADC code which corresponds to the analog signal (digital). The ground loop exists when the digital ground connection between the ADC and the tester is in parallel with the analog grounds that connect the tester with the ADC. When the connection is made in this manner, some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysteresis. The error can be substantially reduced if the analog and digital grounds are isolated from each other in the ADC test system.

### Beat Frequency Test

A "beat frequency test" applied to an ADC806 with a companion sample/hold is an effective means of testing the high-frequency performance of such a system and demonstrates that the ADC806 with its associated sample/hold are capable of digitizing high-frequency signals cleanly. A sample/hold must be used when performing this test to hold the input of the ADC806 constant during the conversion time. Figure 20 is a block diagram of the beat frequency test setup.

The beat frequency test is useful for being able to rapidly determine whether there are any serious problems with the ADC. In this test the input frequency is set at slightly

less than one-half the sampling rate. The slight difference is selected to allow the sample point to vary by 1SLB, or less, on successive samples. The data is clocked into a low frequency reconstruction DAC at one-half the sampling rate to enable viewing on an oscilloscope. Figure 21 is a photograph of the response to a full-scale input sine wave centered around the MSB and Figure 22 is a photograph of a small signal sine wave centered around the MSB. For comparison, a photograph (Figure

23) is included which shows the response of the ADC806 to a 125Hz input signal which is the same as the beat frequency.

Figure 24 is the PC card layout that was used for the beat frequency test. This layout demonstrates some of the layout practices that must be followed when using a high-speed ADC such as an ADC806.

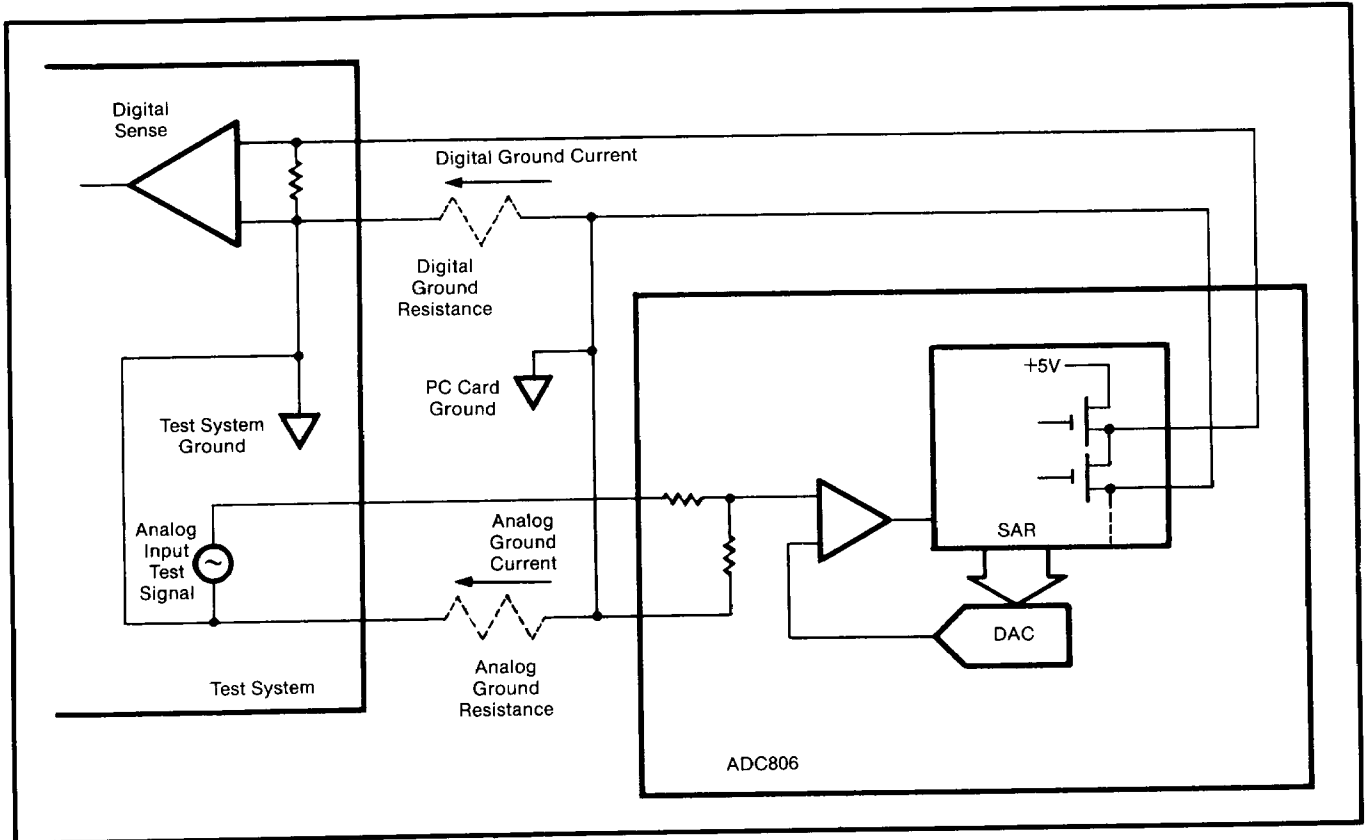


FIGURE 19. Ground loop Interaction Between Analog and Digital Grounds When ADC is Connected Into Test Circuit.

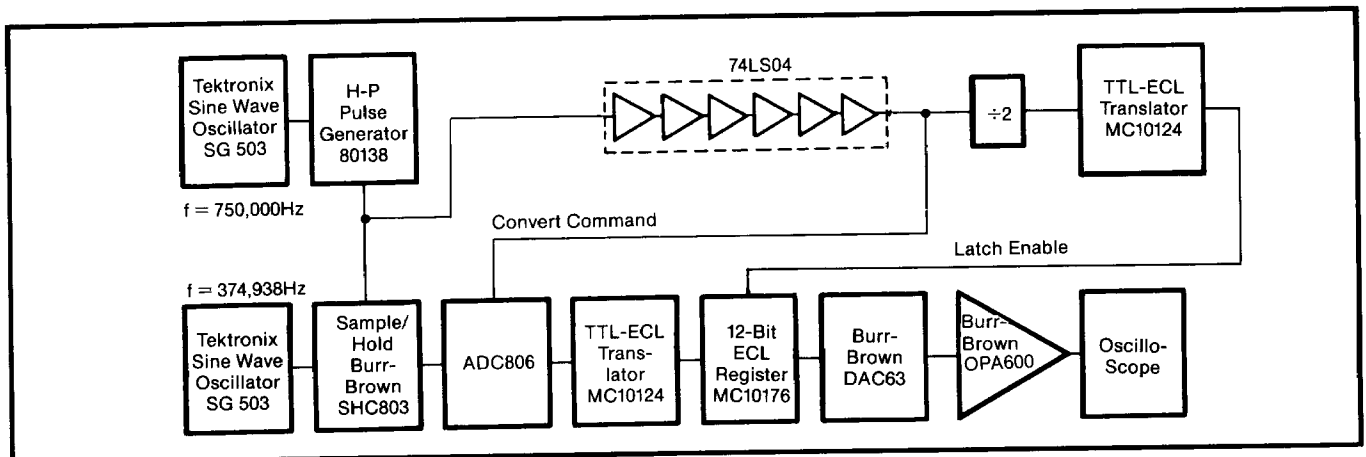
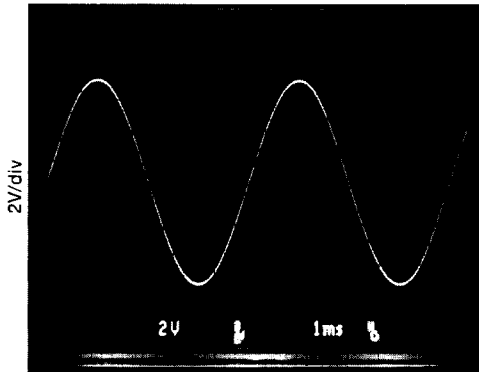
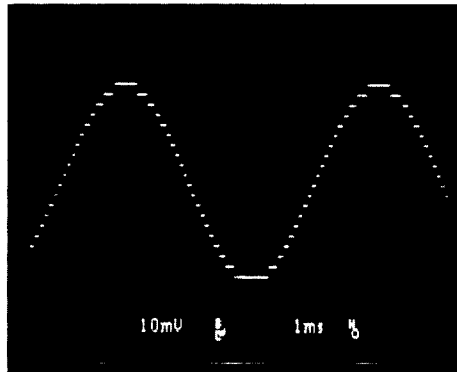


FIGURE 20. Block Diagram of Beat Frequency Test Circuit.



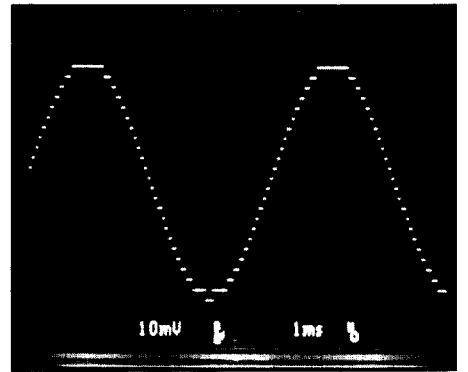
1ms/div

FIGURE 21. Beat Frequency Test Response of Full Scale Sine Wave Input.



1ms/div

FIGURE 22. Beat Frequency Test Response of Small Scale Sine Wave Input.



1ms/div

FIGURE 23. Response of Small Signal 125Hz Sine Wave Input.

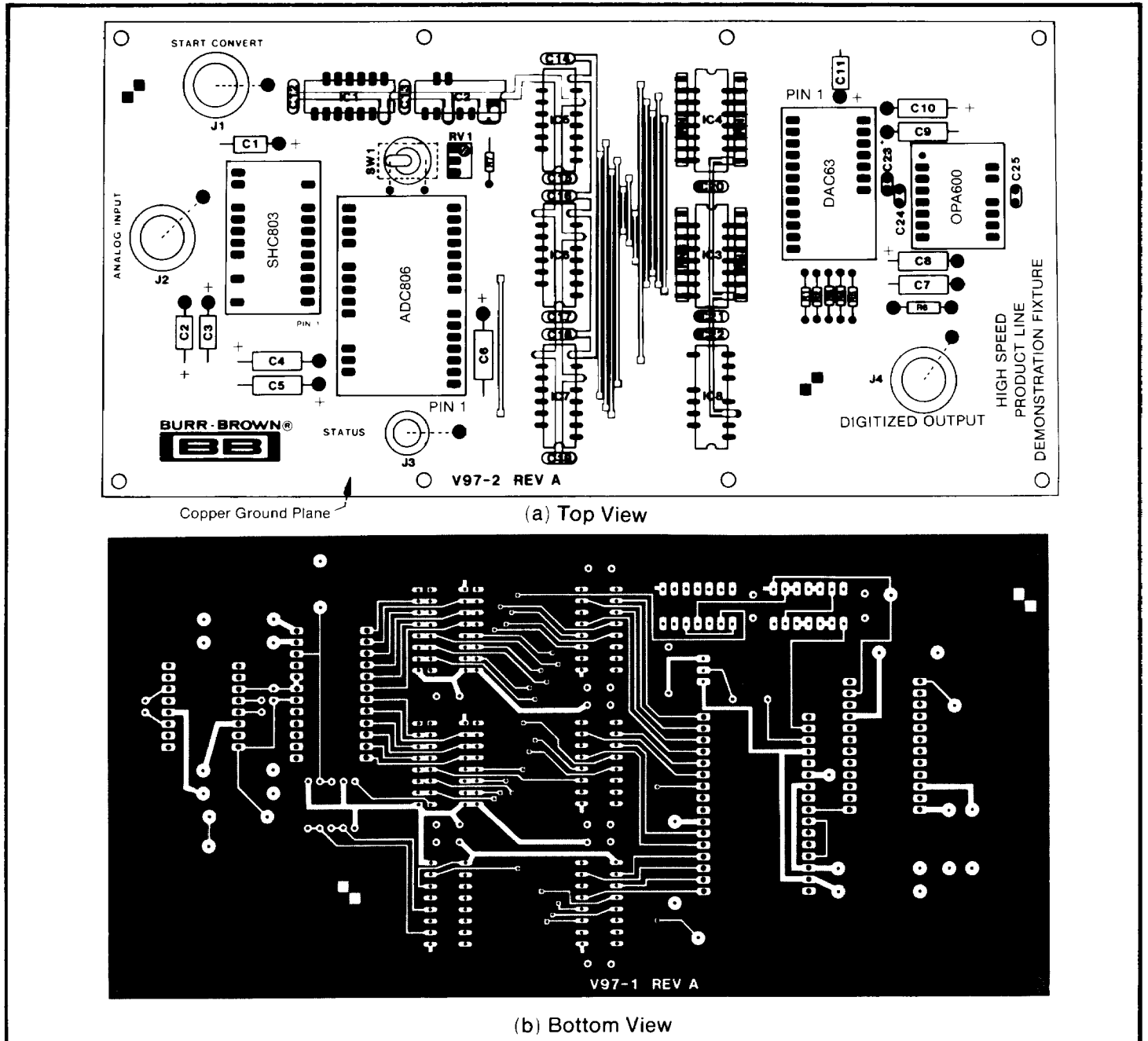


FIGURE 24. PC Board Layout for Beat Frequency Test Fixture.

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