FAIRCHILD
A Schlumberger Company

16P8A, 16RP8A, 16RP6A, 16RP4A Programmable Logic Array

September 1986 PRELIMINARY INFORMATION

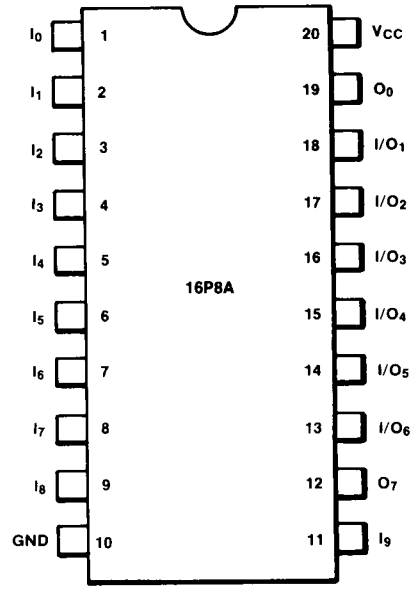
Memory & High Speed Logic

Description

The FASTPLA 16P8A Series of high-performance bipolar programmable logic arrays provide 25 ns maximum propagation delays and are fully compatible with industry standard medium 20-pin PAL® devices. Designed to enhance the flexibility of the FAST family, FASTPLA 16P8A Series offers advanced architectural features including programmable ouput polarity, power-up reset, and power-up three-state. The devices are designed for full AC/DC testability and are manufactured with Fairchild's highly reliable Isoplanar-Z vertical-fuse tecnology.

- **Extension of FAST Product Line**
- **25 ns Maximum Propagation Delays (T_C = 0°C to +75°C)**
- **180 mA Maximum I_{CC} Current**
- **Fully Compatible with Medium 20-Pin PAL® Devices**
- **Individually Programmable Output Polarity**
- **Power-Up Reset and Three-State**
- **Register Preload for Testability**
- **High Programming Yields Using Highly Reliable Vertical-Fuse Technology**
- **Complete AC/DC Testability**
- **Security Fuse to Prevent Unauthorized Duplication**
- **Available in 300-mil Plastic and Ceramic DIP**

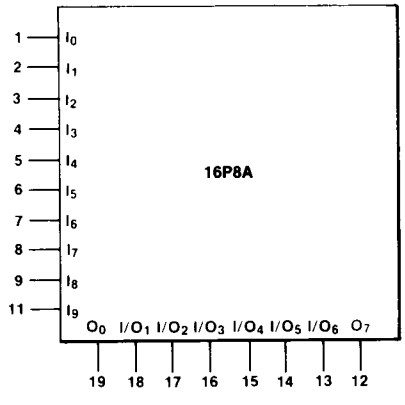
Connection Diagram



Pin Names

I_0 - I_9	Input
O_0, O_7	Output
I/O_1 - I/O_6	Bi-Directional Output

Logic Symbol



V_{CC} = pin 20
GND = pin 10

Ordering Information

16P8A
16RP4A
16RP6A
16RP8A **D** **C** **QR**

Device Name
Package
Temperature Range
Optional Processing

Packages
D = Ceramic DIP
P = Plastic DIP

Temperature Ranges
C = 0°C to +75°C

Optional Processing
QR = Commercial Device with 160 Hour Burn in

®PAL is a registered trademark of Monolithic Memories Inc.

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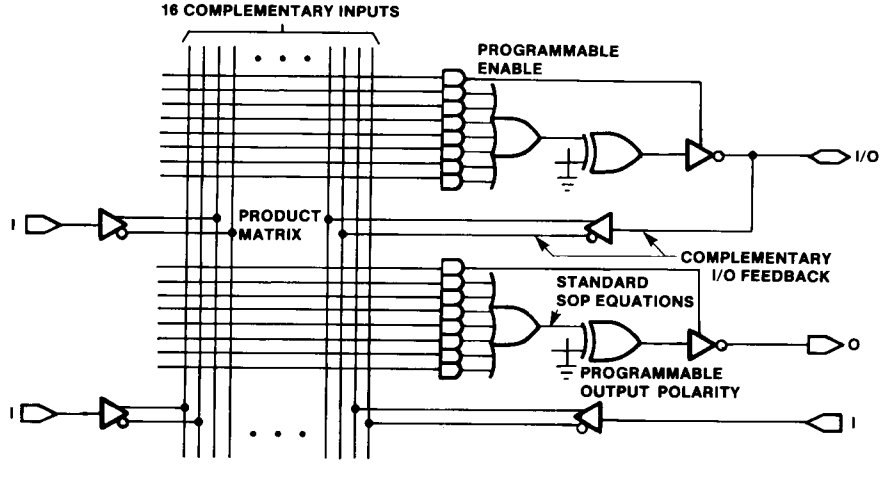
PRELIMINARY INFORMATION

FASTPLA 16P8A Series Summary

		16P8	16RP4	16RP6	16RP8
INPUTS	Dedicated	10	8	8	8
	Clock	—	1	1	1
LOGIC	7-Wide AND/OR	8	4	2	—
	8-Wide AND/OR	—	4	6	8
OE	Individually Programmable	8	4	2	—
	Dedicated	—	4	6	8
OUTPUTS	Programmable Polarity	8	8	8	8
	Bi-Directional	6	4	2	—
	Dedicated	2	—	—	—
	Registered (with feedback)	—	4	6	8

16P8 Functional Diagram



16P8 Functional Description

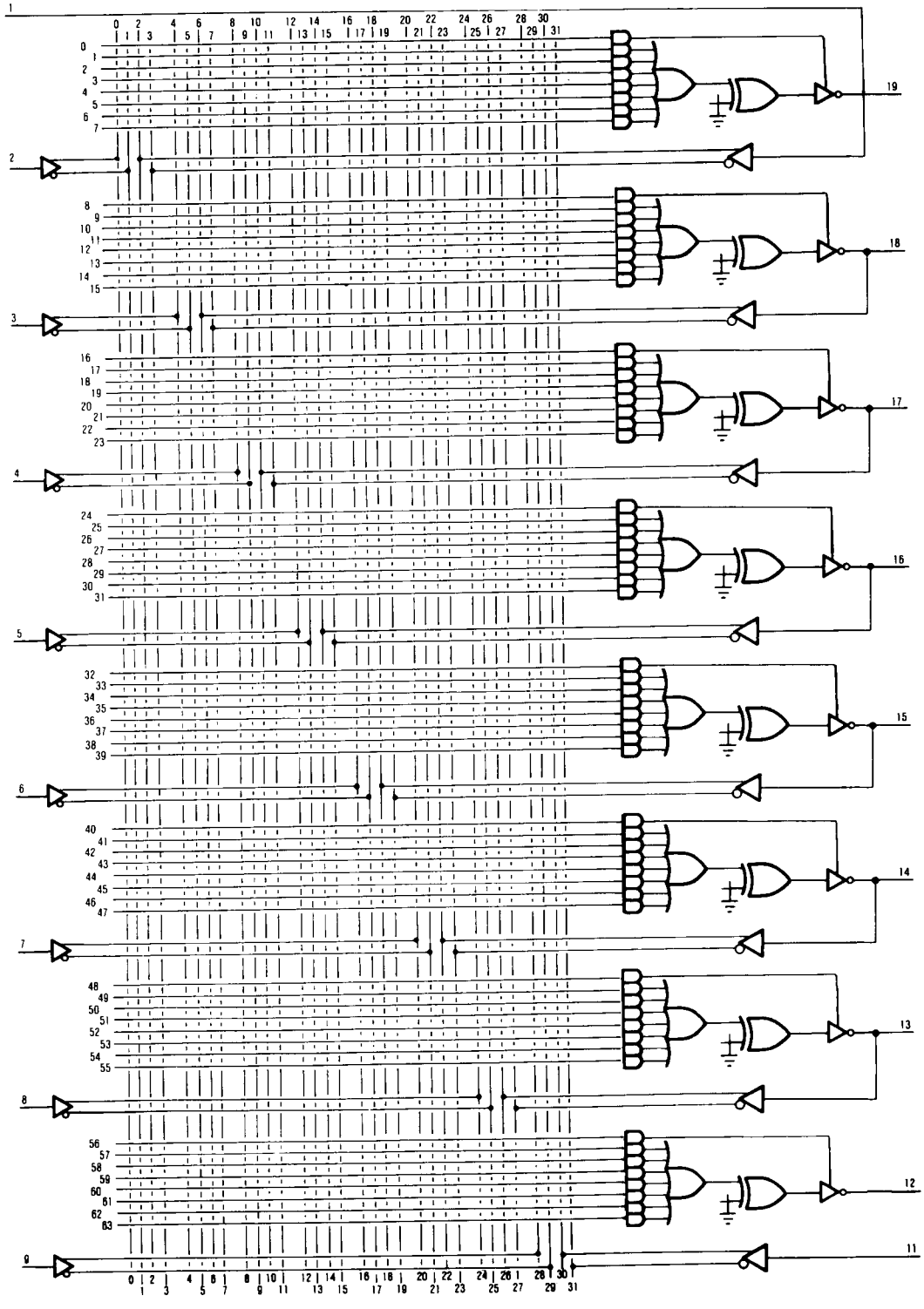
The FASTPLA 16P8A is a bipolar TTL programmable logic array (PLA) consisting of a programmable AND array feeding a fixed OR array. It is organized with 10 dedicated inputs, 2 dedicated outputs, and 6 bi-directional input/outputs as shown in the family summary chart. Standard sum-of-products (SOP) form is equated at the output of the OR array as shown in the functional diagram. The output polarity can be individually programmed or designs can be configured for 16L8 and 16H8 versions. Each output buffer is enabled by a dedicated active HIGH product term.

Initially all vertical fuse cells are unprogrammed. The unprogrammed output polarity fuses are equivalent to low impedance connections from the exclusive OR gate to ground. Hence, all outputs are initially active LOW. Once the polarity fuse is programmed, the output is permanently active HIGH.

At power-on, outputs remain in the high impedance state until DC power supply conditions are met, after which they are controlled by dedicated programmable enable product terms.

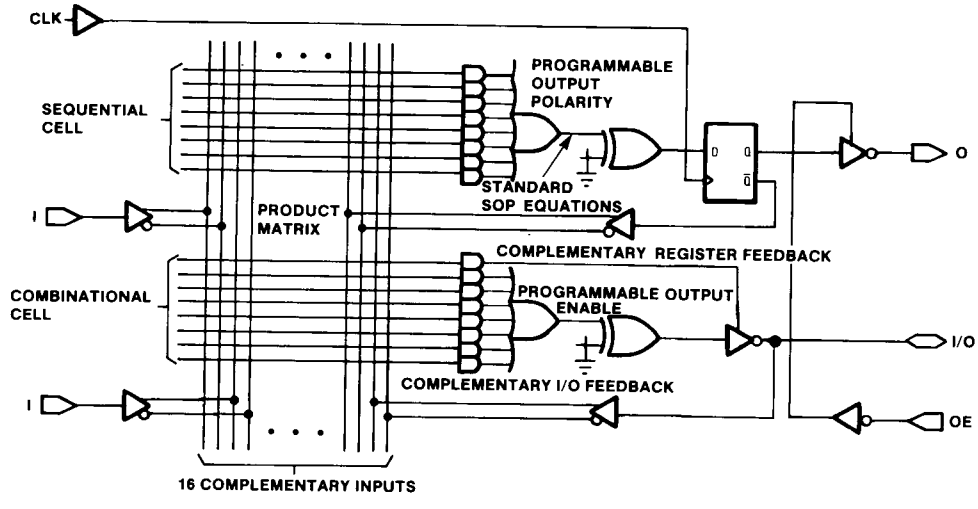
PRELIMINARY INFORMATION

Logic Diagram 16P8A



PRELIMINARY INFORMATION

16RP4, 16RP6, 16RP8 Functional Diagram



Functional Description

The FASTPLA 16RP4, 16RP6, 16RP8 are bipolar TTL programmable logic arrays (PLA) incorporating synchronous D-type registers at the output of the fixed OR array. The 16RP4, 16RP6 have both combinational output cells with feedback and programmable output enable, and sequential output cells with register feedback and dedicated output enable. The 16RP8 has eight sequential output cells with register feedback and dedicated output enable. Refer to the FASTPLA summary chart for the particulars of each device.

Standard sum-of-products (SOP) form is equated at the output of the OR array as shown in the functional diagram. Programmable output polarity gives the user more flexibility in design. Each output polarity may be individually defined active HIGH or active LOW.

At power-on, outputs remain in the high impedance state until DC power supply conditions are met, thereafter changing state according to the inputs (combinational cell) or output enable (sequential cell). At power on all registers are initialized to a logical LOW, thereby setting all outputs to a logical HIGH. At the first LOW-to-HIGH-transition of the clock pulse, the output state will change according to the specified D-inputs. This power-on reset feature assures the user that the registers will begin clocking from a known state and hence simplifies sequential machine design and testing.

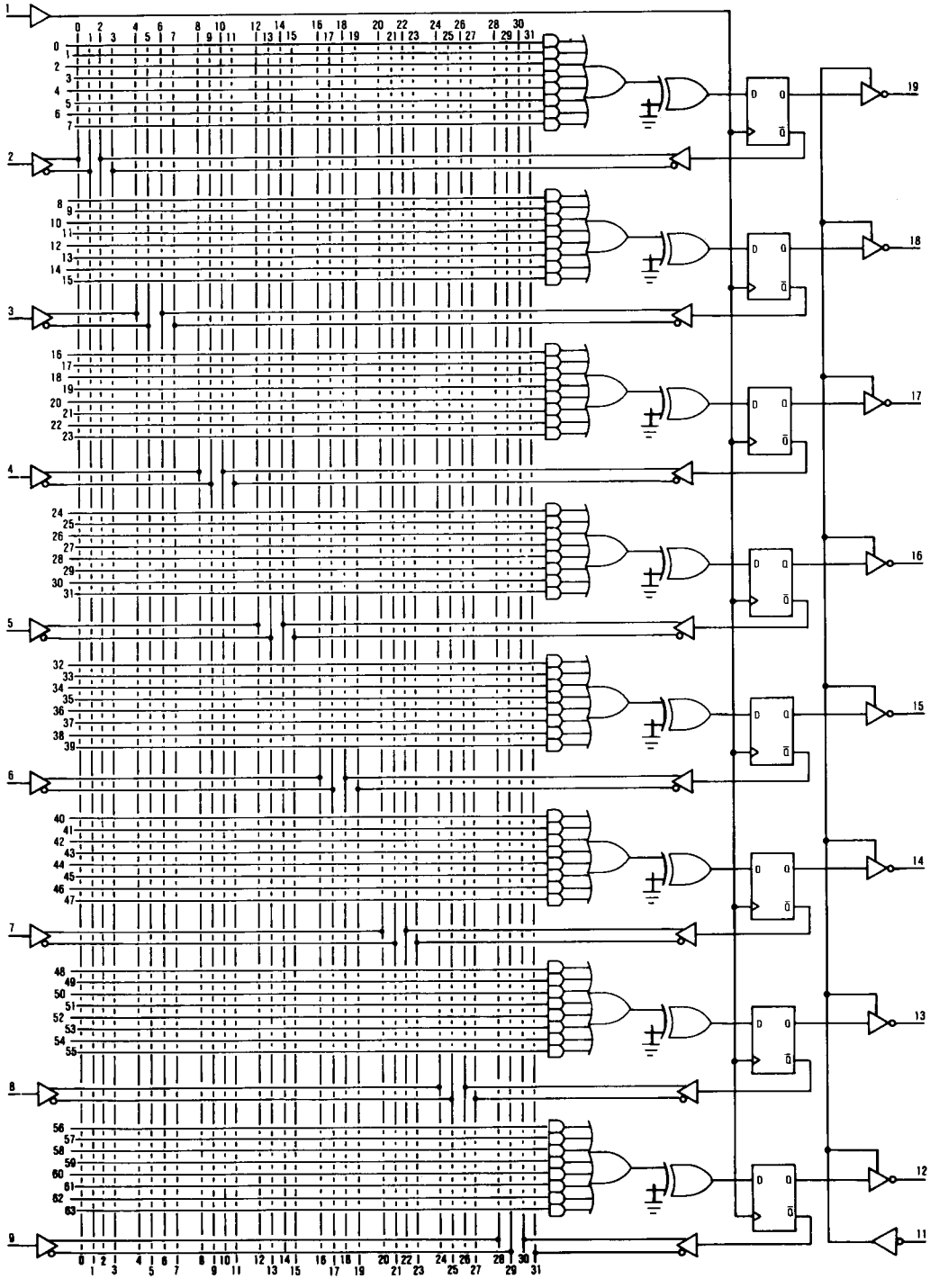
For testability, register preload is provided. It allows the user to individually preset the registers to either a HIGH or LOW level through the use of a 10V control signal. This allows all states of a sequential design to be tested. This feature allows full compatability with PLDtest®* software.

Initially all vertical fuse cells are unprogrammed. The outputs of the AND array are active HIGH true, thereby causing the outputs of the OR array to be HIGH true. All unprogrammed output polarity fuses are equivalent low impedance connections from the exclusive OR gate to ground. All combinational outputs read active LOW true and are enabled. Prior to the first LOW to HIGH clock transition, registered outputs read active HIGH true and are enabled according to the state of the OE pin.

*PLDtest is a registered trademark of DATA I/O Inc.

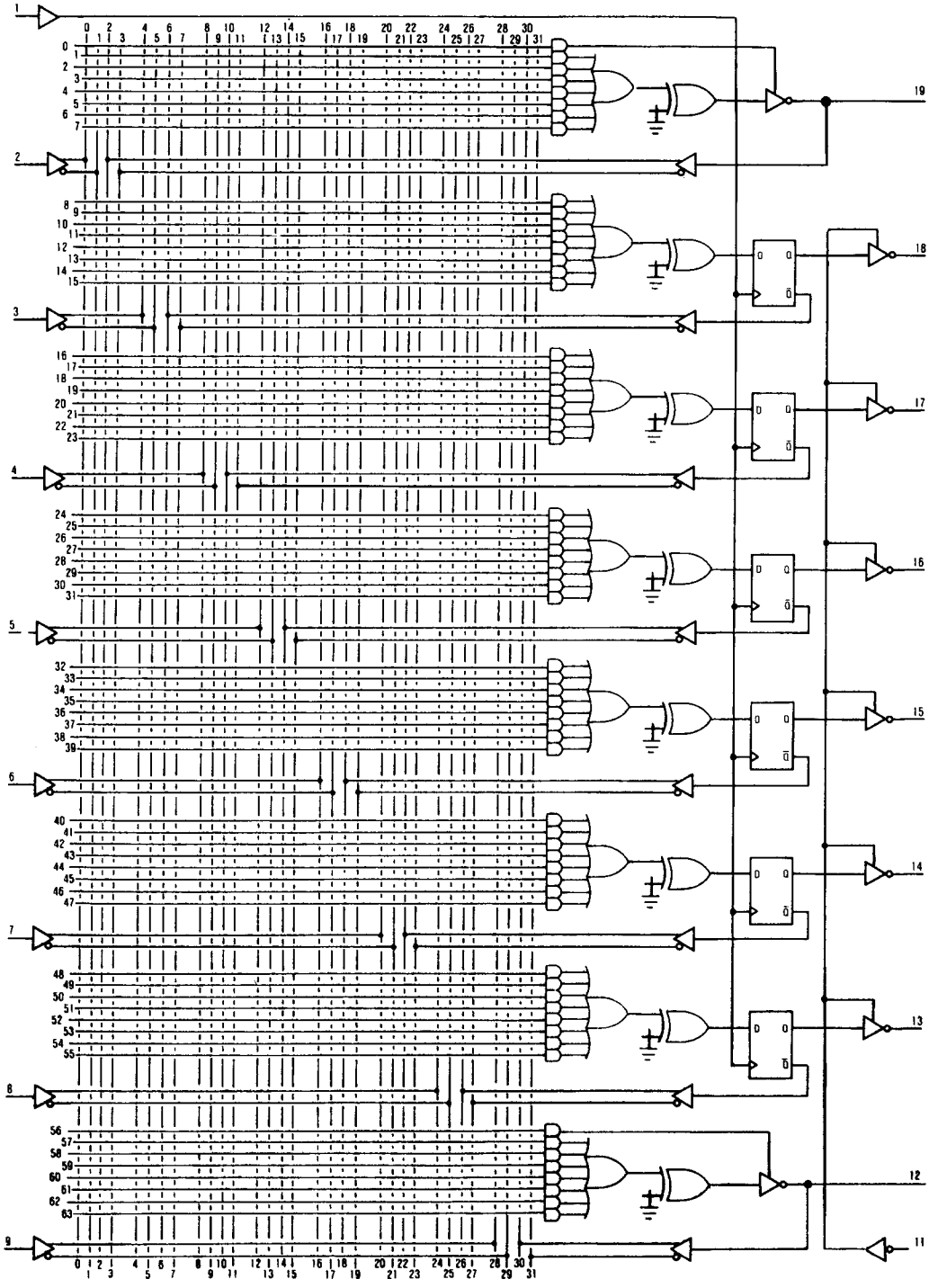
PRELIMINARY INFORMATION

Logic Diagram 16RP8A



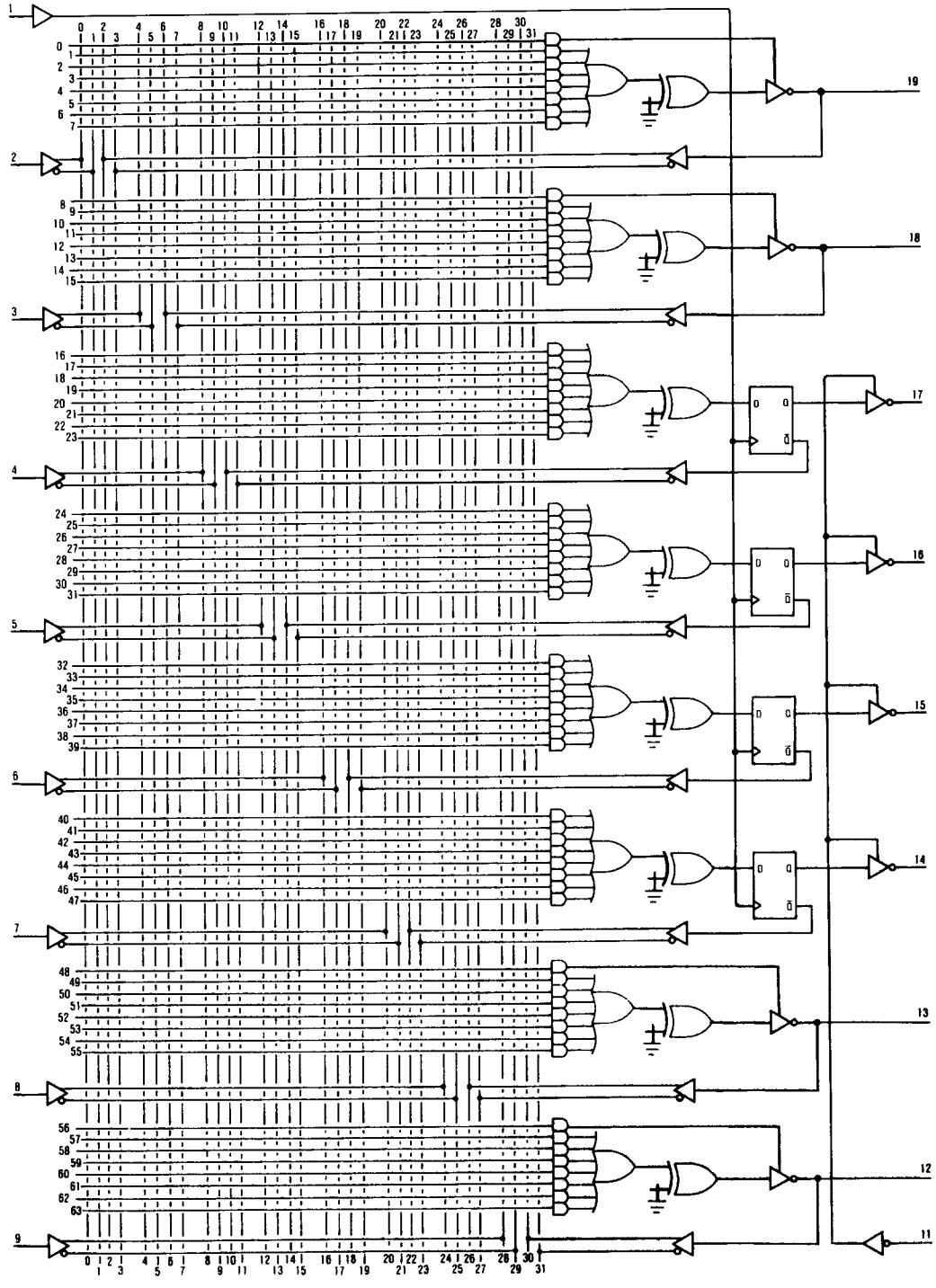
PRELIMINARY INFORMATION

Logic Diagram 16RP6A



PRELIMINARY INFORMATION

Logic Diagram 16RP4A



PRELIMINARY INFORMATION

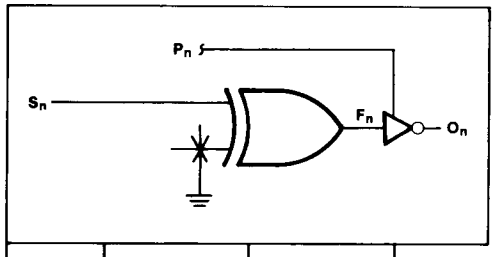
State of Delivery

- Programmability Verified
- All AND Gates are Active HIGH True
- All OR Outputs are Active HIGH True
- All Combinational Outputs are Enabled
- All Combinational Outputs are Active LOW True
- All Registered Outputs are Initialized Active HIGH True
- Security Fuse is Unprogrammed

Shown below are unprogrammed and programmed fuse map relationships:

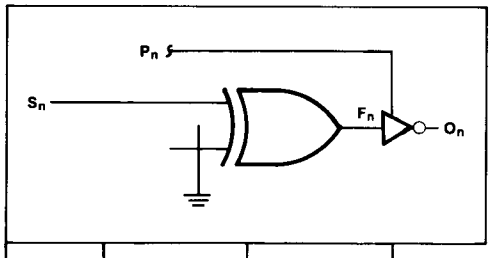
OUTPUT POLARITY

UNPROGRAMMED



O_n STATUS	F_n STATUS	CODE
ACTIVE LOW	ACTIVE HIGH	X*

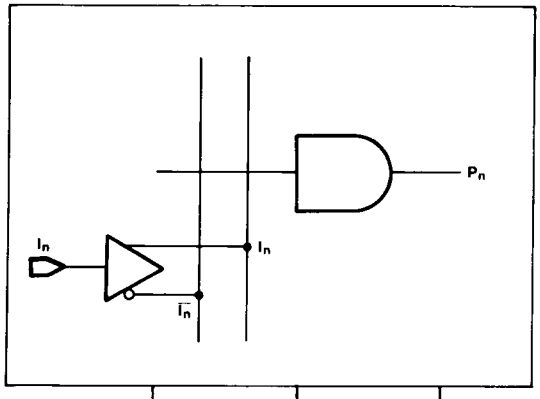
PROGRAMMED



O_n STATUS	F_n STATUS	CODE
ACTIVE HIGH	ACTIVE LOW	—

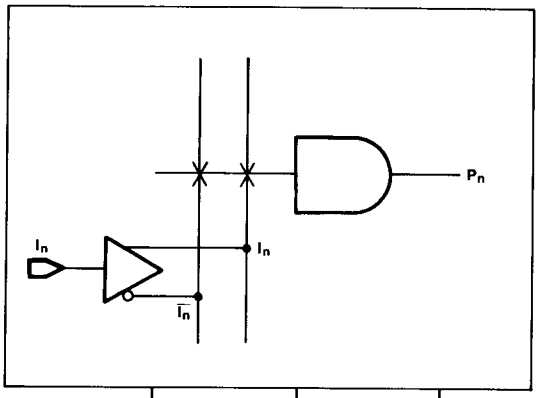
'AND' ARRAY

UNPROGRAMMED



P_n STATE	CODE
LOGIC '1'	—

PROGRAMMED



P_n STATE	CODE
LOGIC '0'	X*

S_n = SUMMING OUTPUT
P_n = PRODUCT TERM
F_n = EXCLUSIVE OR OUTPUT
I_n = INPUT VARIABLE
O_n = OUTPUT VARIBLE

* An 'X' represents a low impedance connection.

PRELIMINARY INFORMATION

Absolute Maximum Rating: Above which the useful life may be impaired[1]

Storage Temperature	-65° C to +150° C
Ambient Temperature Under Bias	-55° C to +125° C
Junction Temperature Under Bias	-55° C to +150° C
V_{CC} Pin Potential to Ground Pin	-1.5 V to +7.0 V
Input Voltage [2]	-1.5 V to +7.0 V
Input Voltage Pin 1, Program Mode	-1.5 V to +21.0 V
Input Voltage Pin 11, Program Mode	-1.5 V to +12.0 V
Input Voltage Pins 2, 12-19 [7]	-1.5 V to +12.0 V
Input Current [2]	-18.0 mA to +5.0 mA
Input Current Pin 1, Program Mode	**+180.0 mA**
Voltage Applied to Outputs (Async)	-0.5 V to V_{CC} max. V
Voltage Applied to Outputs (Registered)	-0.5 V to V_{CC} max. V
Current Applied to Outputs	+100.0 mA

DC Performance Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Parameter	Min	Max	Units	V_{CC}[1]	Conditions
I_{CC}	Supply Current		(180)	mA	Max	All Inputs Equal 0.0 V Outputs Open
V_{IH}[2,3]	Input HIGH Voltage	2.0		V	Max	Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}[2,3]	Input LOW Voltage		0.8	V	Max	Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_Z	Control Voltage	9.5	10.5	V	Min	
V_{CD}	Input Clamp Diode Voltage		-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	2.7		V	Min	V_{IL} = 0.0 V V_{IH} = 3.0 V I_{OH} = -3.2 mA
V_{OL}	Output LOW Voltage		0.5	V	Min	V_{IL} = 0.0 V V_{IH} = 3.0 V I_{OL} = 24 mA
I_{IH}[4]	Input HIGH Current		25	μA	Max	V_{IN} = 2.7 V
I_I[4]	Input HIGH Current		25	μA	Max	V_{IN} = 5.5 V
I_{IL}[4]	Input LOW Current		-250	μA	Max	V_{IN} = 0.5 V
I_{OZH}[4]	Output Leakage Current		50	μA	Max	V_{OUT} = 2.7 V
I_{OZL}[4]	Output Leakage Current		-50	μA	Max	V_{OUT} = 0.5 V
I_{OS}[5]	Output Short Circuit	-60	-150	mA	Max	V_{OUT} = 0.0 V
C_{IN}[6]	Input Capacitance		15	pF		V_{IN} = 2.0 V, f = 1 MHz
C_{OUT}[6]	Output Capacitance		15	pF		V_{IN} = 2.0 V, f = 1 MHz
C_{IO}[6]	Bi-Directional Pin Cap.		15	pF		V_{IN} = 2.0 V, f = 1 MHz

PRELIMINARY INFORMATION

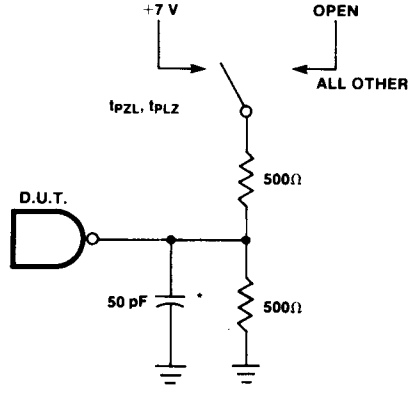
AC Performance Characteristics: V_{CC} = 5.0V ± 5% , GND = 0V, T_C = 0°C to +75°C.

Parameter	Description	Switch[8]	Min	Max	Units
t_{PD}	Input or Feedback to Non-Registered Outputs	Open		25	ns
t_{PZX}[6]	Input to Output Enable ZH ZL	Open Closed		25	ns
t_{PXZ}[6]	Input to Output Disable HZ LZ	Open Closed		25	ns
t_{PZX}	Pin 11 To Output Enable ZH ZL	Open Closed		20	ns
t_{PXZ}	Pin 11 to Output Disable HZ LZ	Open Closed		15	ns
t_{CO}	Clock to Output	Open		15	ns
t_{SU}	Input or Feedback Setup Time		20		ns
t_H	Hold Time		0		ns
t_P[6]	Clock Period		28		ns
t_{WL}[9]	Clock Width LOW		15		ns
t_{WH}[9]	Clock Width HIGH		12		ns
f_{MAX}	Maximum Clock Frequency		35		MHz

Performance Characteristics Notes

1. Unless otherwise restricted or extended by detail specification.
2. Either input voltage or current limit sufficient to protect inputs.
3. These are absolute values with respect to pin 10 (device ground) and includes all overshoots due to system AND/OR tester noise.
4. I/O pin leakage is the worst case of I_{OZX}, I_{IX}, X = H/L.
5. For testing I_{OS}, the use of HIGH speed test apparatus AND/OR sample and hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. For any sequence of parameter tests, I_{OS} tests should be performed last. Only one output should be shorted at a time.
6. These parameters are not 100% tested but are periodically sampled.
7. Preload/clear functions on registered outputs only. The output must be three-stated before V_Z may be applied.
8. See AC test loads.
9. $t_{WH} + t_{WL} \geq 28$ ns.

AC Test Loads

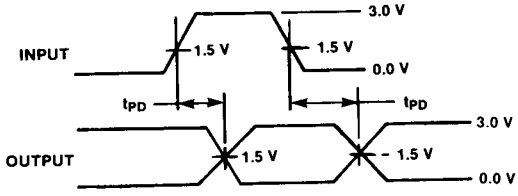


*INCLUDES JIG AND PROBE CAPACITANCE

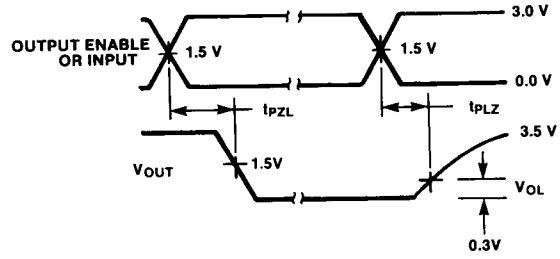
PRELIMINARY INFORMATION

AC Waveforms

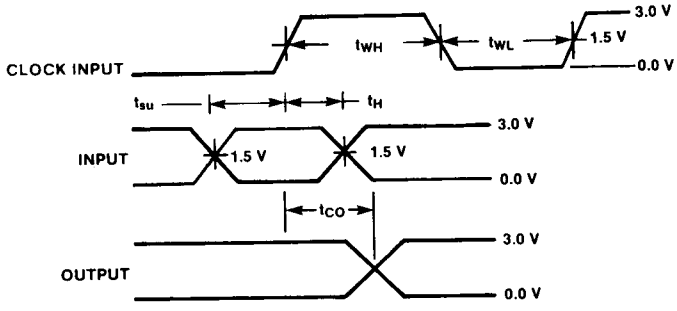
PROPAGATION DELAY



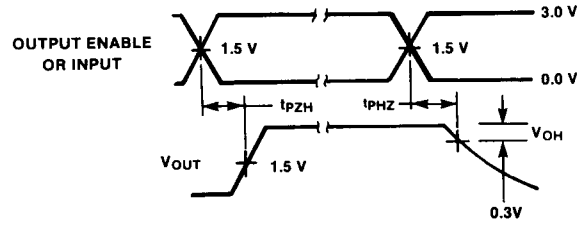
3-State Output LOW Enable and Disable Times



SETUP AND HOLD, PULSE WIDTH

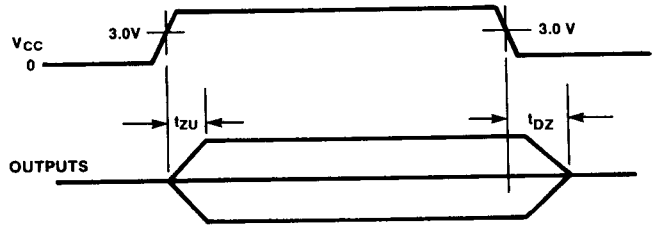


3-State Output HIGH Enable and Disable Times



Power-up Three-state

All outputs will be disabled when V_{CC} is less than approximately 3.0V (25° C).



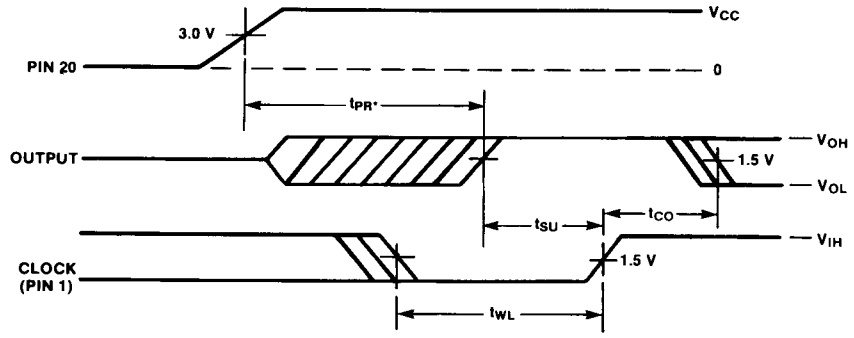
*t_{ZU} and t_{DZ} are less than 0.1 μs.

PRELIMINARY INFORMATION

Power-Up Reset

Two conditions are required to ensure a valid power-up reset:

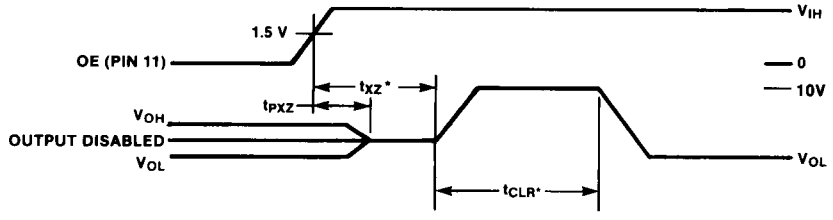
1. V_{CC} must rise to recommended DC value.
2. After reset, the clock input must be held LOW for time t_{SU} before clocking.



Preload of Registered Outputs for Testability

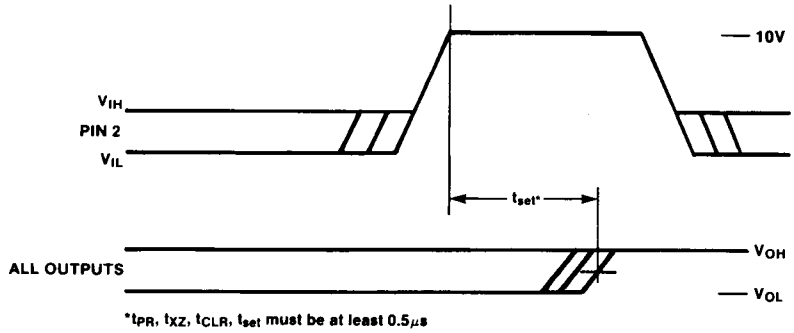
To preload a register to an active HIGH level, the following steps are required:

1. Apply a logic HIGH level voltage to the output enable input (Pin 11) to three-state the device.
2. After the specified time (t_{XZ}) raise desired output pin to the control voltage level (10V) and hold for the specified time (t_{CLR}). (Register is set HIGH, output active LOW).



To preload all registers simultaneously to an active LOW level, the following steps are required:

1. Raise input Pin 2 to the control voltage (10V) for the specified time (t_{set}). (All registers reset LOW, all outputs will be set active HIGH true).



*t_{PR}, t_{XZ}, t_{CLR}, t_{set} must be at least 0.5μs

PRELIMINARY INFORMATION

Programming

The FASTPLA 16P8A Series is programmed by applying a control signal to the Edit Enable pin (pin 11) and appropriate programming waveforms to the Fusing Supply (pin 1). Individual fuses are addressed by applying TTL levels to the row and column address inputs. The Edit Output pin (pin 12 open collector output) is active HIGH when the selected fuse has been programmed.

Programming Sequence*:

1. Connect pin 10 (GND) to Ground.
2. Connect pin 20 (V_{CC}) to 5.5 V.
3. Connect pin 11 (Edit Enable) to 11 V.
4. Connect pin 12 (Edit Output) to V_{CC} through a 1-2K resistor.
5. Connect pin 1 (Fusing Supply) to fusing current source.
6. Apply TTL levels to C_0-C_6 and R_0-R_5 to address desired vertical fuse cell.
7. Apply programming current pulse train to pin 1 reading pin 12 between pulses. Terminate the pulse train when pin 12 is TTL HIGH.
8. Repeat steps 6 and 7 for the next address.

Verification Sequence*:

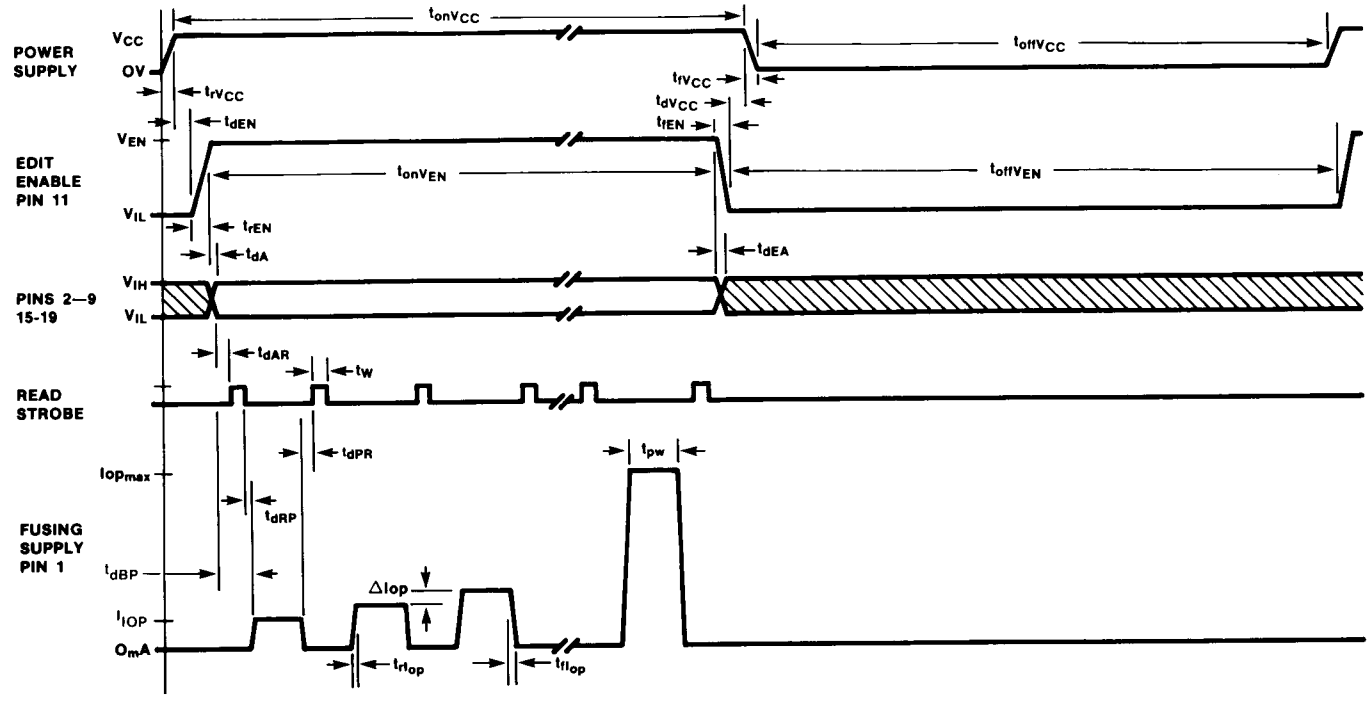
1. Connect pin 10 (GND) to Ground.
2. Connect pin 20 (V_{CC}) to 5.5 V.
3. Connect pin 11 (Edit Enable) to 11 V.
4. Connect pin 12 (Edit Output) to V_{CC} though a 1-2K resistor.
5. Apply TTL levels to C_0-C_6 and R_0-R_5.
6. Read pin 12, TTL HIGH - programmed cell.
   TTL LOW - unprogrammed cell.

*For additional information request Fairchild's complete programming algorithm specification.

Security Fuse

The security fuse is initially unprogrammed to allow editing and programming of the device. When programmed, the security fuse disables the verification circuitry on the device, thereby protecting the design from unauthorized dupication. Programming is accomplished by following the sequence as outlined in the programming specifications table.

Programming Timing Diagram



PRELIMINARY INFORMATION

Programming Specifications[4]

Symbol	Parameter	Min	Recommended Values	Max	Units	Comments
Power Supply						
V_{CC}	Power Supply Voltage	5.4	5.5	5.6	V	
t_{rVCC}	Power Supply Rise Time	0.2	2.0		μs	*See Note 3*
t_{fVCC}	Power Supply Fall Time	0.2	2.0		μs	*See Note 3*
t_{onVCC}	V_{CC} on Time[1]					*See Programming Timing Diagram*
t_{offVCC}	V_{CC} off Time[2]					
	Duty Cycle for V_{CC}			50%		$t_{on}/(t_{on} + t_{off})$
Edit Enable Power Supply						
V_{EN}	Edit Enable Supply Voltage	10.5	11.0	11.5	V	Applied to Pin 11
t_{dEN}	Delay to Enable	1.0	2.0		μs	V_{CC} Settling Time
t_{rEN}	Enable Rise Time	0.4	2.0		μs	*See Note 3*
t_{fEN}	Enable Fall Time	0.4	2.0		μs	*See Note 3*
t_{dA}	Delay to Address	0.1	1.0		μs	Delay from 90% of V_{EN} until Addresses are Valid [6]
t_{dEA}	Delay to Address Invalid			1.0	μs	Delay from 90% of V_{EN} until Addresses are Invalid[6]
t_{dVCC}	Delay to V_{CC} off	1.0	2.0		μs	
t_{onEN}	V_{EN} on Time					*See Programming Timing Diagram*
t_{offEN}	V_{EN} off Time					
	Duty Cycle for V_{EN}			50%		$t_{on}/(t_{on} + t_{off})$
V_{iL}		0	0	0.4	V	
V_{IH}		2.4	5.0	5.0	V	
Read Strobe [5]						
t_{dAR}	Delay from Valid Address to to Valid Read	0.1	0.5		μs	Initial Check
t_{dRP}	Delay from Read to Programming Pulse	0.1			μs	
t_{dPR}	Delay from Programming Pulse to Read	2.0			μs	Verify
t_w	Cell Read Time		1.0		μs	
Programming Current Pulse Train						
I_{lop}	Initial Current Pulse	40	40	60	mA	Current on Pin 1
I_{opmax}	Prog. Current Limit	140	160	180	mA	Current on Pin 1
V_{opmax}	Prog. Voltage Limit	19	20	20	V	Voltage on Pin 1
t_{rlop}	Prog. Pulse Rise Time	0.3	1.0	1.45	μs	*See Note 3*
t_{flop}	Prog. Pulse Fall Time		0.1	0.5	μs	*See Note 3*
t_{dBP}	Delay to I_{lop}	2	3		μs	Delay from Address Valid
t_{pw}	Pulse Width	6	7	8	μs	*See Note 7*
I_{op}	Current Pulse Step	5	10	10	mA	Each Successive Pulse is Increased by Delta I_{op}
	Duty Cycle for Prog. Pulse	10	50	50	%	

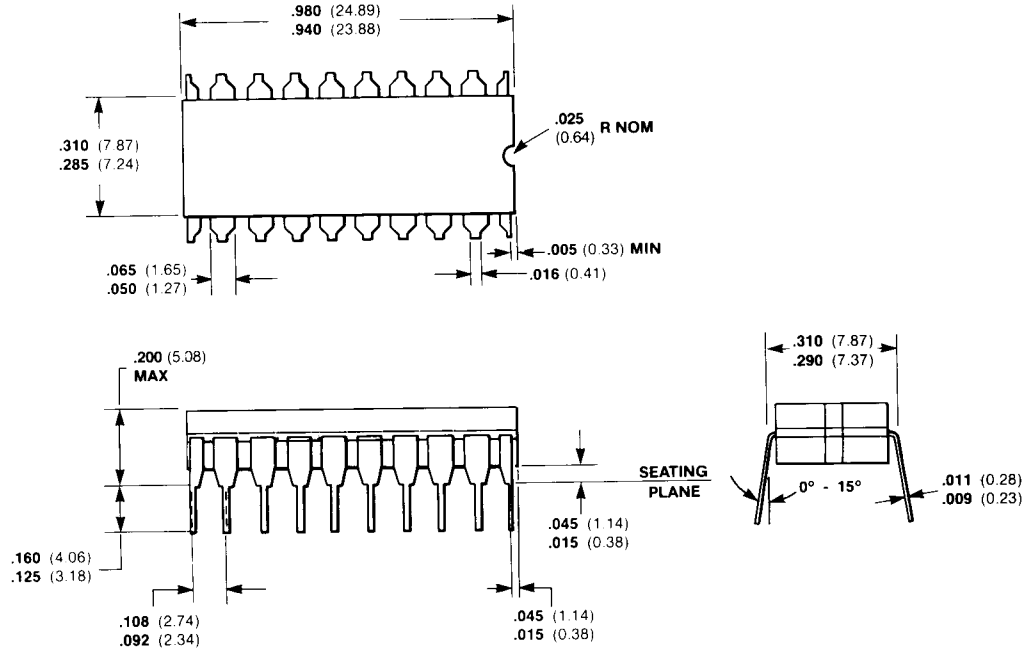
See Notes on Page 15

PRELIMINARY INFORMATION

Programming Specification Notes

1. Total time V_{CC} is on to program cell is equal to or greater than the sum of all the specified delays, pulse width and rise/fall times
2. $t_{off} \geq t_{on}$
3. Rise & fall times are from 10% to 90%
4. Recommended programming temperature, $t_p = 25°C \pm 10°C$
5. Proceed to next address after pin 12 indicates a programmed cell
6. Return to input and/or output function when address is invalid
7. Does not include rise and fall times

Package Outlines
20-Pin Ceramic DIP

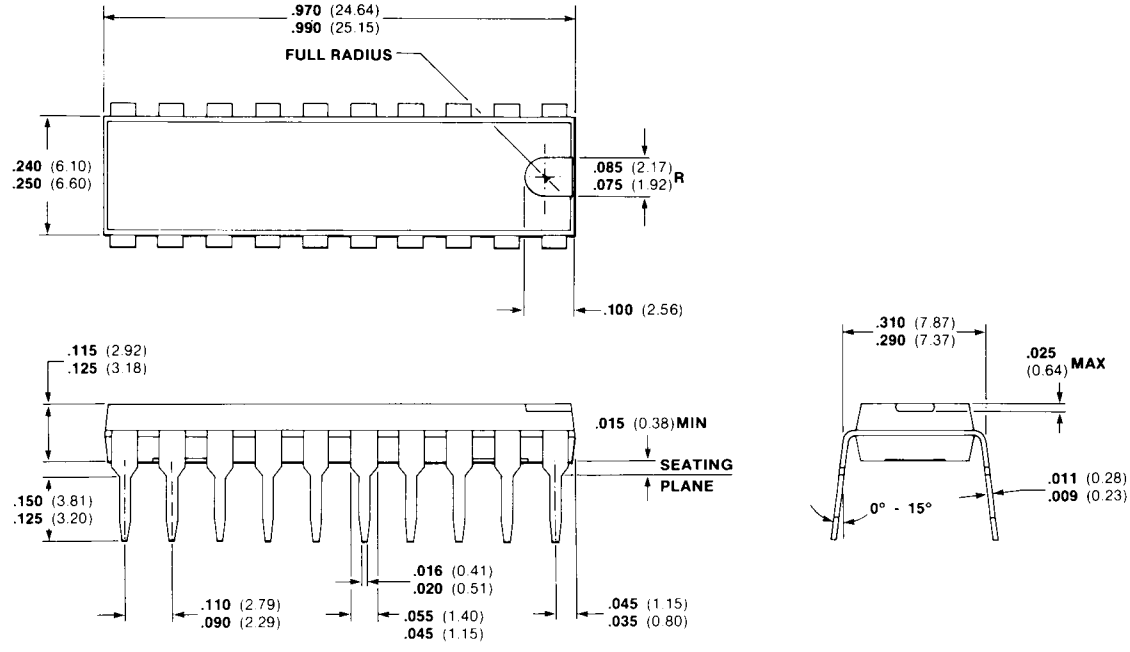


Notes

Pins are tin-plated alloy or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Hermetically sealed alumina package
Package weight is 2.9 grams
These dimensions include misalignment glass over-run etc...
*The **.045 - .030** dimension does not apply to the corner pins
Lead thickness and width may increase by **.003** (0.07) when lead finish is applied.

PRELIMINARY INFORMATION

Package Outlines
20-Pin Plastic DIP



Notes
Pins are nickel plated and solder dipped copper (olin 195)
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.020"** (0.51) diameter lead
Package weight is approximately 1.0 gram
Lead thickness and width may increase by **.003** (0.07) when lead finish is applied

All dimensions in inches **bold** and millimeters (parentheses)

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Manufactured under one of the following U.S. Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.