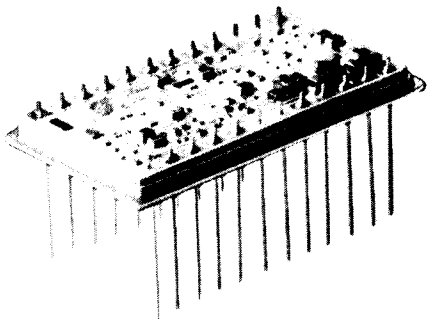
ADH-050 AND ADH-051



HYBRID VIDEO TRACK/HOLD
100 ns Acquisition Time;
± 0.0125% Max Linearity Error

DESCRIPTION

The industry's first hybrid video track and hold module, the ADH-050 features small size, fast acquisition time (100 ns, typ.) and low aperture time uncertainty (500 ps, max.). Standard processing with no added cost conforms to MIL-STD-883 except for burn-in which is an option.

The Model ADH-051 has a larger hold capacitor than the ADH-050. The larger capacitor reduces the hold drift rate by a factor of five, with a corresponding increase in acquisition time and decrease in bandwidth.

Included as standard in all units is a pin programmable input buffer amplifier which may be used differentially, single ended, or as a follower with $10^7\Omega$ input impedance. Linearity is better than .0125%, making the ADH-050 suitable for use in 12 bit systems. No adjustment, trimming, or periodic calibrations are required.

APPLICATIONS

The Model ADH-050 is designed for track/hold requirements for video digitizing. It is ideal for avionics and other high reliability applications. Other uses include high-speed data processing systems and A/D converters.

FEATURES

- *500 pS APERTURE TIME UNCERTAINTY (JITTER)*
- *0.1 mV/μs DROOP*
- *70 ns TYP SETTLING TIME TO ±2 mV*
- *PIN PROGRAMMABLE INPUT BUFFER AMPLIFIER*
- *POWER SUPPLIES INTERNALLY DECOUPLED*

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SPECIFICATIONS

At 25° and nominal supply voltages unless otherwise noted.

PARAMETER	UNITS	VALUE	
ACCURACY (AC, in to out, referred to 10V full scale range)			
Gain (pin programmable)		−1; ±1/2; ±2	
Gain Error	%	0.1 max	
Gain Tempco	ppm/°C	2 typ; 5 max	
Linearity Error	%	±0.0125 max	
Linearity Tempco	ppm/°C	2 typ; 5 max	
Track/Hold Amplifier			
Offset	mV	5 typ; 20 max	
Offset Tempco	μV/°C	20 typ; 50 max	
Pedestal	mV	20 typ. 30 max	
Pedestal Tempco	μV/°C	10 typ; 25 max	
Buffer Amplifier			
Offset, Referred to Buffer Input	mV	1 typ; 3 max	
Offset Tempco	μV/°C	20 typ; 50 max	
Note: See Tempco Values for case temp. −55°C to 110°C			
DYNAMIC CHARACTERISTICS		ADH-050	ADH-051
Small Signal Bandwidth			
Track/Hold Stage	MHz	15 typ	3.5 typ
Buffer Stage (Follower)	MHz	5 typ	5 typ
Slew Rate			
Track/Hold	V/μs	200 typ	80 typ
Buffer Amplifier	V/μs	60 typ	60 typ
Aperture			
Time Delay	ns	5 max	5 max
Delay Uncertainty (Jitter)	ps	500 max	1000 max
Acquisition Time			
±5V T/H Amplifier Input	ns	100 typ	500 typ
	ns	120 max	600 max
±1V T/H Amplifier Input	ns	90 typ	450 typ
	ns	100 max	500 max
Settling Time (To Within ±2 mV of Final Value)			
T/H Amplifier in Track Mode	ns	100 max, 70 typ	
Buffer Amplifier	ns	500 max	
Feedthrough Attenuation (Hold Model)	dB	80 typ	80 typ
	dB	60 max	66 max
Droop Rate at 25°C Case Temp.	mV/μs	0.1 max	0.02 max
Droop Rate Temperature Dependence		Doubles every 10°C	
Note: For lower droop rates, consult factory			

PARAMETER	UNITS	VALUE
ANALOG INPUT		
Input Capacitance w/without Buffer	pF	15 max
Absolute Max Voltage, w/without Buffer	V	±15
Without Buffer Amplifier		
Input Voltage Range	V	±5
Input Impedance	Ω	300
Buffer Amplifier Characteristics		
Impedance as Follower	Ω	10^7 min
Bias Current	na	100 typ; 250 max
Output Voltage Range	V	±5 max
Buffer as Differential Amplifier		
Input Voltage Range	V	±2.5 min
Common Mode Range	V	±10 max
Input Impedance (Differential)	Ω	1000 typ
Buffer as Single Ended Amplifier		
Input Voltage Range	V	±2.5 max
Impedance	Ω	1500 typ
Note: A gain of 1/2 is also pin-programmable – see text		
LOGIC INPUT		
Track Mode Current (-0.8V, Logic 1)	mA	2.2 typ
Hold Mode Current (-1.8V, Logic 0)	mA	1.7 typ
OUTPUT		
Voltage Swing	V	±6 min
Current Range	mA	±10 min
Impedance	Ω	0.1 max
Short Circuit Protection		(up to one minute)
POWER REQUIREMENTS		
Supply Voltages	V	+15 ± 5% / −15 ± 5% / −5.2 ± 5%
Absolute Max Without Damage	V	+18 / −18 / −7
Current	mA	75 max / 55 max / 55 max
THERMAL CHARACTERISTICS		
Operating Temperature (Case)	°C	−55 to +110
Storage Temperature	°C	−55 to +125
Thermal Resistance, Case to Air	°C/Watt	θ_{CA} = 20 typ
PHYSICAL CHARACTERISTICS		
Size (24 Pin Double DIP)	inch	1.4 x 0.8 x 0.28 (3.6 x 2.0 x 0.71 cm)
Weight	oz	0.42 typ (11.9 g)

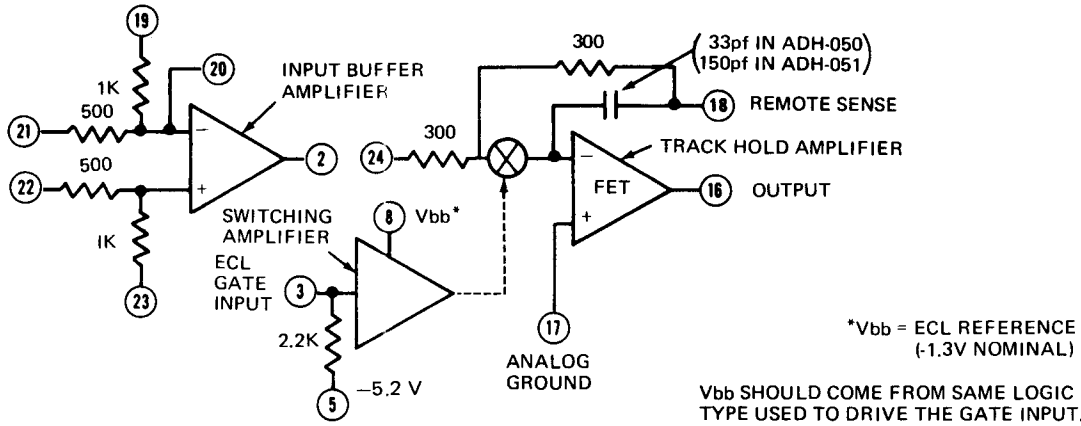


FIGURE 1. ADH-050/051 BLOCK DIAGRAM

TECHNICAL INFORMATION

1. INTRODUCTION

The ADH-050 consists of two parts (Figure 1); a track and hold amplifier with an ECL logic gate input and a gain of -1, and an input buffer amplifier. Depending on the external pin connections, the buffer amplifier may be either by-passed or connected in various ways, as described below.

With the ECL gate at -0.8V (logic 1), the output will track the input with no time limitation. The output is D.C. coupled and there is no duty cycle restriction. On application of -1.8V to the gate (logic 0), the output switches to a "hold" condition, the voltage being held constant by a holding capacitor. Slow leakage from this capacitor causes the output to drift, or droop, in a systematic way as indicated in the specifications.

In a track/hold amplifier such as the ADH-050, the switch is DC coupled to the gate and there is no limitation on the tracking time. In a sample/hold amplifier, the switch is AC coupled, and the input signal is sampled briefly. This usually allows shorter acquisition times and greater sampling rates. Consider the sample/hold amplifiers in the DDC product line for such applications.

The terminology, signal relationships, and major design considerations for track/holds such as the ADH-050 and ADH-051 are discussed in the Background Information at the front of the S/H and T/H section of this catalog.

2. INPUT BUFFER AMPLIFIER

The input buffer amplifier may be connected in a variety of ways. The follower configuration shown in Figure 2 provides an input impedance greater than 10^7 ohm and is useful for multiplexing. Differential and single ended inputs with a gain of 2 may be obtained as in Figures 3 and 4. The gain may be reduced to 1/2 in the circuits of Figures 3 and 4 by interchanging pins 19 and 21, and pins 22 and 23. With a gain of 1/2, the allowable input voltage is ±10V.

Caution: use of external resistors to adjust the gain may greatly increase temperature effects. The internal resistances of the buffer amplifier have been precisely adjusted to provide a gain tempco of less than 3 ppm.

In the differential amplifier configuration shown in Figure 3, any common mode voltage e_{cm} must be less than ±10V.

The bandwidth of the buffer amplifier can be reduced by connecting a capacitor between pins 20 and 19. This may be useful in reducing the input analog signal noise level.

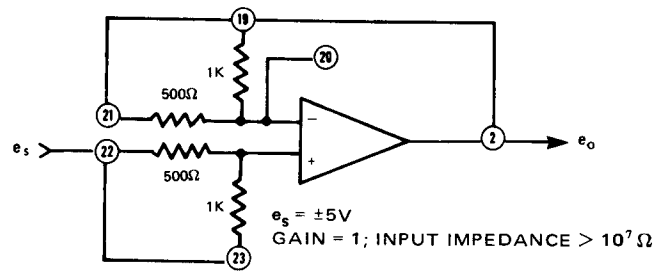


FIGURE 2. BUFFER AMPLIFIER CONNECTED AS FOLLOWER

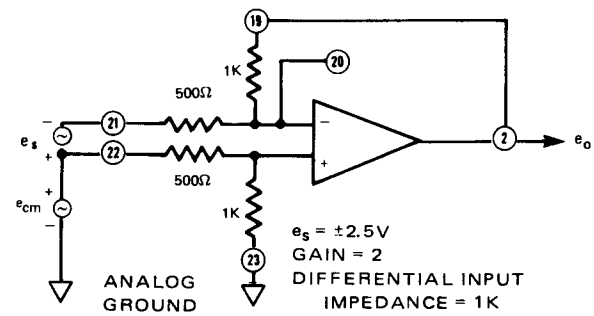


FIGURE 3. BUFFER AMPLIFIER CONNECTED AS DIFFERENTIAL AMPLIFIER

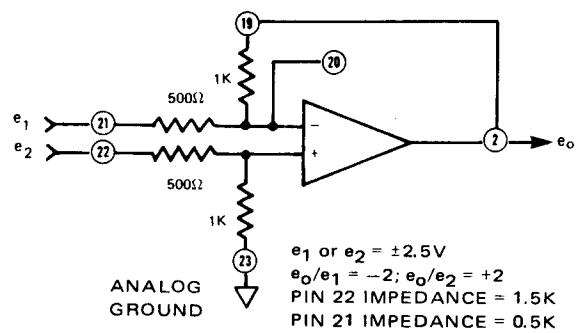
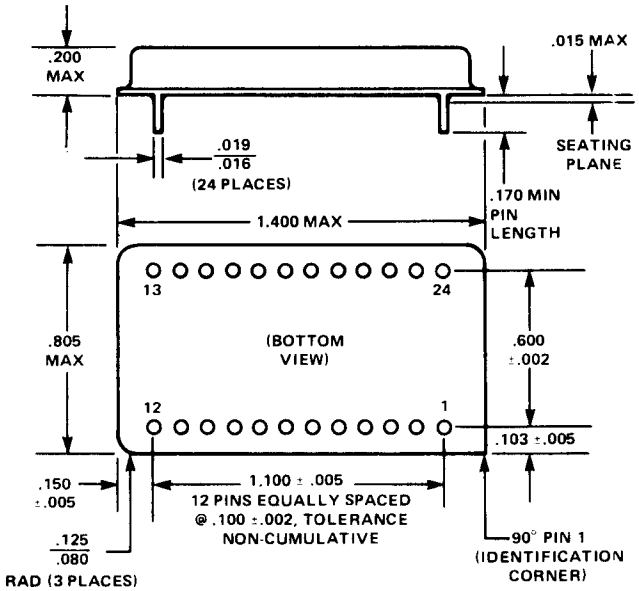


FIGURE 4. BUFFER AMPLIFIER CONNECTED AS SINGLE ENDED AMPLIFIER

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

PIN CONNECTION TABLE

PIN NO.	FUNCTION
1	N.C.
2	Buffer Out
3	T/H Gate In
4	Power Ground
5	-5.2V In
6	N.C.
7	N.C.
8	Vbb In
9	-15V In
10	Power Ground
11	Power Ground
12	+15V In
13	Power Ground
14	N.C.
15	N.C.
16	T/H Output
17	Analog GND
18	T/H Remote Sense (FDBK)
19	Buffer FDBK
20	Buffer S Pt.
21	Buffer (-) In
22	Buffer (+) In No. 1
23	Buffer (+) In No. 2
24	T/H In

Case is connected to Power Ground. Analog Ground is separate from Power Ground.

ORDERING INFORMATION

ADH-050 – 883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - —B = Screened to MIL-STD-883 but without QCI testing.
  - Blank = Screened to MIL-STD-883 but without pre burn-in testing, burn-in, and QCI testing.
- Hold Capacitor Size:
  - 050 = Standard droop rate
  - 051 = 1/5 standard droop rate

B-8/84

C-7/86

When the buffer amplifier is bypassed, the small signal bandwidth and slew rate are somewhat greater, as indicated in the specifications.

3. LOGIC GATE

The ECL gate signal must be high (-0.8V) for the track mode and low (-1.8V) for the hold mode. To ensure positive operation, the -1.3V Vbb voltage supplied to pin 8 on the ADH-050 should come from the gate logic. An ECL gate such as the 10115 includes an appropriate Vbb output generator. When using TTL logic, a TTL to ECL translator such as the 10124 may be used, or a circuit such as shown in Figure 5.

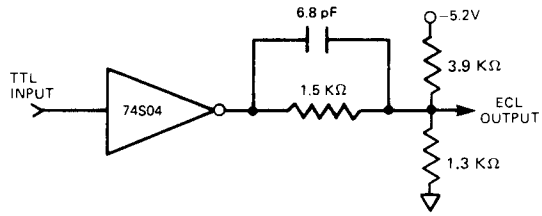


FIGURE 5. CIRCUIT TO PROVIDE ECL GATE FROM TTL LOGIC

4. POWER SUPPLIES

For protection during testing and evaluation, all power supplies should be regulated to ±0.1% and should have current limiting. Set the current limiting for each supply to the maximum value listed in the specifications.

5. OUTPUT AND REMOTE SENSE

A remote sense (pin 18) is available to bypass resistance in the output connections, as shown in Figure 6. Pin 18 must be connected to the output from pin 16 at some point to provide necessary feedback.

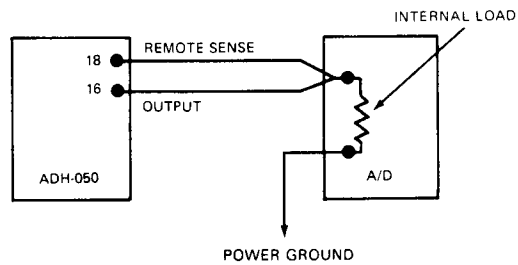


FIGURE 6. OUTPUT CONNECTIONS

6. RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

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