DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

MC-421000AA40 SERIES

1 M-WORD BY 40-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA40 is a 1 048 576 words by 40 bits dynamic RAM module on which 10 pieces of 4 M bits CMOS Dynamic RAM (μPD424400) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1 048 576 words by 40 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA40-60	60 ns	120 ns	6 300 mW	52.5 mW (CMOS level input)
MC-421000AA40-70	70 ns	140 ns	5 250 mW	
MC-421000AA40-80	80 ns	160 ns	4 725 mW	
MC-421000AA40-10	100 ns	190 ns	4 200 mW	

- Fast page mode
- 1 024 refresh cycles / 16 ms
- Three refresh methods can be applied : $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- 40-bit simultaneous switching
- Output buffers control : $\overline{OE}$ pin
- All inputs and outputs TTL compatible
- Single +5.0 V±5 % power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted device
MC-421000AA40B-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Solder coating (HAL)	μPD424400LA 300 mil SOJ×10 (Single side)
MC-421000AA40B-70	70 ns		
MC-421000AA40B-80	80 ns		
MC-421000AA40B-10	100 ns		
MC-421000AA40F-60	60 ns	72-pin Single In-line Memory Module (Socket type) Edge connector : Gold plating	
MC-421000AA40F-70	70 ns		
MC-421000AA40F-80	80 ns		
MC-421000AA40F-10	100 ns		

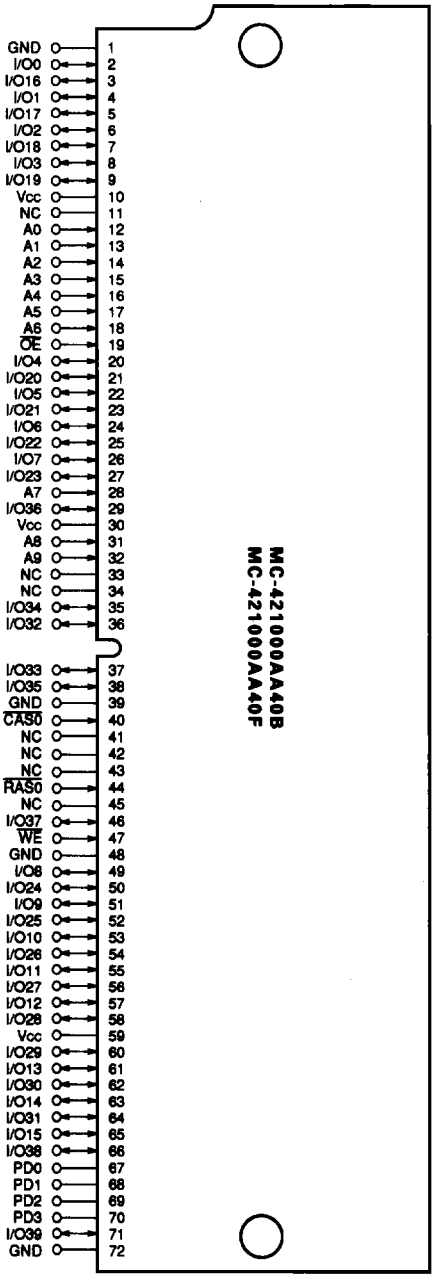
Quality Grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration (Front view)

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder Coating, Gold Plating)

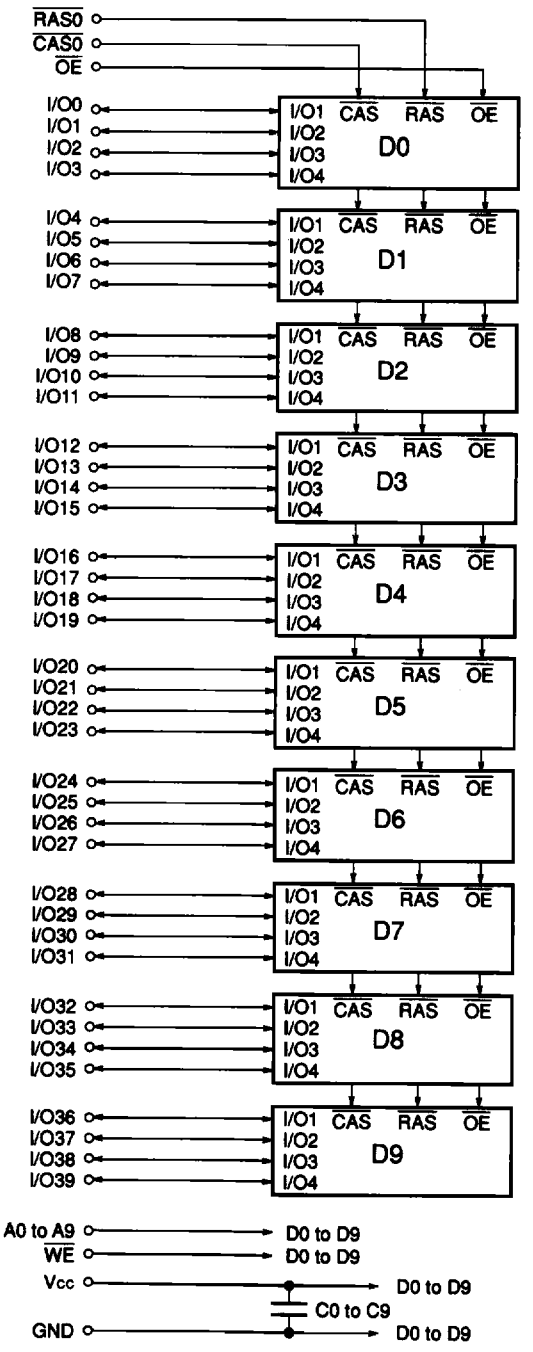


A0 to A9	: Address Inputs
I/O0 to I/O39	: Data Inputs/Outputs
$\overline{CAS0}$	: Column Address Strobe
$\overline{RAS0}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply
GND	: Ground
NC	: No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagram



Remark D0 to D9 : μPD424400LA

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		10	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC}+1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A9			65	pF
	C_{I2}	$\overline{WE}$, $\overline{OE}$			70	
	C_{I3}	$\overline{RAS0}$			60	
	C_{I4}	$\overline{CAS0}$			60	
Data Input/Output capacitance	$C_{I/O}$	I/O0 to I/O39			12	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 200	mA	3,4
			t_{RAC} = 70 ns		1 000		
			t_{RAC} = 80 ns		900		
			t_{RAC} = 100 ns		800		
Standby current	I_{CC2}	$V_{IH(MIN.)} \leq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		20	mA	
		V_{CC}–0.2 V $\leq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		10		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $V_{IH(MIN.)} \leq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 200	mA	3,4
			t_{RAC} = 70 ns		1 000		
			t_{RAC} = 80 ns		900		
			t_{RAC} = 100 ns		800		
Operating current (Fast page mode)	I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS} \leq V_{IL(MAX.)}$ $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		900	mA	3,4
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		700		
			t_{RAC} = 100 ns		600		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 200	mA	3,4
			t_{RAC} = 70 ns		1 000		
			t_{RAC} = 80 ns		900		
			t_{RAC} = 100 ns		800		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	I/O0 to I/O39 are disabled (Hi-Z) V_O = 0 to 5.5 V		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

(1/2)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	120		140		160		190		ns	7
Read Write Cycle Time	t_{RWC}	165		185		210		250		ns	7
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		100		120		ns	7
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t_{AA}		30		35		40		50	ns	8, 9
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	9
Access Time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	9
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	t_{OFF}	0	15	0	15	0	20	0	25	ns	10
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		25		ns	
Output Buffer Turn-off Delay Time ($\overline{OE}$)	t_{OEZ}	0	15	0	15	0	20	0	25	ns	10
$\overline{OE}$ Command Hold Time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time	t_{OES}	0		0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	25	90	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	11
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	12

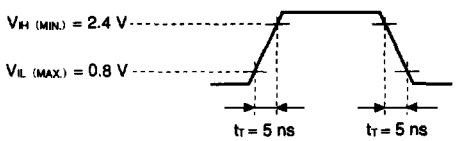
(2/2)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Command Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		20		ns	13
Write Command Pulse Width	t_{WP}	15		15		15		20		ns	13
Data-in Setup Time	t_{DS}	0		0		0		0		ns	14
Data-in Hold Time	t_{DH}	15		15		15		20		ns	14
$\overline{WE}$ Command Setup Time	t_{WCS}	0		0		0		0		ns	15
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		40		45		55		ns	15
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80		90		105		130		ns	15
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)	t_{CPWD}	55		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{WE}$	t_{AWD}	50		55		65		80		ns	15
Write Command Lead Time Referenced to $\overline{RAS}$	t_{RWL}	20		20		20		25		ns	
Write Command Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		20		ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CHR}	15		15		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		20		ns	
Refresh Time	t_{REF}		16		16		16		16	ms	

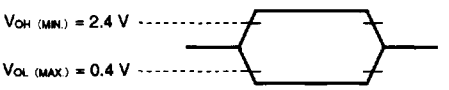
Notes

1. All voltages are referenced to GND.
2. An initial pause of 100 μs is required after power up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on t_{RC} and t_{PC}. Specified values are obtained with outputs open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
5. AC measurements assume t_T = 5 ns.
6. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification

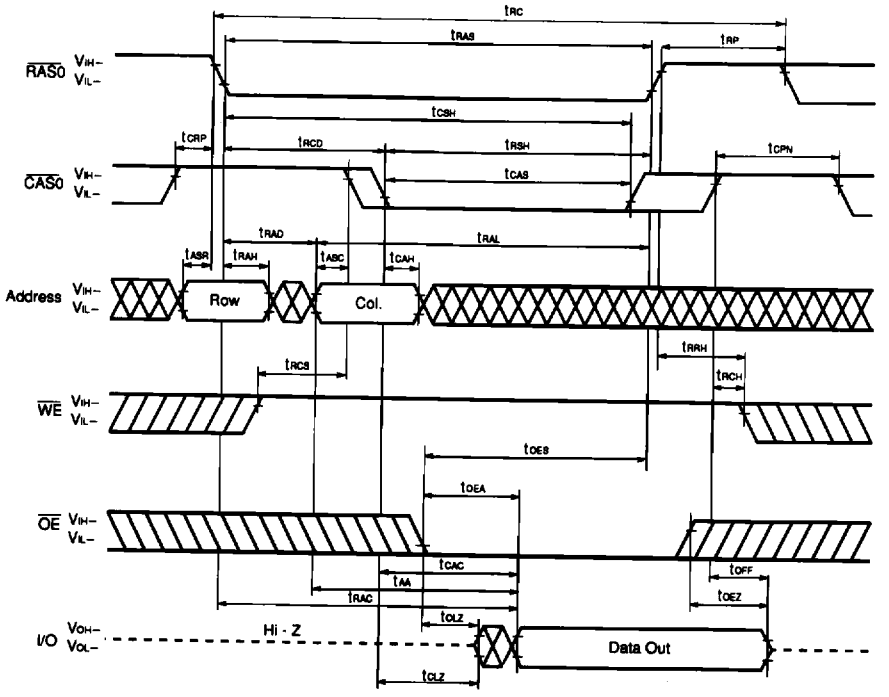


7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.
8. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

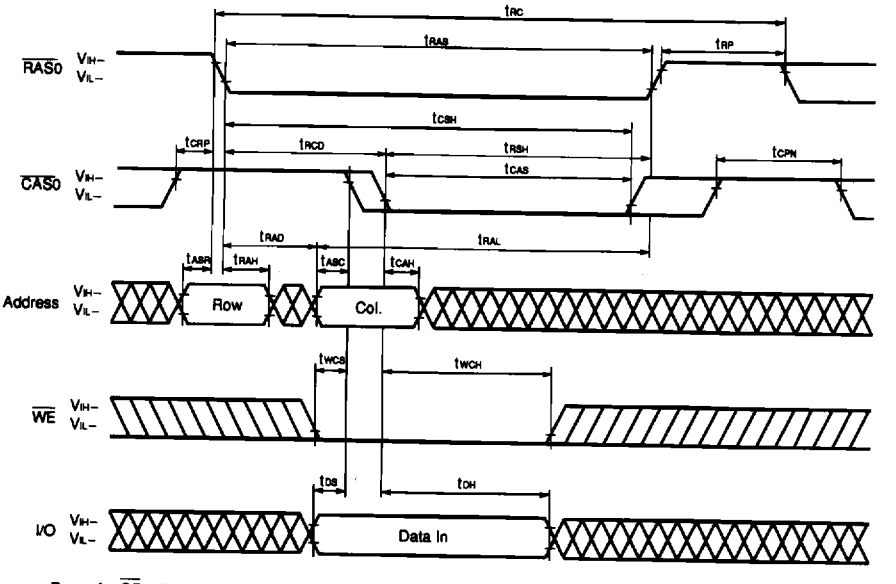
CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD\ (MAX.)} < t_{RAD}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$
$t_{RCD\ (MAX.)} < t_{RCD}$	$t_{CAC\ (MAX.)}$

   $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ indicate the points which the access time changes and are not the limits of operation.
9. Loading conditions are 2 TTL and 100 pF.
10. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
11. $t_{CRP\ (MIN.)}$ requirement should be applicable for $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
12. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ must be satisfied for a read cycle.
13. $t_{WP\ (MIN.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\ (MIN.)}$ should be satisfied.
14. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
15. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$, $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above condition is met, the condition of the data out is indeterminate.

Read Cycle

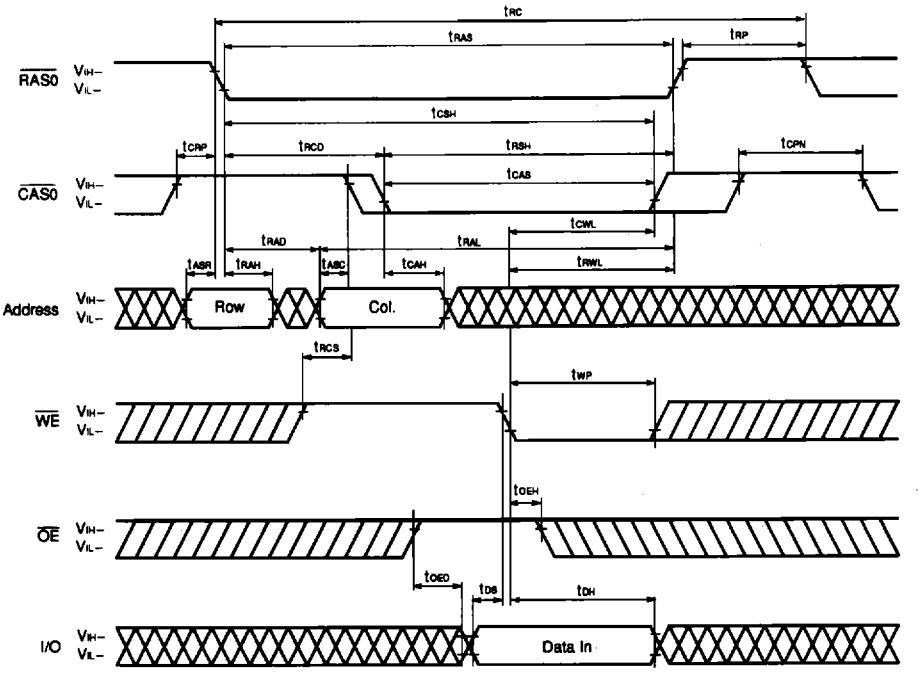


Early Write Cycle

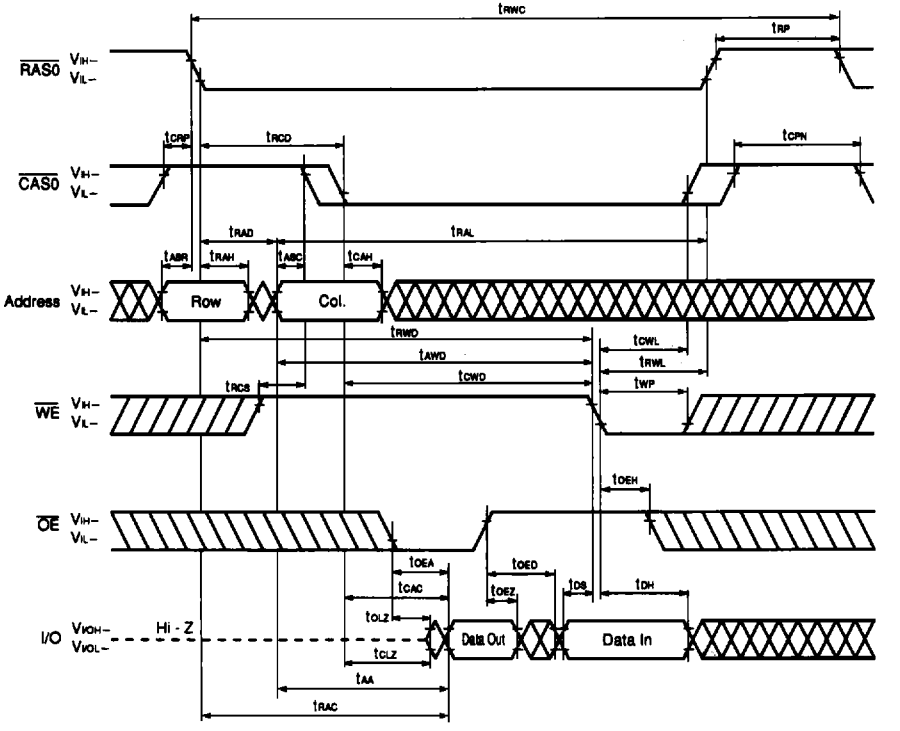


Remark $\overline{OE}$ = Don't Care

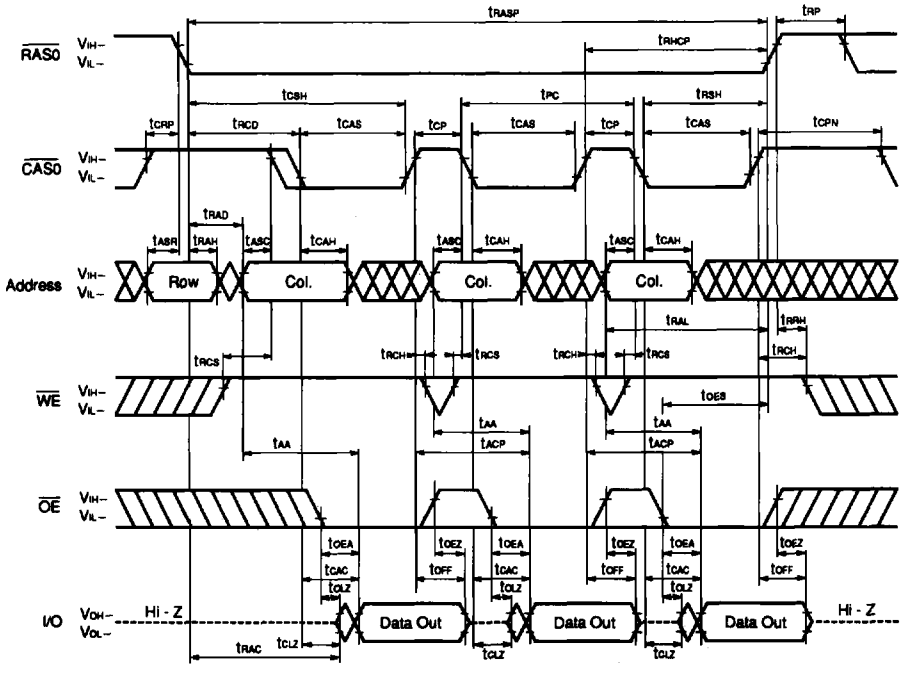
Late Write Cycle



Read Modify Write Cycle

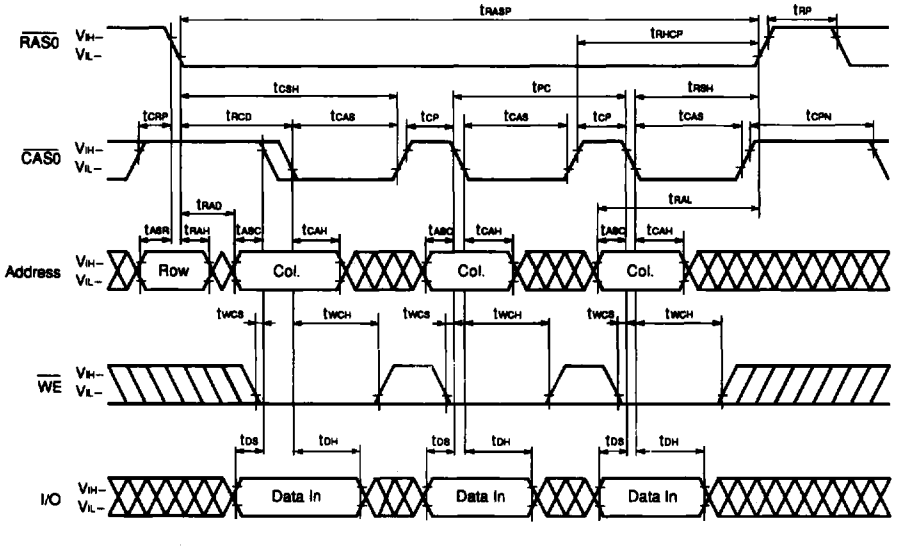


Fast Page Mode Read Cycle



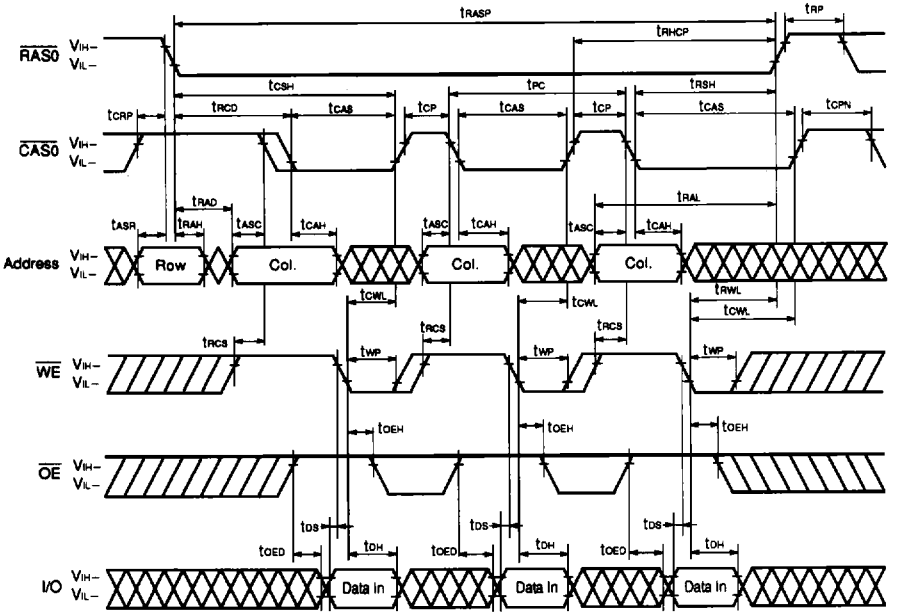
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



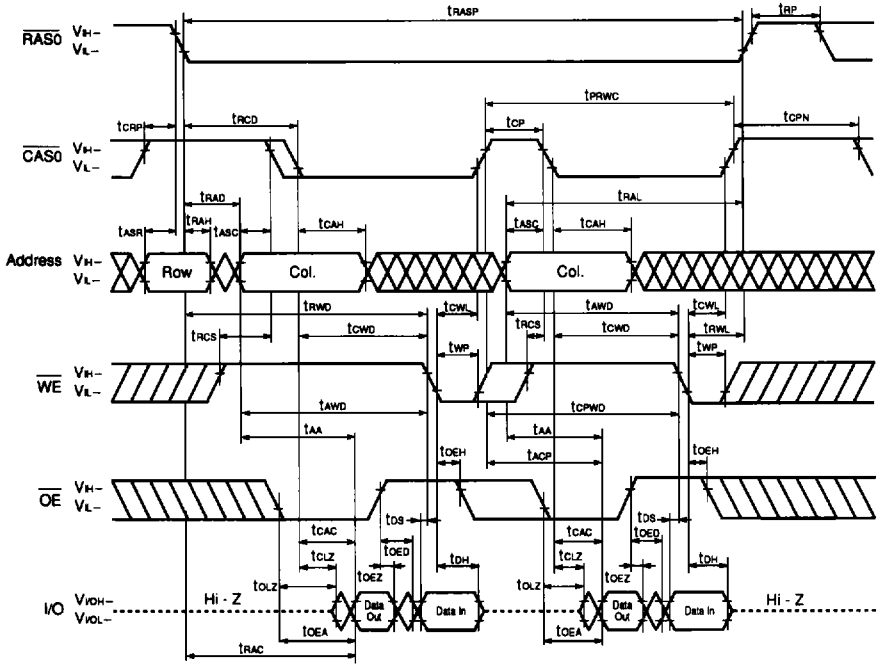
Remark $\overline{OE}$ = Don't Care
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



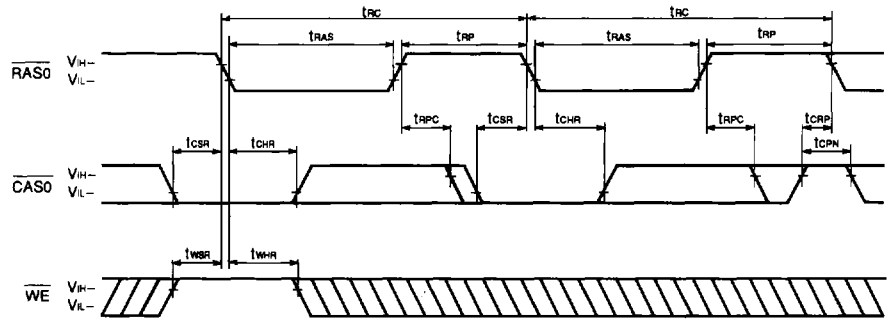
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



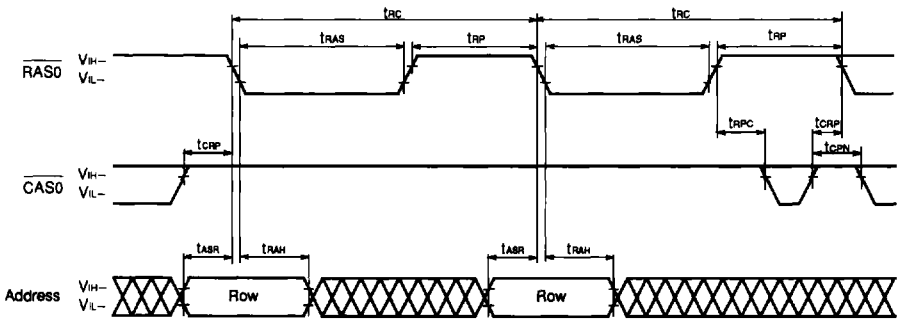
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



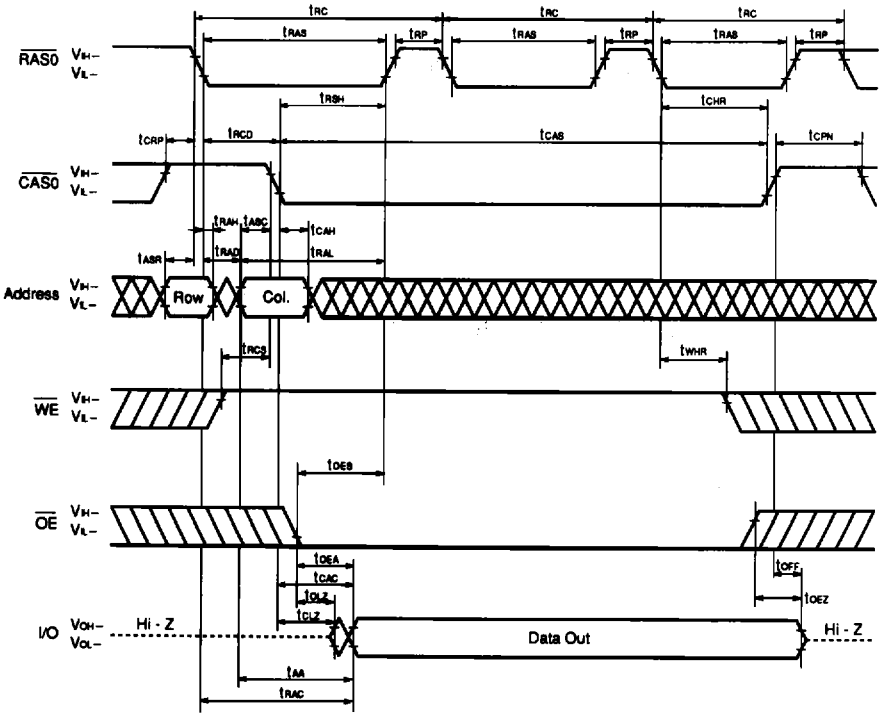
Remark Address, $\overline{OE}$ = Don't care I/O = Hi - Z

$\overline{RAS}$ Only Refresh Cycle



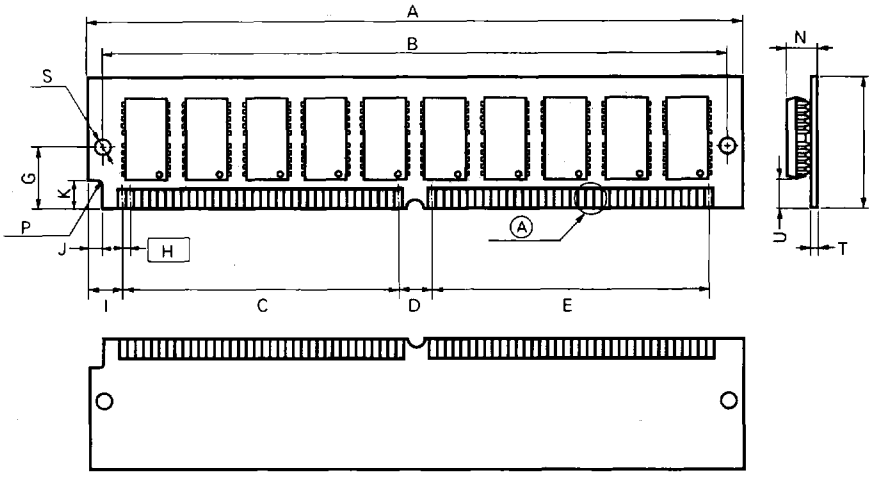
Remark $\overline{WE}$, $\overline{OE}$ = Don't care I/O = Hi - Z

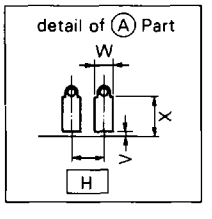
Hidden Refresh Cycle



Package Drawing

MC-421000AA40B, 421000AA40F
72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





M72B-50A26-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	$1.27^{+0.10}_{-0.08}$	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.