DPS128M8

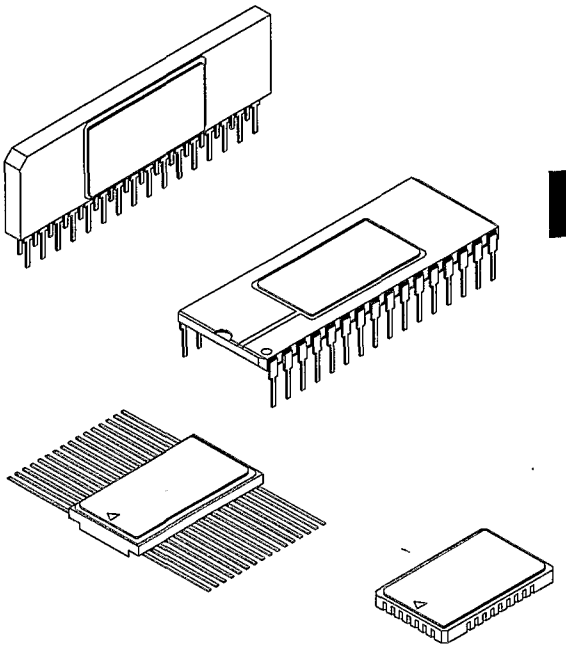
CERAMIC 128K X 8 CMOS SRAM MONOLITHIC

DESCRIPTION:

The DPS128M8 is a monolithic 128K X 8 Static Random Access Memory (SRAM) fabricated using CMOS technology. It is designed for use in high density, high speed, low power applications. All pins are TTL compatible and a single +5 Volt power supply is required.

The DPS128M8 has extremely low standby power dissipation making it suitable for battery backup.

The 600-mil wide, 32-pin ceramic, Dual-In-Line Package (DIP), conforms to the JEDEC standard. Dense-Pac also offers a 32-pin ceramic FLATPACK, a 32-Pad Leadless Chip Carrier (LCC), and a space saving 32-pin Zig-Zag-In-Line Package (ZIP).



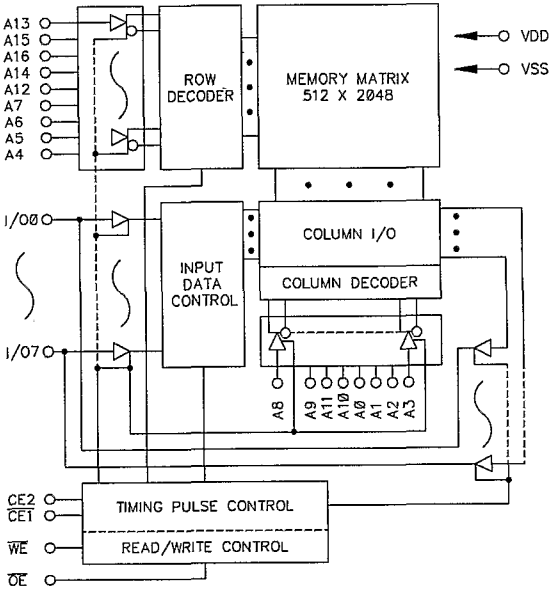
FEATURES:

- 131,072 by 8-Bits Organization
- Access Times: 70*, 85, 100, 120, 150ns (max.)
- Low Power: 10µW (typ.) Standby
  225mW (typ.) Operating
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Two Chip Enables
- Output Enable Functions
- Faster Access Speeds Available Upon Request
- Package Types:
  32-Pin Ceramic Side Brazed DIP
  32-Pin Ceramic FLATPACK
  32-Pin Ceramic ZIP
  32-Pad Ceramic LCC

* Commercial Only

PIN NAMES	
A0-A16	Address Inputs
I/O0-I/O7	Data In/Out
$\overline{CE1}$ / CE2	Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



FOR FURTHER INFORMATION
SEE CHAPTER 3
FOR COMPLETE DATA SHEET

DPS128M8A

HIGH SPEED CERAMIC
128K X 8 CMOS SRAM MONOLITHIC

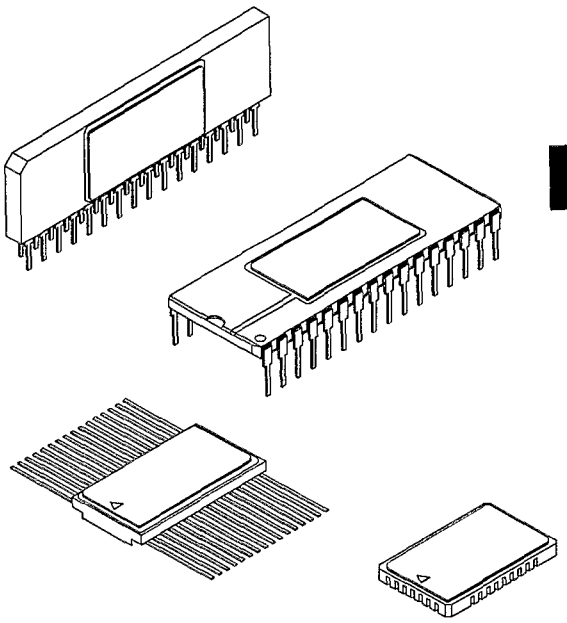
ADVANCED INFORMATION

DESCRIPTION:

The DPS128M8A is a high speed monolithic 128K X 8 Static Random Access Memory (SRAM) fabricated using CMOS technology. It is designed for use in high density, high speed, low power applications. All pins are TTL compatible and a single +5 Volt power supply is required.

The DPS128M8A has extremely low standby power dissipation making it suitable for battery backup.

The 600-mil wide, 32-pin ceramic, Dual-In-Line Package (DIP), conforms to the JEDEC standard. Dense-Pac also offers a 32-pin ceramic FLATPACK, a 32-Pad Leadless Chip Carrier (LCC), and a space saving 32-pin Zig-Zag-In-Line Package (ZIP).



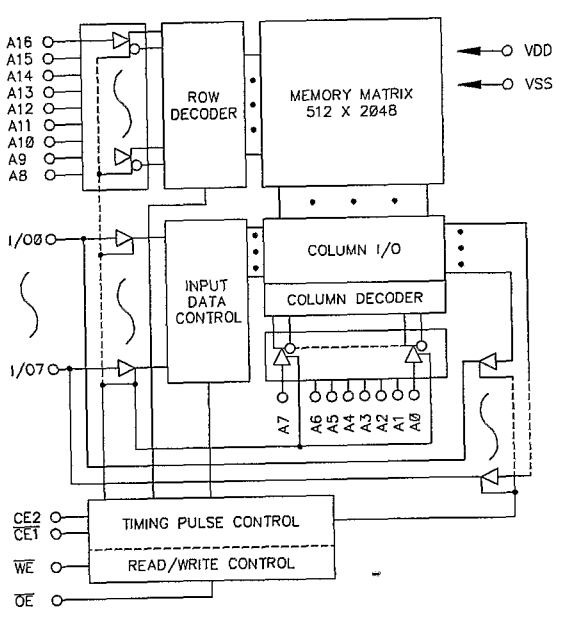
FEATURES:

- 131,072 by 8-Bits Organization
- Access Times: 35*, 45, 55, 70ns (max.)
- Low Power: 50µW (typ.) Standby
  300mW (typ.) Operating
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Two Chip Enables
- Output Enable Functions
- Faster Access Speeds Available Upon Request
- Package Types:
  32-Pin Ceramic Side Brazed DIP
  32-Pin Ceramic FLATPACK
  32-Pin Ceramic ZIP
  32-Pad Ceramic LCC

* Commercial Only

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE1}$, CE2	Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



FOR FURTHER INFORMATION
SEE CHAPTER 3
FOR COMPLETE DATA SHEET