Rockwell

R23C64
64K (8K × 8) CMOS ROM

PRELIMINARY

DESCRIPTION

The Rockwell R23C64 is an 8K × 8 (65,536 bits) CMOS read-on-memory (ROM) housed in a 28-pin JEDEC standard package. It is fabricated in CMOS technology to achieve high performance with extremely low power dissipation. This device is available with maximum access times of 150, 250, or 300 nanoseconds, latched or non-latched chip selects, optional extended temperature range, and packaged in ceramic or low-cost plastic.

The R23C64 is controlled via the chip enable ($\overline{E}$) and the mask programmable output enable (G/$\overline{G}$/N) and chip selects (S1/$\overline{S1}$/N and S2/$\overline{S2}$N). The address is latched on the falling edge of $\overline{E}$, allowing the R23C64 to operate on a multiplexed bus as well as a non-multiplexed bus. The output enable and chip selects control the output buffers, however, these buffers do not become active until valid data is present from the internal data latches. This prevents spurious, invalid outputs that increase power dissipation. When $\overline{E}$ is high, the output buffers are in the high impedance state and the address, output enable and chip select pins are ignored (standby). $\overline{E}$ may also be held low indefinitely, keeping the address latched and the output buffers under output enable and chip select control. The R23C64 is in a low-power quiescient active mode when $\overline{E}$ is low and the other control inputs (G, S1 and S2) are steady state.

FEATURES

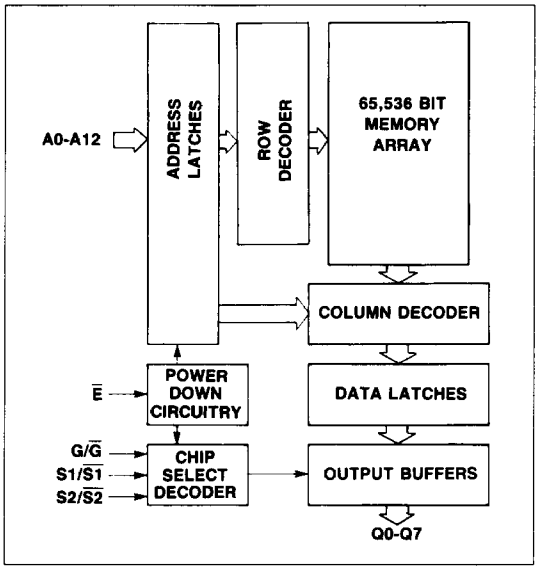
- 8,192 × 8 organization
- JEDEC standard pinout
- Extremely low power
  - — Active 10 mW/MHz (max.)
  - — Active quiescent 50 μW (max.)
  - — Standby 50 μW (max.)
- Fast access times: 150 ns, 250 ns and 300 ns (max.)
- Mask programmable chip selects and output enable
- Latched addresses and (optional) latched chip selects
- Drives two TTL loads and 100 pF
- Single 5V ±10% power supply
- Pin compatible with Mostek MK37000

ORDERING INFORMATION

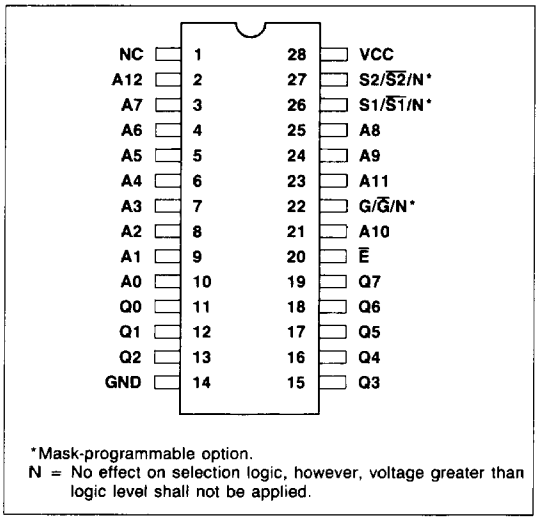
Part Number: R23C64 _ _ _ _

- Package:
  - C = Ceramic
  - P = Plastic
- Temperature Range:
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Access Time (Max):
  - 15 = 150 ns
  - 25 = 250 ns
  - 3 = 300 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.



R23C64 Block Diagram



*Mask-programmable option.
N = No effect on selection logic, however, voltage greater than logic level shall not be applied.

R23C64 Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Temperature Under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P	1.0	W

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ±10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[3]	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −200 μA
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.2 mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.3		0.8	V	
I_{LI}	Input Load Current			±1	μA	V_{CC} = 5.5V, 0V < V_{IN} < 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC1}	Power Supply Current, Active			2	mA	t_{ELQV} = 150 ns[1], V_{CC} = 5.5V
I_{CC2}	Power Supply Current, Standby			10	μA	$\overline{E}$ = V_{CC} −0.5V; all other pins active
I_{CC3}	Power Supply Current, Active Quiescent			10	μA	$\overline{E}$ = V_{IL} $\overline{G}$ = $\overline{S1}$ = $\overline{S2}$ = Steady State (V_{IL} or V_{IH})
C_I	Input Capacitance (all but $\overline{E}$)[2] ($\overline{E}$)			7 10	pF pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C, f = 1 MHZ
C_O	Output Capacitance[2]			10	pF	

Notes:
1. t_{ELEH} = 150 ns, all pins active, no loads, 1 μs cycle time (t_{ELEL} = 1 μs).
2. This parameter is periodically sampled and is not 100% tested.
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R23C64-15		R23C64-25		R23C64-3		Unit
		Min	Max	Min	Max	Min	Max	
t_{ELEL}	Cycle Time	220		365		465		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	150		250		300		ns
t_{EHEL}	Chip Enable High to Chip Enable Low	60		100		150		ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		150		250		300	ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	50		65		80		ns
t_{GVQV}	Output Enable Valid to Output Valid	75		100		150		ns
t_{EHQX}	Chip Enable High to Output Invalid	10		10		10		ns
t_{GXQX}	Output Enable Invalid to Output Invalid	10		10		10		ns
t_{EHQZ}[4]	Chip Enable High to Output High Z		50		65		70	ns
t_{GXQZ}[4]	Output Enable Invalid to Output High Z		60		75		90	ns
t_F, t_R	Rise and Fall Times[2]		10		15		20	ns

Notes:

1. Test Conditions: Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V; Output: 0.8V, 2.0V.
2. Rise and Fall times stated are required for these high performance parameters only and may be relaxed for slower operation, e.g., 100 kHz operation.
3. $\overline{G}$ may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
4. t_{EHQZ}, t_{GHQZ} are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

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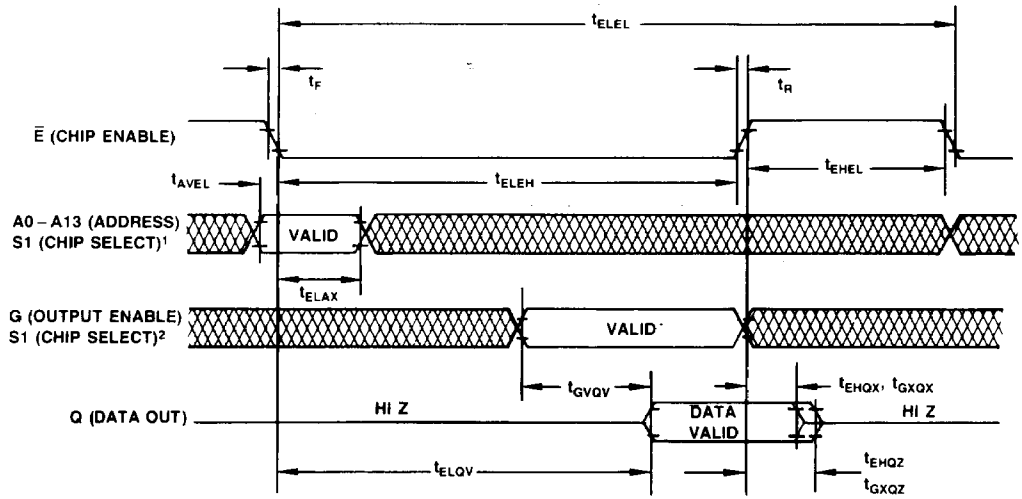
TIMING DIAGRAM

READ CYCLE TIMING

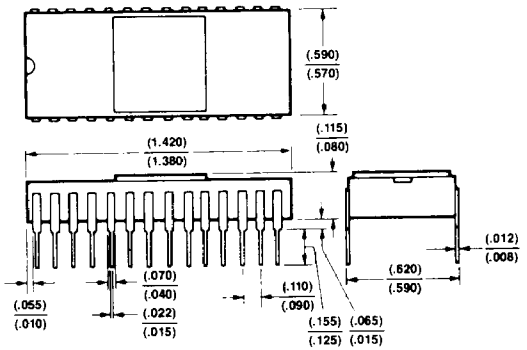


NOTES:

1. **CHIP SELECTS (S1/$\overline{S1}$ AND S2/$\overline{S2}$) LATCHED.**
2. **CHIP SELECTS (S1/$\overline{S1}$ AND S2/$\overline{S2}$) NOT LATCHED.**

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP