PHAST®-12P Device

STM-4/OC-12 SDH/SONET Overhead Terminator with CDB/PPP UTOPIA/POS-PHY Interface

TXC-06412B

DATA SHEET

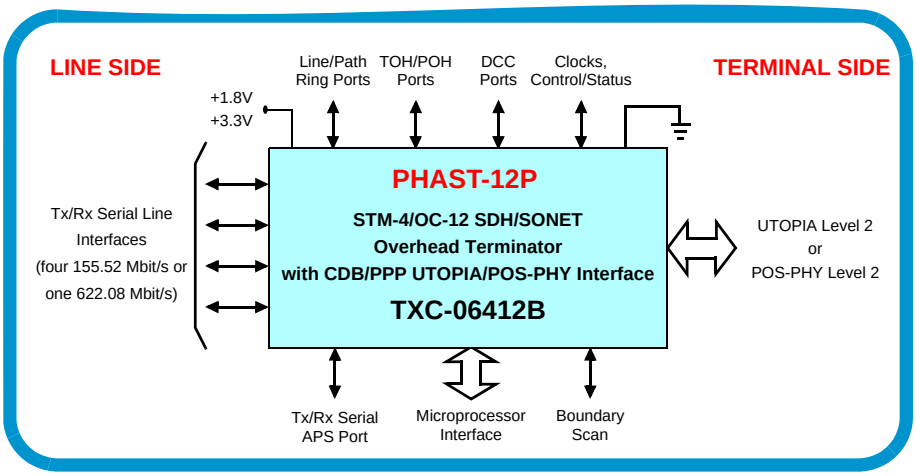
TXC-06412B-MB, Ed. 6
April 2009

FEATURES

- Bit-serial LVPECL SDH/SONET line interface with integrated clock recovery and clock synthesis
  - Single 622.08 Mbit/s STM-4/OC-12 signal or
  - Four 155.52 Mbit/s STM-1/OC-3 signals
- Bit-serial LVDS 622.08 Mbit/s APS port
- Supports 1+1, 1:1 and 1:n APS for STM-1/OC-3 and STM-4/OC-12 signals using a serial port interface
- Complete RS/section and MS/line overhead processing
- Complete high order path overhead processing at VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STC-6c/STS-9c/STS-12c SPE level
- High order path cross connect with VC-3/STS-1 SPE granularity
- ATM cell handling
- PPP packet handling
- UTOPIA Level 2 16-bit interface at 50 MHz
- POS-PHY Level 2 16-bit interface at 50 MHz
- MS/Line or RS/Section DCC access port per line
- Ring Ports for line/path ring applications
- TOH and POH access port
- 16-bit wide microprocessor interface, selectable between Motorola or Intel
- Software device driver is provided
- Boundary scan and line loopback
- +3.3V and +1.8V power supplies, 3.3V digital I/O leads
- 376-lead plastic ball grid array (PBGA) package (23 mm x 23 mm)

APPLICATIONS

- SDH/SONET add/drop and terminal multiplexers
- Linear MS/Line protection
- ATM and packet switches
- Multiservice applications



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LIST OF FIGURES

LIST OF TABLES

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated PHAST-12P device Data Sheet that have significant differences relative to the previous and now superseded PHAST-12P Data Sheet:

Updated PHAST-12P device Data Sheet: Edition 6, April 2009

Previous PHAST-12P device Data Sheet: Edition 5, December 2007

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
2	Removed two patent numbers at bottom left corner.
2	Updated Patent List.
3-10	Updated “Table of Contents”, “List of Figures” and “List of Tables”.
13	Updated “List of Data Sheet Changes”.
75	Added footnote “c” and “d” to Table 3
80	Added Note below Figure 29
194	Added “Bit Transmisssion Order“ to the paragraph in introduction of Memory Maps.
214	Updated RDI_value description in Table 40.

APPLICABLE STANDARDS DOCUMENTATION

Standards documents applicable to the functions of the PHAST®-12P device are listed below.

Short Name	Description
ANSI T1.105	SONET - Basic description including Multiplex structure, rates and formats, 2001
ANSI T1.105.02	Synchronous Optical Networks (SONET), Payload Mappings, 2001
ANSI T1.107	Digital Hierarchy - Formats Specifications, 1995
ATM Forum af-phy-0039.00	UTOPIA Level 2, version 1.0 (06/95)
ETSI EN 300-417 1-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - Generic processes and performance
ETSI EN 300-417 2-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - SDH and PDH physical section layer functions
ETSI EN 300-417 3-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - STM-N regenerator and multiplex section layer functions
ETSI EN 300-417 4-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - SDH path layer functions
ETSI EN 300-417 9-1	Transmission and Multiplexing (TM) - Generic requirements of transport functionality of equipment - SDH concatenated path layer functions; Sub-part 1: Requirements
IEEE 1149.1	Standard Test Access Port and Boundary Scan Architecture (May 21, 1990)
IEEE 1596.3	Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) (March 21, 1996)
IETF RFC 1662	PPP in HDLC-like Framing (07/94)
IETF RFC 2615	PPP over SONET/SDH (06/99)
ITU-T I.432	B-ISDN user-network interface - Physical layer specification (02/1999)
ITU-T G.707/Y.1322	Network Node interface for the Synchronous Digital Hierarchy (SDH) (10/2000)
ITU-T G.783	Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks (10/2001)
ITU-T G.803	Architecture of transport networks based on the SDH (03/2000)
ITU-T G.805	Generic functional architecture of transport networks (03/2000)
ITU-T G.806	Characteristics of transport equipment - Description methodology and generic functionality (10/2000)
POS PHY	POS-PHY Level 2, PMC-971147, issue 5: December 1998 Saturn Compatible Packet over SONET Interface specification for physical layer devices
Telcordia GR-253-CORE	SONET Common Generic Criteria, Rev 3, September 2000
Telcordia GR-499-CORE	Transport Systems Generic Requirements: Common Requirements, Issue 2, December 1998

OVERVIEW

The PHAST®-12P is a highly integrated SDH/SONET overhead terminator device designed for ATM cell or PPP packet payload mappings. A single PHAST-12P can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line. Each SDH/SONET terminator has a line interface block that performs clock synthesis and clock recovery for four 155.52 Mbit/s signals or a single 622.08 Mbit/s serial signal. It provides glueless 1+1, 1:1 and 1:n APS for STM-1/OC-3 and STM-4/OC-12 applications using a 622.08 Mbit/s serial APS port interface.

The PHAST-12P performs RS (section) and MS (line) overhead processing, high order pointer tracking and retiming, and high order path overhead processing and performance monitoring. It contains a full non-blocking cross connect at the high order path level with VC-3/STS-1 SPE granularity allowing path loopbacks, MS or line protection and UPSR and SNC/P path protection. It can terminate ATM payloads from any of the above signals into a 16-bit UTOPIA Level 2 PHY interface. PPP payloads are terminated into a 16-bit wide POS-PHY Level 2 interface.

Fully functional Device Driver software exists including comprehensive API's, documentation and sample application code which is made available on-line for registered users or through TranSwitch Applications Engineering group. The sample applications represent different modes of operation for the device with the proper procedures and sequencing of routines that may contain multiple API's and parameters to more easily implement these specific applications.

The PHAST-12P device provides RS/section and MS/line overhead processing, high order AU-3/AU-4/AU-4-Xc/STS-1/STS-3c/STC-6c/STS-9c/STS-12c pointer tracking and retiming, and high order VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE path overhead processing and performance monitoring. It provides full non-blocking cross connecting at the high order path level allowing path loopbacks, line/MSP protection and UPSR and SNC/P path protection.

The device supports the following APS architectures:

1. STM-4/OC-12 mode: 1+1 or 1:1 APS using two devices connected via the APS port
2. STM-1/OC-3 mode: 1+1, 1:1 or 1:n (n<=3) APS using a single device without APS port
3. STM-1/OC-3 mode: 1+1, 1:1 or 1:n (n<=7) APS using two devices connected via the APS port

The device operates from 1.8V and 3.3V power supplies.

Major interfaces include:

1. Serial LVPECL line interfaces: single STM-4/OC-12 or four STM-1/OC-3
2. UTOPIA Level 2 bus interface
3. POS-PHY Level 2 bus interface
4. 622.08 Mbit/s serial LVDS APS port interface
5. Line/MS Alarm/Ring port selectable per line interface
6. SOH/TOH byte interface
7. DCC interface
8. High Order Path Alarm/Ring port selectable per SDH/SONET path
9. High Order POH byte interface
10. Motorola/Intel style microprocessor interface for configuration, alarms and performance monitoring
11. JTAG interface to IEEE 1149.1
12. Various reference clocks, and lead programmed HW configuration controls

The PHAST-12P software driver has the same architecture as other TranSwitch device drivers and is meant to be easily integrated with them. The application software calls the driver functions to configure, control and manage the PHAST-12P device. The device driver insulates the application from the internal details of the device register usage and provides a higher level of abstraction.

FEATURES

The following is a list of features supported by the PHAST-12P:

Modes of Operation

- Line interfaces:
  - Four STM-1/OC-3 line interfaces, or
  - One STM-4/OC-12 line interface[1]
- ATM/PPP operation:
  - ATM cell delineation, UTOPIA Level 2 interface, or
  - PPP packet delineation, POS-PHY Level 2 interface
- SDH/SONET mapping:

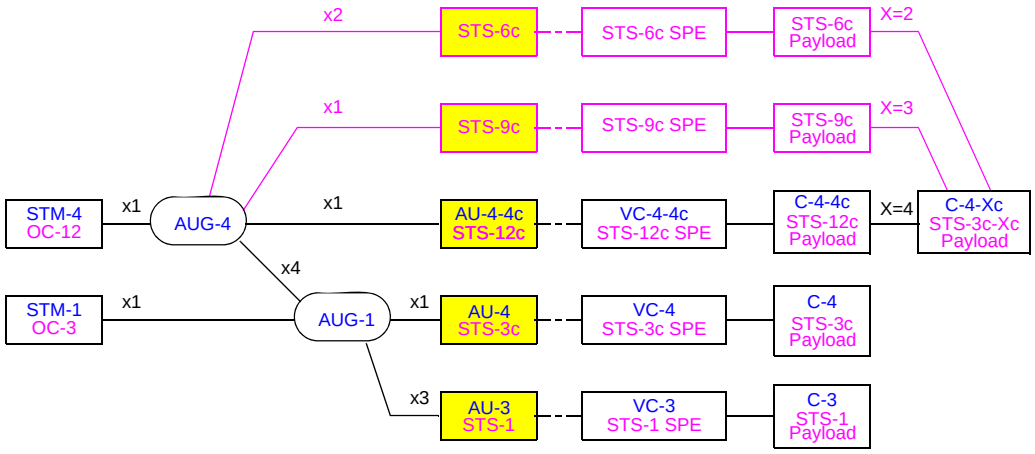


Figure 1. Supported SDH/SONET Mapping

Line Interface

- LVPECL serial line interfaces:
  - Line Interface #1 can handle 155.52 Mbit/s (STM-1/OC-3 mode) or 622.08 Mbit/s (STM-4/OC-12 mode) signals
  - Line Interfaces #2 to #4 handle 155.52 Mbit/s signals and are only used in STM-1/OC-3 mode

1. The term STM-4c/OC-12c is sometimes used to denote a STM-4/OC-12 interface transporting a contiguous concatenated VC-4-4c/STS-12c SPE high order path. The STM-4/OC-12 mode of operation allows transport of any type of high order path container. ITU-T/ANSI compliant terminology will be used throughout this document.

- Transmit clock synthesis
- Per Line Interface:
  - Receive clock recovery
  - Loss of Signal detection
  - Receive 19.44 MHz (STM-1/OC-3 mode) or 77.76 MHz (STM-4/OC-12 mode) clock output reference
  - General purpose input/output pins

APS Port Interface

- Single 622.08 Mbit/s LVDS serial interface:
  - Receive clock recovery
  - Transmit clock synthesis
  - Receive 77.76 MHz clock output reference
  - Transport of high order path data for four STM-1/OC-3 signals or one STM-4/OC-12 signal between two PHAST-12P devices
  - Transport of K1/K2 APS signal, signal fail and signal degrade indications for up to four lines between two PHAST-12P devices
- The APS port transports the payload and APS signaling between two mate devices. The APS finite state machine itself needs to be implemented by the external host software. The resulting bridge and switch requests are performed by configuring the cross connect.

RS/Section Layer Processing

- A1/A2 frame alignment
  - Out of frame and loss of frame detection
- J0 Trail Trace Identifier:
  - Insertion and monitoring of single repeating byte and 16-byte trace messages
  - Trace identifier mismatch detection
- Scrambling and descrambling
- B1 BIP-8 insertion and monitoring
- D1-D3 DCC accessible via the DCC port
- All received RSOH bytes are stored in on-chip memory and transmitted on the TOH port
- All RSOH bytes can be inserted from on-chip memory or from the TOH port

MS/Line Layer Processing

- B2 BIP-24/96 insertion and monitoring
  - Degraded signal and excessive bit error detection
  - Block and bit error performance monitoring counters
- D4-D12 DCC can be accessible via the DCC port
- Insertion and monitoring of remote information (RDI, REI)
- Insertion and monitoring of MS/line AIS
- Insertion and monitoring of the K1/K2 APS signal
- Insertion and monitoring of the S1 synchronization status message (SSM)
- All received MSOH bytes are stored in on-chip memory and transmitted on the TOH port
- All MSOH bytes can be inserted from on-chip memory or from the TOH port

High Order Path Layer Processing

- J1 Trail Trace Identifier:
  - Insertion and monitoring of single repeating byte, 16-byte and 64-byte trace messages
  - Trace identifier mismatch detection
- B3 BIP-8 insertion and monitoring
  - Degraded signal and excessive bit error detection
  - Block and bit error performance monitoring counters
- C2 Trail Signal Label insertion and monitoring
  - Unequipped, VC-AIS, payload mismatch detection
- G1 insertion and monitoring
  - Single bit RDI and three bit E-RDI
  - REI insertion and block/bit performance monitoring counter
- K3 insertion and monitoring
  - Automatic Protection Switching detection
- Unequipped and Supervisory Unequipped generation and detection
- Unidirectional mode
- All received POH bytes are stored in on-chip memory and transmitted on the POH port
- All POH bytes can be inserted from on-chip memory except for B3, which is used as an errormask

High Order Path Cross Connect

- Non-blocking 36x36 cross connect:
  - 3 input and 3 output ports: line side, APS port and terminal side
  - 12 time slot channels per port
- VC-3/STS-1 SPE granularity allowing cross connecting at VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE level
- Path loopbacks and multi-casts are supported
- Each individual output channel can be forced to source an AIS or unequipped maintenance signal

ATM Cell Handling

- Egress: ATM cell demapping from SDH/SONET streams
  - Cell delineation including header error detection and correction
  - HEC checking
  - Filtering of idle cells, unassigned cells, user defined pattern cells, cells with uncorrected HEC error
  - Detection of loss of cell delineation and RDI-P insertion
  - Detection of Rx FIFO overflow
  - Performance counters
- Ingress: ATM cell mapping into SDH/SONET streams
  - HEC checking, calculation and insertion
  - Insertion of idle, unassigned and user defined pattern cells
  - Performance counters

PPP Packet Handling

- Egress: PPP packet demapping from SDH/SONET streams
  - Descrambling
  - Address/control fields checking and stripping
  - HDLC framing and byte destuffing, including escape character discarding
  - FCS checking and stripping
  - 32/16 bit FCS
  - Detection of Rx FIFO overflow
  - Discarding of too short and too long frames
  - Discarding of frames with abort sequence
  - Performance counters
  - Optional Transparent demapping
- Ingress: PPP packet mapping into SDH/SONET streams
  - Address/control fields insertion
  - FCS insertion
  - 32/16 bit FCS
  - HDLC flag insertion and byte stuffing, including escape character insertion
  - Optional multiple flag insertion
  - Scrambling
  - Detection of Tx FIFO underflow
  - Detection of errored packets and insertion of abort sequence
  - Performance counters
  - Optional Transparent mapping

UTOPIA Level 2 Interface (PHY Layer)

- Pins shared with POS-PHY level 2 interface
- 16 bit data bus width
- Maximum clock speed 50 MHz
- Cell level handshaking for up to twelve high order path cell streams
- Single-PHY or multi-PHY mode
- Status indication modes
  - Direct status indication, see [UTOPIA Level 2] section 4.3: at most 4 CLAV's are used, at most 4 PHY's are possible
  - Multiplexed status polling with full address, see [UTOPIA Level 2] section 4.2: 1 CLAV signal (CLAV0) is used, at most 31 PHY's are possible
  - Multiplexed status polling with group address, see [UTOPIA Level 2] section 4.4: 4 CLAV signal are used, at most 31 PHY's are possible
- Odd/even parity over data or data and control signals
- Detection of unexpected or missing SOC

POS-PHY Level 2 Interface (PHY Layer)

- Pins shared with UTOPIA level 2 interface
- 16 bit data bus width
- Maximum clock speed 50 MHz
- Packet level handshaking for up to twelve high order path packet streams
- Single-PHY or multi-PHY mode
- Status indication modes
  - Direct status indication: at most 4 DTPA's are used, at most 4 PHY's are possible
  - Multiplexed status polling with full address: 1 PTPA signal (PTPA0) is used, at most 31 PHYs are possible
- Odd/even parity over data or data and control signals
- Detection of missing SOP and missing EOP

Microprocessor Interface

- Bidirectional 16-bit wide Data bus (allowing 16-bit word accesses only)
- 14-bit wide Address bus
- The following microprocessor interface modes are supported:
  - Generic Motorola mode
  - Generic Intel mode (with separate address/data bus)
  - MPC860 mode
  - MPC8260 Local Bus mode
- Interrupt request lead
- Interrupt mask bits for controlling generation of hardware interrupt requests

Testing

- Line loopbacks
- High order path loopbacks via the cross connect
- Boundary scan

Device Driver

- Device configuration
- Fault monitoring
- Performance monitoring

APPLICATION EXAMPLES

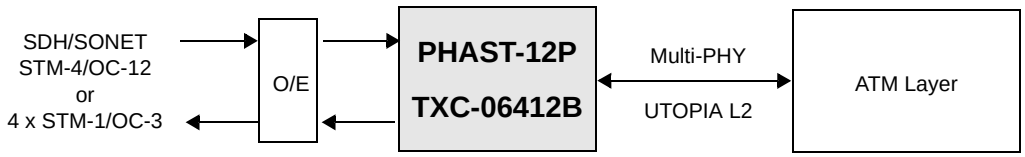


Figure 2. STM-4/OC-12 or 4 x STM-1/OC-3 ATM DSLAM Network Card

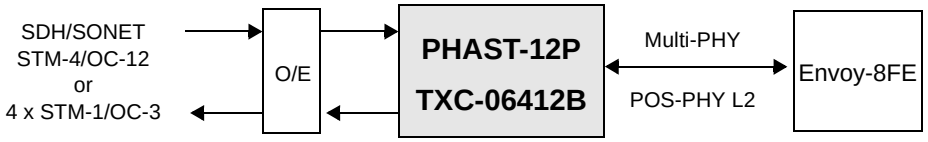


Figure 3. STM-4/OC-12 or 4 x STM-1/OC-3 IP (PPP) DSLAM Network Card

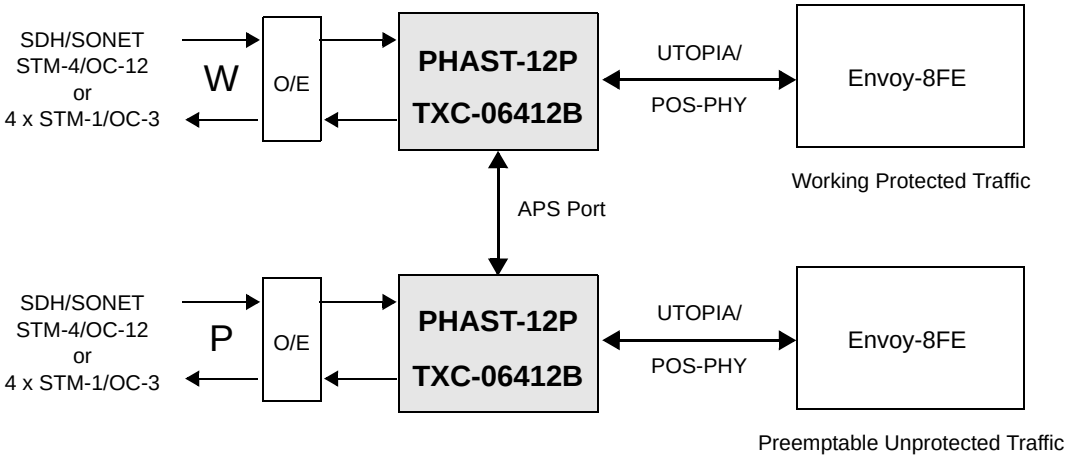


Figure 4. STM-4/OC-12 or 4 x STM-1/OC-3 1+1, 1:1 APS Line Protection

1.0 DEVICE DESCRIPTION

1.1 BLOCK DIAGRAM

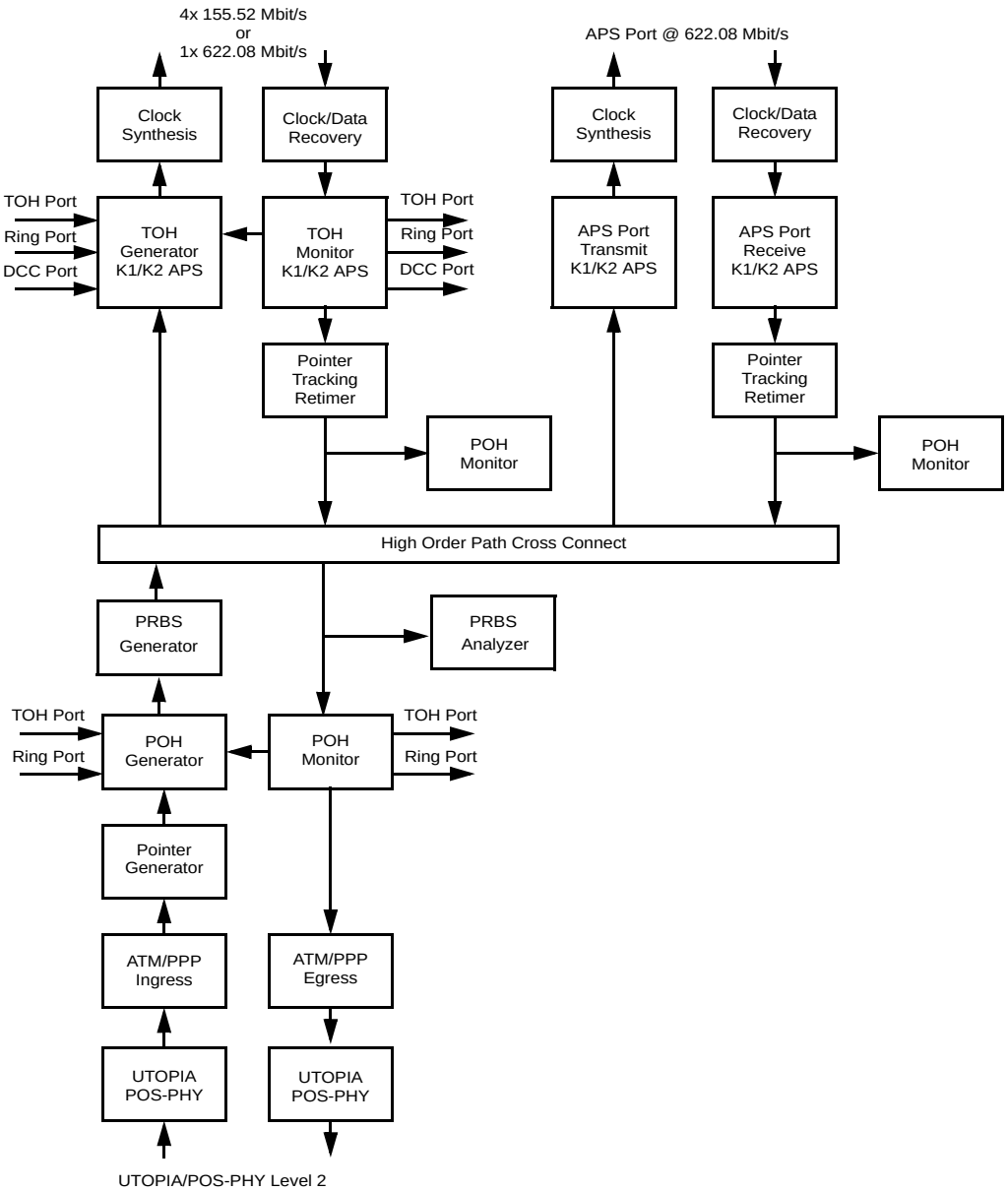
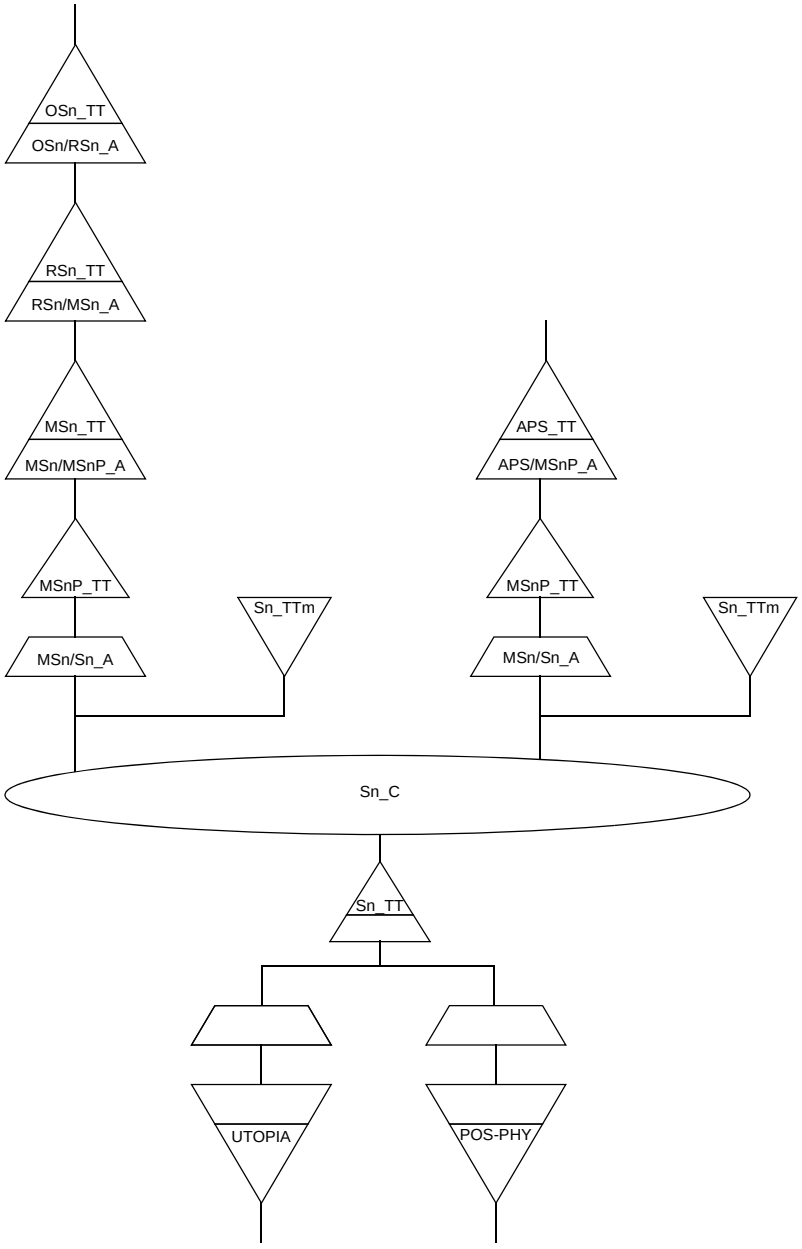


Figure 5. PHAST-12P TXC-06412B Block Diagram

1.2 FUNCTIONAL MODEL



Note: Additional information regarding Functional Diagram of the PHAST-12P can be found in ITU-T G.783 Standards Documentation.

Figure 6. PHAST-12P Functional Model

1.3 DEVICE DESCRIPTION

1.3.1 Line Side

The PHAST-12P can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line. Each incoming line signal is monitored for loss of signal and clock and data recovery is performed. Reference clocks derived from each recovered clock are available.

The subsequent TOH Monitor will terminate all RS/section and MS/line overhead bytes compliant to the latest ITU/ETSI/ANSI standards. Additionally, the received raw TOH overhead bytes are stored in on-chip memory and output on the TOH port interface for external processing (except for BIP where the error mask is calculated). The received data communication channel bytes, selectable RS/section or MS/line, are output on a DCC port interface per line interface. The K1/K2 APS signal bytes are debounced and forwarded to the APS interface. RDI and REI are output on the external and internal line ring port interfaces for ring applications.

The PHAST-12P performs high order pointer processing on the H1/H2 bytes from the receive line interfaces. The high order path containers are retimed to the local system clock.

High order POH monitoring is performed on all received high order path containers for SNC/P and UPSR applications.

In the transmit direction, the TOH Generator will insert all RS/section and MS/line overhead bytes. The TOH overhead bytes can be inserted from on-chip memory or the TOH port interface. Additionally the data communication channel bytes, selectable RS/section or MS/line, can be inserted from a DCC port interface. Remote information, RDI and REI can be inserted from the internal or external ring port interface. This selection can be made on a per line basis. The K1/K2 APS can be inserted from the APS port interface.

Finally, four individual STM-1/OC-3 lines or a single STM-4/OC-12 line are transmitted using the device's system clock.

1.3.2 APS Port Side

The serial 622.08 Mbit/s APS port interface is monitored for loss of clock and data recovery is performed. A reference clock derived from the recovered clock is available.

The received APS port signal is monitored for signal quality and the APS information exchanged between two mate PHAST-12P devices, including K1/K2 APS signal, signal fail and signal degrade status, is stored for software access.

The PHAST-12P performs high order pointer processing on the H1/H2 bytes from the receive APS port. The high order path containers are retimed to the local system clock.

High order POH monitoring is performed on all received high order path containers for SNC/P and UPSR applications.

In the transmit direction, the APS information exchanged between two mate PHAST-12P devices, including K1/K2 APS signal, signal fail and signal degrade status, is inserted either from on-chip memory or directly from the TOH monitor.

Finally the serial 622.08 Mbit/s APS port signal is transmitted using the device's system clock.

1.3.3 High Order Path Cross Connect

The non-blocking high order path cross connect block can connect each output high order path time slot to each input high order path time slot. The presence of an active cross connect does not 'block' a cross connect to another output. AIS or unequipped maintenance signals can be inserted into each output time slot.

The cross connect has three input buses and three output buses: line side, APS port side and terminal side. Each bus contains the high order path containers equivalent to an STM-4/ STS-12.

1.3.4 Terminal Side

The POH Monitor will terminate all path overhead bytes of the dropped high order path containers compliant to the latest ITU/ETSI/ANSI standards. Additionally, the received raw POH overhead bytes are stored in on-chip memory and output on the POH port interface for external processing (except for BIP where the error mask is calculated). The remote information, RDI and REI, is output on the external and internal path ring port interfaces for ring applications.

The high order path payload is subsequently demapped by the ATM/PPP egress block. The cells or packets are then output on the UTOPIA or POS-PHY interface.

In the transmit direction, ATM cells or PPP packets are input from the UTOPIA or POS-PHY interface. The ATM/PPP ingress block will map the cells or packets into the high order path payload.

The POH Generator will optionally insert all path overhead bytes. The POH overhead bytes can be inserted from on-chip memory or the POH port interface. The remote information, RDI and REI, can be inserted from the internal or external ring port interface. This selection can be made on a per high order path basis.

For Test purposes, a PRBS pattern can be generated and inserted on a particular path by the PHAST-12P. PRBS can be analyzed for bit errors on the receive side.

2.0 CONFIGURATION AND USE

2.1 MODES

2.1.1 Line Interface Mode

The PHAST-12P supports either one STM-4/OC-12 line interface, or four STM-1/OC-3 line interfaces.

In STM-4/OC-12 mode line interfaces #2 to #4 will not be used.

STM4_Mode	Description
0 (Default)	STM-1/OC-3 Mode: line interfaces #1 to #4 are 155.52 Mbit/s signals.
1	STM-4/OC-12 Mode: line interface #1 is a 622.08 Mbit/s signal, line interfaces #2 to #4 are not used.

2.1.2 SDH/SONET Mapping

The PHAST-12P supports the SDH/SONET structures presented in Figure 1. The mapping of receive and transmit line interfaces, receive and transmit APS port interfaces, and receive and transmit terminal side interfaces is independent. All mapping configurations default to all AU-4/VC-4 resp. STS-3c.

In STM-4/OC-12 mode the line interface transports a single AUG-4. A standard AUG-4 consists either of a single VC-4-4c/STS-12c or four AUG-1's. To support non-standard VC-4-2c/STS-6c SPE and VC-4-3c/STS-9c SPE contiguous concatenated containers a **TimeSlotIsConcatenated** register is provided per AUG-1 time slot.

TimeSlotIsConcatenated$_{[aug1]}$	Description
0 (Default)	The AUG-1 time slot is either not part of a contiguous concatenated container, or it is the master time slot (i.e., it carries the POH column) of a VC-4-Xc resp. STS-Nc contiguous concatenated container.
1	The AUG-1 time slot is a slave (i.e., it does not carry the POH column) of a VC-4-Xc resp. STS-Nc contiguous concatenated container.

The following table lists all valid contiguous concatenation settings:

contiguous concatenation structure				TimeSlotIsConcatenated[aug1]			
				0	**1**	**2**	**3**
AUG-1	AUG-1	AUG-1	AUG-1	0	0	0	0
AUG-1	AUG-1	VC-4-2c/STS-6c SPE		0	0	0	1
AUG-1	VC-4-2c/STS-6c SPE		AUG-1	0	0	1	0
AUG-1	VC-4-3c/STS-9c SPE			0	0	1	1
VC-4-2c/STS-6c SPE		AUG-1	AUG-1	0	1	0	0
VC-4-2c/STS-6c SPE		VC-4-2c/STS-6c SPE		0	1	0	1
VC-4-3c/STS-9c SPE			AUG-1	0	1	1	0
VC-4-4c/STS-12c SPE				0	1	1	1

Each AUG-1 time slot that is not part of a contiguous concatenated container, can independently be configured to consist of a single VC-4/STS-3c SPE or three VC-3/STS-1's SPE. A **Has_AU3** register per AUG-1 time slot determines the structure of that time slot.

Has_AU3[aug1]	Description
0 (Default)	The AUG-1 time slot consists of a single AU-4/VC-4 resp. STS-3c container.
1	The AUG-1 time slot consists of three AU-3/VC-3 resp. STS-1 containers.

In STM-1/OC-3 mode each line interface transports a single AUG-1. With the **Has_AU3** register each AUG-1 can independently be configured to consist of a single VC-4/STS-3c SPE or three VC-3/STS-1's SPE. In STM-1/OC-3 mode, it is mandatory that the **TimeSlotIsConcatenated** registers are set to the default master mode.

2.1.3 System Interface Mode

The PHAST-12P system interface operates either in UTOPIA Level 2 mode or in POS-PHY level 2 mode. The configuration of the receive and transmit system side interface is independent.

UTOPIA2	Description
0	System side interface operates in POS-PHY Level 2 mode.
1 (Default)	System side interface operates in UTOPIA Level 2 mode.

2.2 CLOCK ARCHITECTURE

The PHAST-12P's internal Transmit Clock synthesizer generates, using a selectable Tx timebase, a high-speed Transmit Clock, running at 622.08 MHz.

The System Clock, running at 77.76 MHz, is a divided-down version of this high-speed Transmit Clock.

As the PHAST-12P is a PHY-layer device, it gets both Receive and Transmit UTOPIA/POS-PHY clocks as inputs. These clocks are generated by the ATM/Link layer device. Clock boundary crossings from/to the System Clock are done in Rx and Tx Cell/Packet FIFOs.

The System Clock is available on an output lead: LINETXCLK, optionally divided down to 19.44 MHz.

The PHAST-12P's internal Clock Recovery units, operating on the four SDH/SONET Receive Line interfaces and the Receive APS Port generate five recovered clocks: one for each channel.

Internally, these units require a high-speed Receive Clock, which is synthesized using a selectable Rx timebase.

The recovered data from the four SDH/SONET Receive Lines and from the Receive APS Port is retimed to the System Clock, before entering the Cross Connect.

Divided-down versions of each recovered clock are available on output leads: LINERXCLK1 (19.44 or 77.76 MHz), LINERXCLK2 (19.44 MHz), LINERXCLK3 (19.44 MHz), LINERXCLK4 (19.44 MHz), and APSRXCLK (19.44 or 77.76 MHz).

The Tx timebase can be selected using control bits:

- Either one of the two external Transmit Clock sources: REFTXCLK1 or REFTXCLK2P/N (External Timing) (control field **TxRefSelect**, see Table 73 of the Memory Maps)
- The recovered 622.08 MHz Receive APS Port clock (External Timing) (control field: **LineTimingChannel** and **TimingMode**, see Table 73 of the Memory Maps)
- The recovered 622.08 MHz clock in STM-4/OC-12 application (Line/Loop - Timing) (control field: **LineTimingChannel** and **TimingMode**, see Table 73 of the Memory Maps)
- Any of the four recovered 155.52 MHz clocks in STM-1/OC-3 application (Line/Loop - Timing) (control field: **LineTimingChannel** and **TimingMode**, see Table 73 of the Memory Maps)

The frequency of REFTXCLOCK1 is selectable:

- 19.44 MHz
- 77.76 MHz

The frequency of REFTXCLOCK2P/N is selectable:

- 19.44 MHz
- 77.76 MHz
- 155.52 MHz
- 622.08 MHz (bypass mode)

The Rx timebase can be selected using control bits:

- Either one of the two external Tx clock sources: REFTXCLK1 or REFTXCLK2P/N (External Timing) (control field **TxRefSelect**, see Table 73 of the Memory Maps)
- The external Rx clock source: REFRXCLOCK (Line/Loop - Timing) (control field **RxRefSelect**, see Table 73 of the Memory Maps)

In case REFTXCLOCK2P/N is used as Rx timebase, the 622.08 MHz frequency (bypass mode) is not supported.

In Line/Loop - Timing mode, it is mandatory to provide an external Rx clock source at REFRXCLK. Its frequency is selectable:

- 19.44 MHz
- 77.76 MHz

Figure 7 shows the relation between synthesized/recovered clocks and the reference clocks.

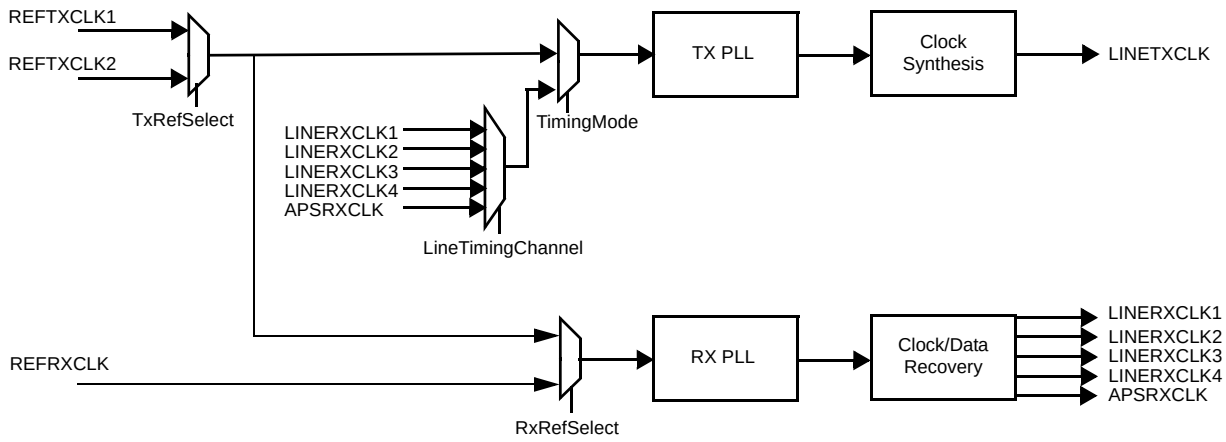
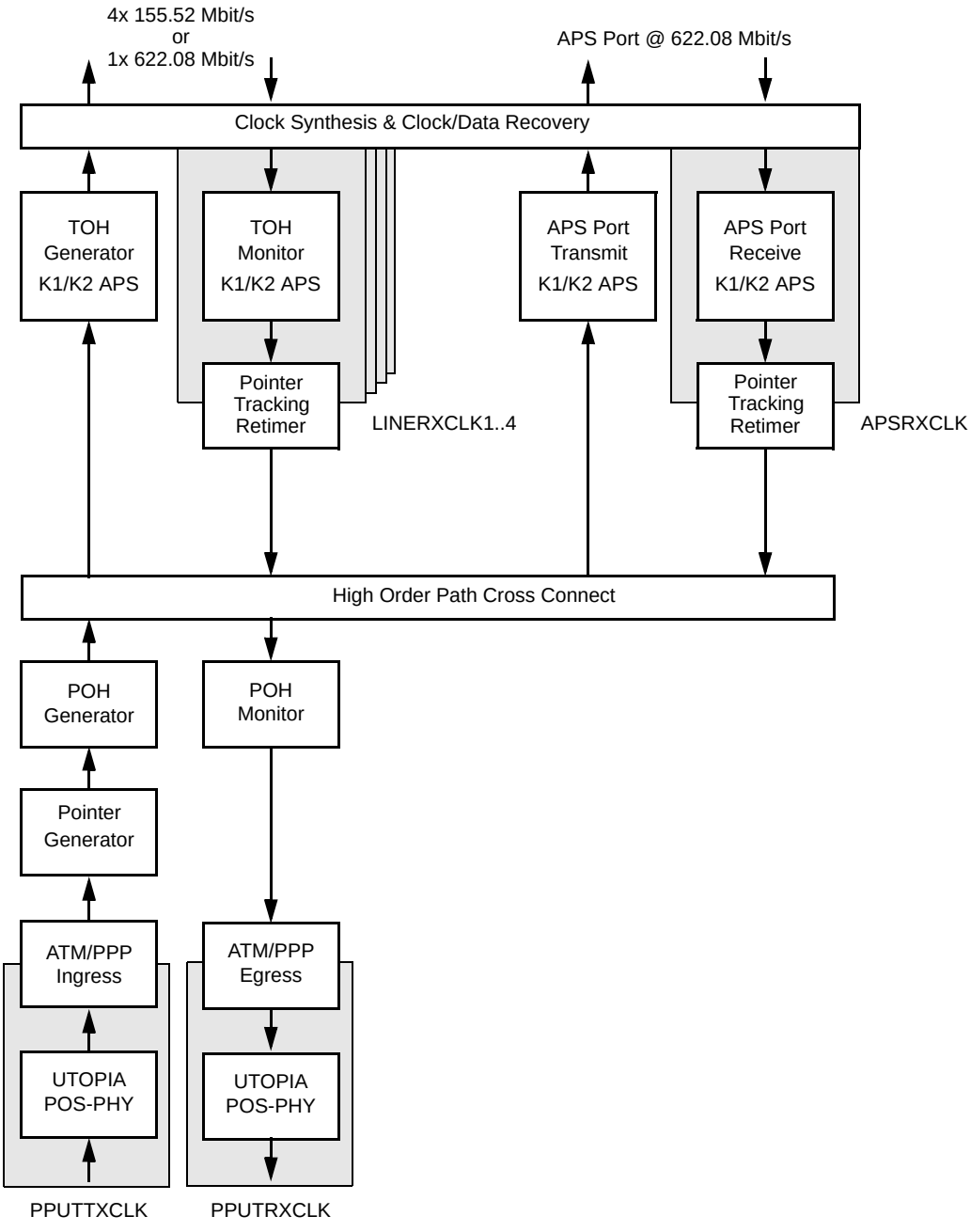


Figure 7. Clock Recovery and Clock Synthesis

2.2.1 Clocks and Software-Access



UTOPIA/POS-PHY Level 2

Following table gives an overview of the different clock domains which are necessary in order to access a particular block (see Memory Maps).

Clock Domain	Blocks
MPCLK	Global Control Reset Generator Interrupt Clock Recovery/Clock Synthesis/SerDes JTAG Master
MPCLK System Clock (=LINETXCLK)	Line Ring Port/Alarm Interface Transmit APS Port POH Generator TOH Generator TOH and DCC Port High Order Pointer Tracker and Retimer - Rx Line Interface High Order Pointer Tracker and Retimer - Rx APS Interface POS/ATM Demapper POS/ATM Mapper Pointer Generator Cross Connect High Order Path Ring Port/Alarm Interface POH Monitor - Rx Line Interface POH Monitor - Rx APS Interface POH Monitor - Terminal Side PRBS Generator/Analyzer
MPCLK System Clock (= LINETXCLK) LINERXCLK1	TOH Monitor - Rx Line 1 (STM-4 / STM-1 mode)
MPCLK System Clock (= LINETXCLK) LINERXCLK2	TOH Monitor - Rx Line 2 (STM-1 mode only)
MPCLK System Clock (= LINETXCLK) LINERXCLK3	TOH Monitor - Rx Line 3 (STM-1 mode only)
MPCLK System Clock (= LINETXCLK) LINERXCLK4	TOH Monitor - Rx Line 4 (STM-1 mode only)

Clock Domain	Blocks
MPCLK System Clock (= LINETXCLK) APSRXCLK	Receive APS Port
MPCLK System Clock (= LINETXCLK) PPUTTXCLK	Ingress UTOPIA/POS-PHY Level 2 Interface
MPCLK System Clock (= LINETXCLK) PPUTRXCLK	Egress UTOPIA/POS-PHY Level 2 Interface

2.2.2 Loss of Clock Detection

All clocks, except the microprocessor clock, are monitored for Loss of Clock. The clock to be monitored is divided by **LocDivider** + 1.

Loss of Clock is detected as follows:

- Entry: when **LOC_EntryThreshold** microprocessor clock cycles have passed without transitions on the divided clock to be monitored
- Exit: when **LOC_ExitThreshold** transitions are detected the divided clock

Note: The Loss of Clock detector can only operate correctly if the optical transceiver generates a constant output (no transitions) on the receive side when there is no valid incoming optical signal.

2.3 RESET

2.3.1 External Lead Controlled Hardware Reset

Hardware Reset (Active Low): The use of this lead at power-up is mandatory. Holding this lead low for at least 50ns causes all the registers in the device to be reset.

2.3.2 Microprocessor Controlled Hardware Reset (RESETH)

When written with the value 0x91H all registers in the device will be reset but with a few exceptions.

The registers in the following blocks will not be reset:

- Microprocessor interface
- Global control
- Reset generator
- Interrupt
- Clock recovery / clock synthesis / SerDes
- JTAG Master

These are the registers that operate in the microprocessor clock domain.

2.3.3 Microprocessor Controlled Reset Per Clockdomain

There are 6 major interfaces. For each of these there is a separate microprocessor controlled reset available. Reset is activated by writing the value 0x91 H to the corresponding register.

- RxLine1_Reset ... RxLine4_Reset: Reset in the RxLine 1 ... 4 clock domain

These software resets may only be asserted when RESETH is equal to 0x91. They may be deasserted at anytime.

2.4 POWERUP, INITIALIZATION AND STARTUP

After powerup and external reset of the device, no internal clocks are active. This section describes the way the necessary clocks need to be brought up and the initialization of the device.

The first clock present in the device is the external microprocessor clock. The registers which are needed to bring up the internal clocks are located in the clock domain from this external microprocessor clock.

The clock domains which must be brought up next are:

- System Clock
- Rx Line 1 Clock
- Rx Line 2 Clock
- Rx Line 3 Clock
- Rx Line 4 Clock
- Rx APS Clock

The Ingress and Egress UTOPIA/POS-PHY interfaces use external clocks. These clocks must be running in order to access the register in these domains.

At this stage of the process, the hardware interrupt can be enabled through the **HINTEN** field (see Table 11 of Memory Maps section). The interrupt masks must be properly disabled here.

It is advised to unmask the Global Control Interrupt now. In the Global Control block, the Loss of System Clock and Loss of Clock for the active lines must be unmasked to enable the hardware interrupt for events on the Loss of Clock detection.

After this, the Clock Recovery/Clock Synthesis block must be configured and powered up (see section Powerup of the CDR/CS).

It is recommended to leave **RESETH** (see Table 10) asserted until this point. Once **RESETH** is deasserted, the device will start a reset sequence for all of its internal RAMs. The **RamResetDone** record in the Global Control block (see Table 6) indicates which clock domains have finished resetting their RAMs.

Once all the necessary clock domains are powered up, and the corresponding RAMs are reset, the device will not yet be operational. Operation is halted so the device can be configured in a clean way. Once the configuration is done, **DeviceInitialized** field in Global Control can be set to 1 and the device will start its normal operation.

2.4.1 Powerup of the CDR/CS

A startup sequence for the Clock and Data Recovery / Clock Synthesis part of the PHAST-12P is given below (refer to the CDR/CS section of the Memory Map):

- The 1st phase requires the CDR/PLL to be set into a power down state so that it can be brought up from a known state. This is performed by doing the following accesses:

Table 1: CDR/CS Initialization Sequence, Power Down Phase

Register	Data
0x00a0	0x0091
0x0010	0x0000 or 0x0001[a]
0x3a66	0x0000
0x3a6a	0x0000
0x3a6e	0x0000
0x3a7e	0x2241
0x3a60	0x0000
0x3a62	0x0000
0x3a64	0x0000
0x3a68	0x0000
0x3a6c	0x0000
0x3a74	0x0254
0x3a76	0x0254
0x3a78	0x0254
0x3a7a	0x0254
0x3a7c	0x0254
0x3a32	0x001f
0x3a30	0x001f
0x3a34	0x0001
0x3a00	0x0000
0x3a02	0x0000
0x3a04	0x0000
0x3a06	0x0000
0x3a08	0x0000
0x3a0a	0x0000

Table 1: CDR/CS Initialization Sequence, Power Down Phase

Register	Data
0x3a0c	0x0f00
0x3a0e	0x0820
0x3a26	0x0000
0x3a5e	0x0000
0x3a48	0x0fe0
0x3a22	0x0000
0x3a24	0x0000
0x3a4c	0x0000
0x3a50	0x03ff
0x3a52	0x0000
0x3a54	0x3fff
0x3a56	0x7fff
0x3a58	0x0001
0x3a5a	0x001f
0x3a70	0x001f
0x3a72	0x001f
0x3a20	0x0001

a. Set to 0x0000 for 155.52Mbps mode or 0x0001 for 622.08Mbps mode.

- At this point poll 0x3a20 until it is set to 0x0000. This takes approximately 420 microprocessor clock cycles.
- After 0x3a20 is verified to be 0x0000, poll 0x3a40 and verify that bits 5 and 6 are both set to 0.
- The 2nd PHASE is to configure the PLL parameters as shown below:
- Configure the PLLs for External or Line Timing as follows in the order given:

Table 2: CDR/CS Initialization Sequence, Power Up Phase

Register	External Timing	Line Timing
T_PLLTune (Address 0x3a7e)	Set Tx PLL Tuning Parameters	Set TX PLL Tuning Parameters

Table 2: CDR/CS Initialization Sequence, Power Up Phase

Register	External Timing		Line Timing	
T_CDRTune (Addresses: 0x3a74, 0x3a76, 0x3a78, 0x3a7a, 0x3a7c)	Set Rx PLL Tuning Parameters		Set Rx PLL Tuning Parameters	
RxRefSelect (Address 0x3A66)	Select Rx Reference Clock		Select Rx Reference Clock	
RxRefFreq (Address 0x3A6E)	Select Rx PLL Reference Clock Frequency		Select Rx PLL Reference Clock Frequency	
TxRefSelect (Address 0x3A64)	Select Tx Reference Clock		N/A	
TxRefFreq (Address 0x3A6C)	Select Tx PLL Reference Clock Frequency		N/A	
OC3NotOC12 (Address 0x3A5A)	STM-1/OC-3 Mode	STM-4/OC-12 Mode	STM-1/OC-3 Mode	STM-4/OC-12 Mode
	0x000F	0x000E	0x000F	0x000E
LineRate (Address 0x3A52)	N/A		Select Line Rate of Reference Channel	
TimingMode (Address 0x3A60)	0x0		0x1	
LineTimingChannel (Address 0x3A62)	N/A		Select timing mode channel	
RxPLL_Cap_Enable (Address 0x3A6A)	Enable/Disable External Capacitor for Rx PLL		Enable/Disable External Capacitor for Rx PLL	
IndirectAccessMode (Address 0x3a26)	0x0000		0x0000	
IndirectAccessData (Address 0x3a5e)	0x0017		0x0017	
SerDes_LoadConfig (Address 0x3a20)	0x0001		0x0001	
Poll 0x3a20 and wait until it is 0x0000. (~420 microprocessor clock cycles)				
TxPLL_PowerDown (Address 0x3A70)	0x0008		0x0008	
RxPLL_PowerDown (Address 0x3A72)	0x0008		0x0008	

Table 2: CDR/CS Initialization Sequence, Power Up Phase

Register	External Timing	Line Timing
TxRefClock2 (Address 0x3a34)	Write 0x0001 to power down REFTXCLK2 pads if not used. Write 0x0000 to power up REFTXCLK2 pads if used.	Write 0x0001 to power down REFTXCLK2 pads if not used. Write 0x0000 to power up REFTXCLK2 pads if used.
RxPAD (Address 0x3a30)	Power up RX PADs	Power up RX PADs
RxPowerDown1 (Address 0x3a54)	0x0000	0x0000
RxPowerDown2 (Address 0x3a56)	0x0000	0x0000
TxPowerDown (Address 0x3a50)	0x0000	0x0000
ToplevelPowerDown (Address 0x3a58)	0x0000	0x0000
IndirectAccessMode (Address 0x3a26)	0x0008	0x0008
IndirectAccessData (Address 0x3a5e)	0x5000	0x5000
SerDes_LoadConfig (Address 0x3a20)	0x0001	0x0001
Poll 0x3a20 and wait until it is 0x0000. (~420 microprocessor clock cycles)		
After 0x3a20 is verified to be 0, wait an additional 5ms for the power down settings to settle.		
TxPLL_PowerDown (Address 0x3A70)	0x0000	0x0000
RxPLL_PowerDown (Address 0x3A72)	0x0000	0x0000
SerDes_LoadConfig (Address 0x3a20)	0x0001	0x0001
Poll 0x3a20 and wait until it is 0x0000. (~420 microprocessor clock cycles)		
TxPLL_Cap_Enable (Address 0x3A68)	Enable/Disable External Capacitor for Tx PLL	Enable/Disable External Capacitor for Tx PLL
SerDes_LoadConfig (Address 0x3a20)	0x0001	0x0001
Poll 0x3a20 and wait until it is 0x0000. (~420 microprocessor clock cycles)		
Poll 0x3a40 and verify that bits 5 and 6 are both set to 1. If not repeat the process starting from the power down sequence in **Table 1** above.		

Table 2: CDR/CS Initialization Sequence, Power Up Phase

Register	External Timing	Line Timing
TxPAD (Address 0x3a32)	Power up Tx Pads	Power up Tx Pads
DivideClocks (Address 0x3a4c)	Set APS and TX clock outputs to 77.76MHz or 19.44MHz	Set APS and TX clock outputs to 77.76MHz or 19.44MHz
RESETH (Address 0x00a0)	0x0000	0x0000

Note: Some CDR/CS configurations are transferred to the CDR/CS part only after a software command. Following settings will not have effect before transferring them:

CDR_CS_Setup.TxPowerDown

CDR_CS_Setup.RxPowerDown1

CDR_CS_Setup.RxPowerDown2

CDR_CS_Setup.ToplevelPowerDown

CDR_CS_Setup.OC3NotOC12

PLL_Control.TxPLL_Cap_Enable

PLL_Control.RxPLL_Cap_Enable

PLL_Control.TxPLL_PowerDown

PLL_Control.RxPLL_PowerDown

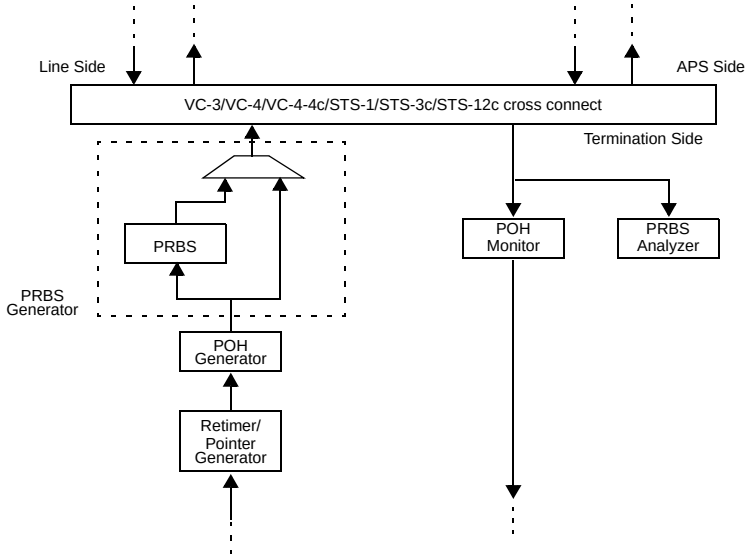
PLL_Control.CDRTune

PLL_Control.PLLTune

All configurations done via the indirect access register (IndirectAccessData and IndirectAccessMode)

After configuration of these fields, one has to set **SerDes_LoadConfig** to 0x1 in order to make these settings effective. A transfer of the above mentioned configuration records will start. **SerDes_LoadConfig** will be reset automatically by the device after the transfer is completed (approx. 420 microprocessor clockcycles). Note however settings to other addresses than those before mentioned are still possible during this transfer. The configured registers will not be reset after transfer.

2.5 PRBS GENERATOR AND PRBS ANALYZER



The PHAST-12P has a built-in PRBS generator and analyzer for test purposes. PRBS can be inserted on one path of the Terminal Side input port of the cross connect (port #3). This way PRBS can be routed through the cross connect to each of its three output ports. The PRBS analyzer is situated on the Terminal Output of the cross connect (port #3). The PRBS polynomial is $2^{23}-1$. The output of the PRBS generator and the input of the PRBS analyzer can optionally be inverted. In order to use the PRBS generator/analyzer functionality the **AUG1_Mode_Config** record in the CDR/CS block has to be configured properly. This record is a don't care if the PRBS functionality is not used. Configuration of the PRBS generator and analyzer is done in the **XConnectPRBSControl** registers.

The PRBS analyzer will lock on the incoming PRBS data after 24 consecutive correct bits. This is reported in the **Status_Unlatched** register. Once in lock the PRBS analyzer will stay in lock and count the received bit errors. These are accessible via the **PRBSBitErrorCounter**, which is reset each time a (software) read access is done to this register (clear-on-read).

The state machines are reset when disabling the PRBS generator/analyzer, so make sure to disable the PRBS generator and analyzer before (re-)configuring them.

Important Notes:

1. Although the PRBS bit error counter is mapped in the memory map of the CDR/CS block, the System clock (LINETXCLK) must be available when reading this counter.
2. B3 may contain errors as it is not recalculated on the PRBS data.
3. If the PRBS analyzer loses lock, it will not re-synch on its own; it needs to be disabled and then re-enabled in order to lock to a new pattern.

2.6 LINE INTERFACE

Four serial line interfaces with differential input/output and integrated clock recovery and synthesis are provided.

The device supports two modes: either a single STM-4/OC-12 signal, or four STM-1/OC-3 signals.

- Line Interface #1 can handle 622.08 Mbit/s or 155.52 Mbit/s data rate for STM-4/OC-12, STM-1/OC-3 applications respectively.
- Line Interfaces #2 - #4 can handle 155.520 Mbit/s data rate for STM-1/OC-3 applications.

The device's system clock is the time base for the transmit SDH/SONET line output(s).

Each individual line interface can be powered down via a memory mapped register.

Frame alignment is recovered from the A1-A2 bytes of the received signals.

The OOF anomaly and the dLOF defect will be detected according to the latest ITU/ETSI/ ANSI standards.

The following additional functions are provided:

- Four (one for each line interface) active high status inputs to monitor the external optical transceivers for low power status.
- Four (one for each line interface) output control signals under microprocessor command to control each individual external optical transceiver.
- Four (one for each line interface) reference clocks derived from the received signal. The rate of these reference clocks will be selectable per line.

AIS will be inserted per line on detection of dLOF, on detection of dLOS, optionally on the externally detected Signal Detect or under software control.

$$\begin{aligned} \textbf{aAIS} &= \textbf{not SignalDetect}_{[line]} * \textbf{not SignalDetect\_AIS\_Insert\_Disable}_{[line]} \\ &+ \textbf{dLOS}_{[line]} * \textbf{not LOS\_AIS\_Insert\_Disable}_{[line]} \\ &+ \textbf{dLOF}_{[line]} * \textbf{not LOF\_AIS\_Insert\_Disable}_{[line]} \\ &+ \textbf{Framer AIS Force}_{[line]} \end{aligned}$$

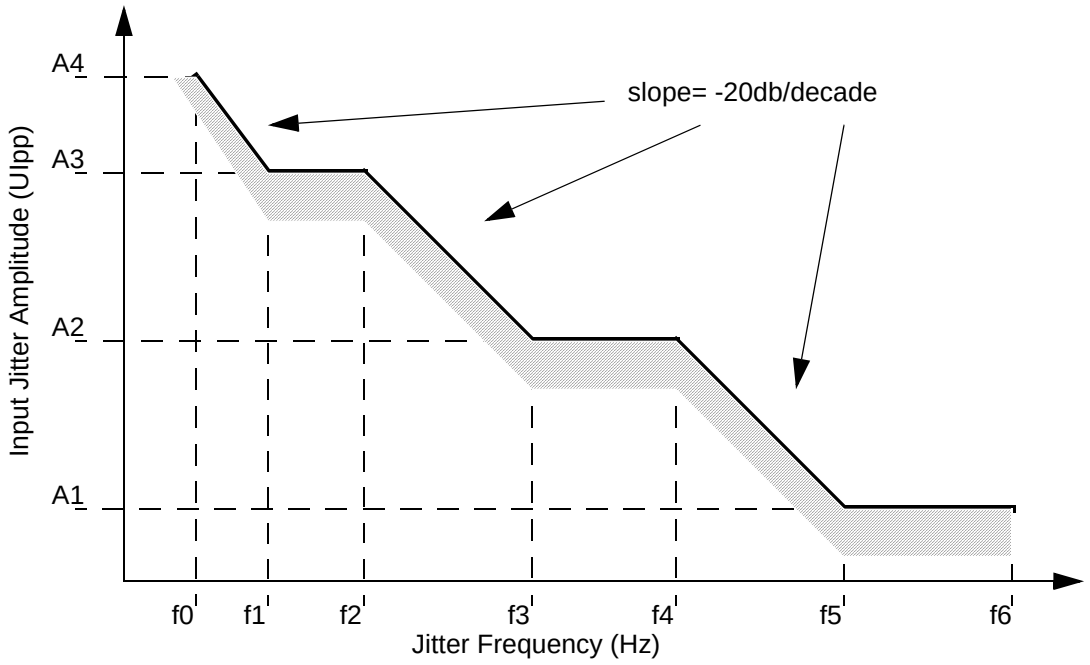
2.6.1 Jitter Generation

Below are the jitter generation figures that can be expected if a reference clock is used that meets the requirements put forth in the lead descriptions for the REFTXCLKxx leads.

Line Rate	Standard	Measurement Filter	Requirement	Actual
155.52 Mbps	ITU-T G.813 Option 1	500Hz-1.3MHz	0.50 UIpp	0.020 UIpp
		65kHz-1.3MHz	0.10 UIpp	0.020 UIpp
	ITU-T G.813 Option 2	500Hz-1.3MHz	0.50 UIpp	0.020 UIpp
		12kHz-1.3MHz	0.10 UIpp	0.020 UIpp
	GR-253	12kHz-1.3MHz	0.10 UIpp	0.020 UIpp
			0.01 UIrms	0.002 UIrms
622.08 Mbps	ITU-T G.813 Option 1	1000Hz-5MHz	0.50 UIpp	0.085 UIpp
		250kHz-5MHz	0.10 UIpp	0.070 UIpp
	ITU-T G.813 Option 2	1000Hz-5MHz	0.50 UIpp	0.085 UIpp
		12kHz-5MHz	0.10 UIpp	0.080 UIpp
	GR-253	12kHz-5MHz	0.10 UIpp	0.080 UIpp
			0.01 UIrms	0.004 UIrms

2.6.2 Jitter Tolerance

The PHAST-12 device exceeds the GR-253 jitter tolerance masks for both 622Mbps and 155Mbps rates as shown below.

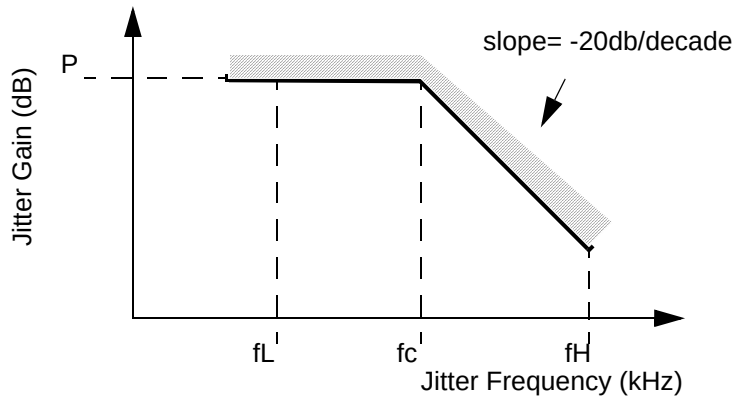


Rate (Mbps)	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (Hz)	f4 (kHz)	f5 (kHz)	f6 (MHz)	A4 (UIpp)	A3 (UIpp)	A2 (UIpp)	A1 (UIpp)
155	10	NA	68.7	500	6.5	65	1.3	NA	10.9	1.5	0.15
622	10	18.5	100	1000	25	250	5.0	27.8	15	1.5	0.15

Figure 8. Jitter Tolerance

2.6.3 Jitter Transfer

The PHAST-12 device meets the jitter transfer requirements below in Line/Loop Timing mode.



Rate (Mbps)	fL (kHz)	fc (kHz)	fH (MHz)	P (dB)
155	1.3	130	1.3	0.1
622	15	500	5	0.1

Figure 9. Jitter Transfer

2.7 APS INTERFACE

The APS Port transports the payload and APS signaling between two mate devices. The APS finite state machine itself needs to be implemented by the external host software. The resulting bridge and switch requests are performed by configuring the cross connect.

A single 622.08 Mbit/s LVDS serial APS interface with differential input/output is provided. Clock recovery and synthesis are integrated.

The device's system clock is the time base for the transmit APS interface output.

The APS port interface can be powered down via a memory mapped register.

The APS Interface characteristic information consists of:

- A1, A2, J0, and B1 overhead bytes similar to the STM-4/OC-12 RS (section) overhead
- The high order path data for four STM-1/OC-3 signals or one STM-4/OC-12 signal
- The received and transmitted K1/K2 APS signal for up to four lines
- Signal fail and signal degrade indications for up to four lines

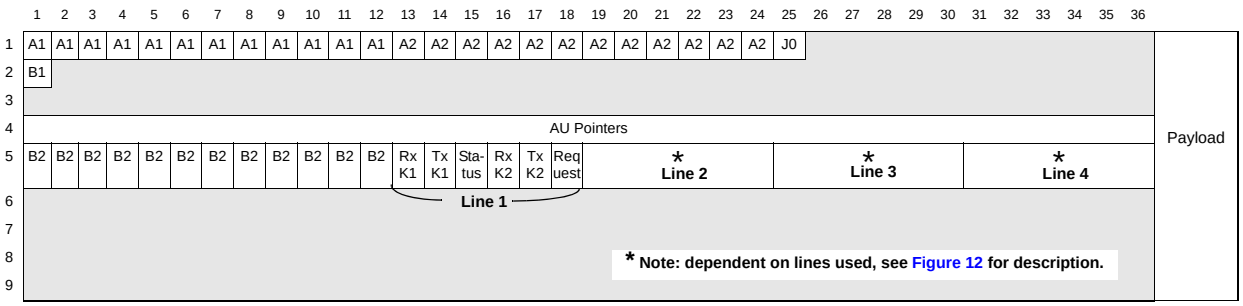


Figure 10. APS Overhead

2.7.1 APS Interface Generator

The PHAST-12P generates the APS interface overhead bytes.

- The SDH/SONET frame alignment signal will be inserted in the A1-A2 bytes
- The signal will be scrambled, except for the first SOH row
  - Software will be able to disable scrambling for test purposes
- A single byte Trail Trace Identifier (TTI) will be inserted in the J0 byte
- A fixed value (0xCC) will be inserted in the Z0 bytes. Remark the inserted value is different from 0x00 to avoid LOS detection.
- BIP-8 will be calculated over all bits of the preceding STM-4 like APS frame after scrambling and will be inserted in the B1 byte of the current frame before scrambling
- BIP-96 will be calculated over all bits of the preceding STM-4 frame except the first three SOH rows and will be inserted in the B2 bytes of the current frame. The software configurable B2 bytes have a special behavior, in that the filled in bytes are used as an error-mask to corrupt the calculated B2 bytes.
- Rx K1, Tx K1, Rx K2, Tx K2, Status and Request are inserted according to the APS protocol
- AU Pointer bytes are passed
- Unused bytes are set to 0x00

2.7.2 APS Interface Monitor

The PHAST-12P terminates the APS interface overhead bytes.

- Loss of Lock (LOL) of the on-chip clock and data recovery will be reported
- Frame alignment is recovered from the A1-A2 bytes of the received signals
- Errors in the frame alignment signal will be detected and reported as OOF
- The signal will be descrambled, except for the first SOH row
  - Software will be able to disable descrambling for test purposes

- The single byte Trail Trace Identifier (TTI) in the J0 byte will be compared to an expected value and the TTI Mismatch defect (TIM) will be detected
- The accepted Trail Trace Identifier will be reported
- The Z0 bytes are ignored
- BIP-8 will be calculated over all bits of the preceding STM-4 like APS frame before descrambling and will be compared to the B1 byte of the current frame after descrambling
- B1 BIP-8 errored blocks will be counted in a one second performance counter
- 3 subsequent frames with B1 BIP-8 errored blocks will be reported as a degraded signal (**B1_Error**) alarm, 5 subsequent non-errored frames will clear the **B1_Error** alarm. Remark the B1 BIP-8 errored blocks continues to count the errored frames on incoming SSF. As a consequence B1_Error will also be declared. Note:
  - B1_Error is not a standard SONET/SDH defect. No consequent actions are defined for it.
  - APS is a dedicated interface and the only reason for incoming SSF is Loss Of Frame (which indicates there is something wrong in the APS connection).
  - In the Line RSOH monitor the B1 counter is frozen on incoming SSF.
- B2 bytes are ignored.
- Rx K1, Tx K1, Rx K2, Tx K2, Status and Request are monitored according to the APS protocol
- All other (unused) bytes are ignored.

2.8 REGENERATOR SECTION (SECTION) OVERHEAD PROCESSING

The PHAST-12P device complies to the latest ITU/ETSI/ANSI standards and features regarding the generation and monitoring of the Regenerator Section Overhead bytes.

2.8.1 Regenerator Section Overhead Generator

The PHAST-12P generates the Regenerator Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- The frame alignment signal will be inserted in the A1-A2 bytes
- The signal will be scrambled, except for the first SOH row
  - Software will be able to disable scrambling for test purposes
- A single or 16 byte Trail Trace Identifier will be inserted in the J0 byte
- The interleave depth coordinate can be inserted in the Z0 bytes for backwards compatibility. Note the Z0 bytes need to be carefully chosen in order to guarantee enough transitions on the first TOH row.
- BIP-8 will be calculated over all bits of the preceding STM-n frame after scrambling and will be inserted in the B1 byte of the current frame before scrambling. The software configurable B1 byte has a special behavior, in that the filled in byte is used as an error-mask to corrupt the calculated B1 byte
- The D1-D3 bytes will optionally be inserted from
  - The transmit DCC interface, if the latter is configured for RS DCC
  - The TOH byte interface
  - The transmit TOH RAM
- The E1, F1, user bytes and MDB bytes will optionally be inserted from
  - The transmit TOH byte interface
  - The transmit TOH RAM

2.8.2 Regenerator Section Overhead Monitor

The PHAST-12P terminates the Regenerator Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- The signal will be descrambled, except for the first SOH row
  - Software will be able to disable descrambling for test purposes
- The single or 16 byte Trail Trace Identifier in the J0 byte will be compared to an expected value and the dTIM defect will be detected
  - Software will be able to disable the TTI mismatch process
  - AIS insertion upon dTIM detection will be configurable
- The accepted Trail Trace Identifier will be reported
- BIP-8 will be calculated over all bits of the preceding STM-n frame before descrambling and will be compared to the B1 byte of the current frame after descrambling. The software readable B1 byte has a special behavior, in that the transmitted byte represents the error mask (difference between calculated and received byte).
- The D1-D3 bytes will be forwarded to the receive DCC interface, if the latter is configured for RS DCC
- The D1-D3, E1, user bytes and MDB bytes will be written to the receive TOH RAM

- The D1-D3, E1, user bytes and MDB bytes will be forwarded to the receive TOH byte interface
- Near End Defect Second: Occurrence of aTSF will result in a Near End Defect Second. This register is cleared on the one-second boundary, after it has been copied to its shadow register (software readable).

The PHAST-12P RSOH Monitor will insert AIS per line interface towards the MSOH Monitor according to the following expression:

$$aAIS_{[line]} = dTIM_{[line]} * \text{not } TIM\_AIS\_Insert\_Disable_{[line]} + RSOH\_AIS\_Force_{[line]}$$

2.9 MULTIPLEX SECTION (LINE) OVERHEAD PROCESSING

The PHAST-12P device is compliant to the latest ITU/ETSI/ANSI standards and features regarding the generation and monitoring of the Multiplex Section Overhead bytes.

2.9.1 Multiplex Section Overhead Generator

The PHAST-12P generates the Multiplex Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- BIP-nx24 will be calculated over all bits of the preceding STM-n frame except the first three SOH rows and will be inserted in the B2 bytes of the current frame. The software configurable B2 bytes have a special behavior, in that the filled in bytes are used as an error-mask to corrupt the calculated B2 bytes.
- Per line the internal or the external ring port can be selected as source for the REI and RDI indications
- The REI will be inserted into the M1 byte
- The RDI will be inserted into the K2 byte
- The MSP APS signal will be inserted into the K1-K2 bytes from
  - The receive APS Port
  - The transmit receive TOH RAM
- The D4-D12 bytes will optionally be inserted from
  - The transmit DCC interface, if the latter is configured for MS DCC
  - The transmit TOH byte interface
  - The transmit TOH RAM
- The E2 byte will optionally be inserted from
  - The transmit TOH byte interface
  - The transmit TOH RAM
- The synchronization status message will be inserted into the S1 byte. The sources are
  - The transmit TOH byte interface
  - The transmit TOH RAM

2.9.2 Multiplex Section Overhead Monitor

The PHAST-12P terminates the Multiplex Section overhead bytes of one STM-4/OC-12 or four STM-1/OC-3 signals.

- BIP-nx24 will be calculated over all bits of the preceding STM-n frame except the first three SOH rows and will be compared to the B2 bytes of the current frame
  - An errored near-end block nN_B will be counted for performance monitoring if one or more errors in a STM-n frame are detected by the BIP-nx24. Optionally bit errors will be counted. The software readable B2 bytes have a special behavior, in that the transmitted bytes represent the error mask (difference between calculated and received bytes).
  - The error count per frame will be forwarded to the internal and external line ring ports as REI indication for the mate TOH generator
  - The dDEG and dEXC defects will be detected for both bursty and Poisson error distributions based on (block) error thresholds
- The errored far-end blocks will be counted for performance monitoring based on the REI value retrieved from the M1 byte. Optionally bit errors will be counted
- The dAIS and dRDI defects will be detected
- The MSP APS signal will be retrieved from the K1-K2 bytes and
  - Written to the receive TOH RAM
  - Forwarded to the receive TOH byte interface
  - Forwarded to the transmit APS Port
- The D4-D12 bytes will be forwarded to the receive DCC interface, if the latter is configured for MS DCC
- The D4-D12, E2 and S1 bytes will be written to the receive TOH RAM
- The D4-D12, E2 and S1 bytes will be forwarded to the receive TOH byte interface
- The synchronization status message accepted from the S1 byte will be reported
- The S1 byte will be monitored for changes in the accepted synchronization status message
- Far End Defect Second: Occurrence of dRDI will result in a Far End Defect Second. This register is cleared on the one-second boundary, after it has been copied to its shadow register (software readable).

Per line AIS will be inserted on detection of dAIS or dEXC on that line or under software control.

Per line RDI will be forwarded to the internal and external line ring ports for the mate TOH generator.

The signal degrade (dDEG) and signal fail indications will be forwarded to the transmit APS port.

The PHAST-12P MSOH Monitor will insert AIS per line interface towards the pointer tracker according to the following expression:

$$aAIS_{[line]} = dAIS_{[line]} * \text{not AIS\_AIS\_Insert\_Disable}_{[line]} + dEXC_{[line]} * \text{not EXC\_AIS\_Insert\_Disable}_{[line]}$$

$$+ \quad dSSF_{[line]} * \text{not } SSF\_AIS\_Insert\_Disable_{[line]}$$
$$+ \quad MSOH\_AIS\_Force_{[line]}$$

The PHAST-12P MSOH Monitor will insert RDI per line interface towards the RX Line Ring Port according to the following expression:

$$aRDI_{[line]} = dAIS_{[line]} * \text{not } AIS\_RDI\_Insert\_Disable_{[line]}$$
$$+ \quad dEXC_{[line]} * \text{not } EXC\_RDI\_Insert\_Disable_{[line]}$$
$$+ \quad dSSF_{[line]} * \text{not } SSF\_RDI\_Insert\_Disable_{[line]}$$
$$+ \quad MSOH\_AIS\_Force_{[line]}$$

2.10 HIGH ORDER CROSS CONNECT

The PHAST-12P provides a high order SDH/SONET path cross connect function. Each VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE path at the cross connect outputs will be able to serve as connection destination point. Each VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE path at the cross connect inputs will be able to serve as connection source point.

The cross connect function will support uni-directional connections between source points at any of its inputs to destination points at any of its outputs.

The cross connect function will support multicasting of a single source point to any number of destination points.

The cross connect function will source the appropriate unequipped signal at not connected destination points.

At power up or reset, the cross connect will default all destination points to not connected.

The cross connect will be able to squelch or insert AIS at each destination point.

The cross connect function will be non-blocking.

For each output time slot the following parameters will be configurable by the user:

- The connection source point (input bus and time slot)
- Concatenation indication according to the SDH/SONET mapping mode
- Forced unequipped signal insertion (if no connection active)

$Force\_Uneq_{[bus][ts]}$	Description
0	Output time slot [ts] on bus [bus] is connected to the SourceBus/SourceTs channel.
1 (Default)	Output time slot [ts] on bus [bus] is forced to unequipped.

- Forced AIS insertion (for APS squelching)

Force_AIS$_{[bus][ts]}$	Description
0 (Default)	Output time slot [ts] on bus [bus] is connected to the SourceBus/SourceTs channel.
1	Output time slot [ts] on bus [bus] is forced to AIS.

The PHAST-12P high order cross connect function will support three input buses and three output buses.

- Line interface
- APS Port
- POH Termination

Each bus will transport synchronous payload containers equivalent to a STM-4/OC-12 rate, i.e., up to 12 AU-3/VC-3/STS-1's, up to four VC-4/STS-3c's SPE, up to two STS-6c's, one STS-9c, one VC-4-4c/STS-12c SPE, or combinations thereof.

2.11 AUTOMATIC PROTECTION SWITCHING

2.11.1 Single Device Operation

The PHAST-12P device will support two 1+1, two 1:1 or one 1:n (n=2-3) protection groups within a single PHAST-12P device in STM-1/OC-3 mode. The incoming K1/K2 APS will be monitored by the TOH Monitor block. The outgoing K1/K2 APS will be generated by the TOH Generator block. The high order path cross connect will support bridge and switch operation. Figure 11 shows a 1:3 APS in idle state and in bridge/switch state after a failure of working line #2.

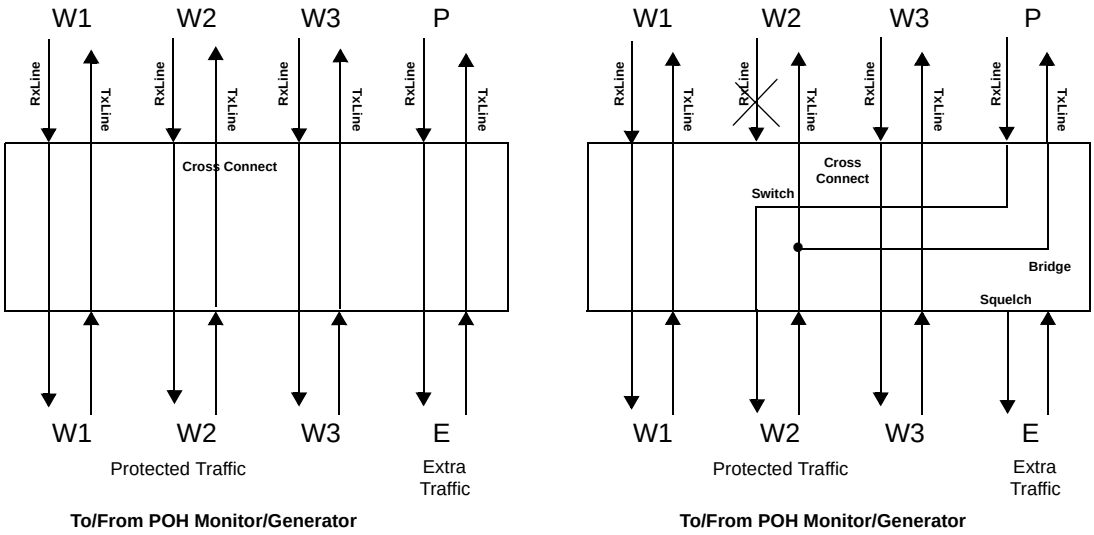


Figure 11. STM-1/OC-3, 1:3 APS with One PHAST-12P

2.11.2 Dual Device Operation

When two PHAST-12P devices are connected through the APS Port Interface, the following protection schemes are supported:

- 1+1, 1:1 or 1:n (n<=7) in STM-1/OC-3 mode,
- 1+1 or 1:1 in STM-4/OC-12 mode.

The APS Port interface will transport payload data and the APS finite state machine (FSM - implemented by external host software) indications between the two participating PHAST-12P devices. The interface consists of two point-to-point interfaces: one will transport payload data and FSM indications from the worker lines to the protection line, the other will transport payload data and FSM indications from the protection line to the worker lines.

The FSM indications include:

- RxAPS: the K1/K2 APS code received from the receive line interface,
- TxAPS: the K1/K2 APS code which needs to be sent on the transmit line interface,
- Status: the status of the received line, including the signal failure and signal degrade conditions,
- Request: actions requested by the finite state machine implemented by external host software, including switch and bridge requests.

The high order path cross connect will support bridge and switch operation.

2.11.3 APS Port Architecture

Figure 12 shows the Receive and Transmit APS Port interface in relation to the Receive and Transmit Line interface and high order cross connect function.

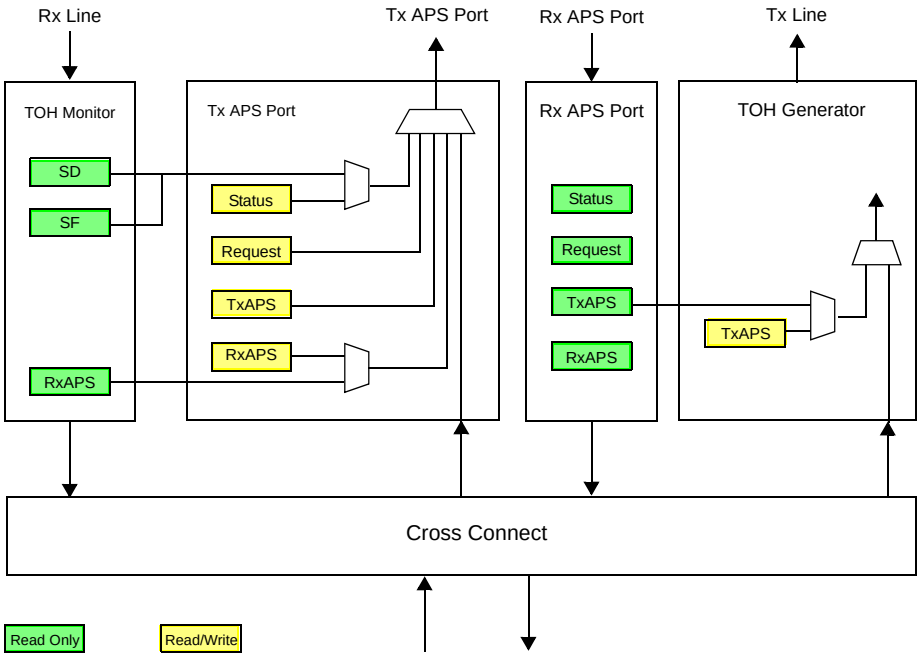


Figure 12. APS Port Architecture

The Tx APS Port interface sends the synchronous payload data from this PHAST-12P to its mate PHAST-12P.

It also allows the in-band forwarding of RxAPS, TxAPS, Status and Request:

- RxAPS: forwarded from the receive line interface, or optionally under software control
- TxAPS: under software (APS finite state machine) control
- Status: forwarded from the receive line interface, or optionally under software control
- Request: under software (APS finite state machine) control

The Rx APS Port interface receives the synchronous payload data from the mate PHAST-12P. It will also monitor the in-band forwarded of RxAPS, TxAPS, Status and Request indications. The TxAPS will be forwarded to the TOH Generator. The latter will have an option to insert the transmitted K1/K2 APS autonomously from the TxAPS on the Rx APS Port or from software controlled registers.

The functionality of the APS Interfaces described in “APS Interface” on page 44, the presence of the AU Pointer Tracker and the STM-4 like APS frame makes the APS port can be used as a STM-4 SONET Lite Port. Important limitation to know about this: the incoming B2 bytes are

NOT processed by the APS Monitor. Remark also the APS port has LVDS I/Os while the Line Ports has LVPECL I/Os

2.11.4 Example: STM-4/OC-12 Mode, 1+1 APS Protection

Figure 13 shows an example of a 1+1 APS protection architecture in STM-4/OC-12 mode. One PHAST-12P device handles the Worker line (W) while a second PHAST-12P handles the Protection line (P). Both devices are interconnected through the full bandwidth of APS Port interface. The cross connects of both devices setup a permanent bridge from the Worker Transmit line to the Protection Transmit line over one of the APS Port interfaces. The received protection payload is available on the other APS Port interface.

When the APS FSM detects a failure of the Worker line the cross connect of the Worker PHAST-12P performs the protection switch. It connects the receive protected traffic to the Receive APS Port interface which transports the payload of the received Protection line.

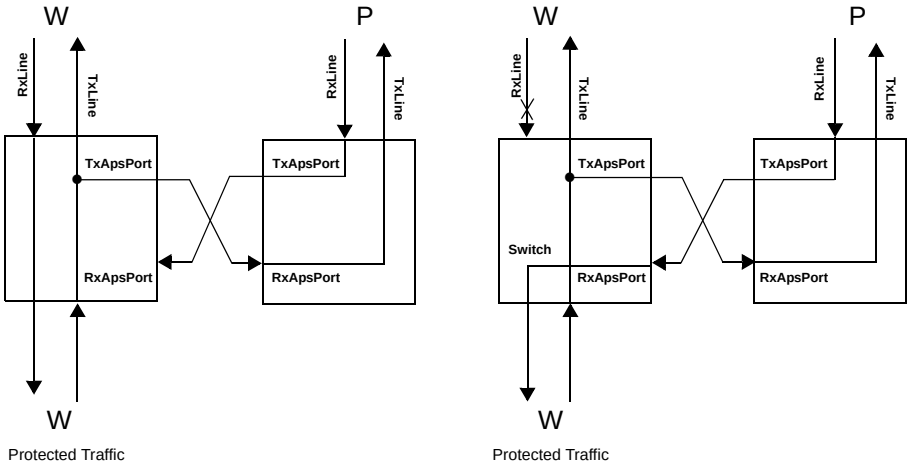


Figure 13. STM-4/OC-12, 1+1 APS

2.11.5 Example: STM-4/OC-12 Mode, 1:1 APS Protection

Figure 14 shows an example of a 1:1 APS protection architecture in STM-4/OC-12 mode. The setup is similar to the 1+1 case without the permanent bridge. This allows unprotected extra traffic to be transported over the Protection line while there is no protection request active.

When the APS FSM detects a failure of the Worker line the cross connect of the Protection PHAST-12P performs a protection bridge connecting the transmit protected traffic to the transmit Protection line. The Worker PHAST-12P performs the protection switch. It connects the protected traffic to the Receive APS Port interface which transports the payload of the received Protection line. The unprotected extra traffic is no longer available and will be squelched.

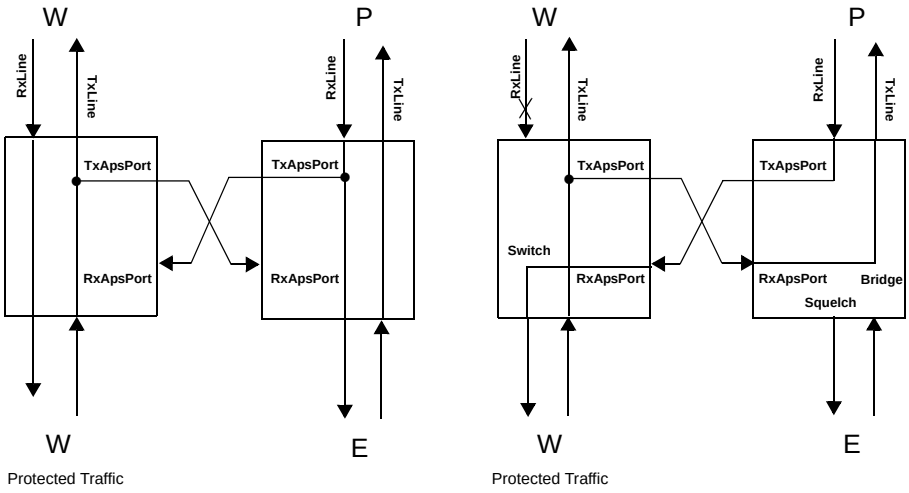


Figure 14. STM-4/OC-12, 1:1 APS

2.11.6 Example: STM-1 Mode, 1+1 APS Protection

Figure 15 shows an example of a 1+1 APS protection architecture in STM-1/OC-3 mode using two PHAST-12P devices. One PHAST-12P device handles up to four Worker lines (W) while a second PHAST-12P handles the associated Protection lines (P). Both devices are interconnected through the APS Port interface, using one fourth of the bandwidth per STM-1/OC-3 protection group. The cross connects of both devices setup permanent bridges from the Worker Transmit lines to their Protection Transmit lines over one of the APS Port interfaces. The received protection payload of the four lines is available on the other APS Port interface.

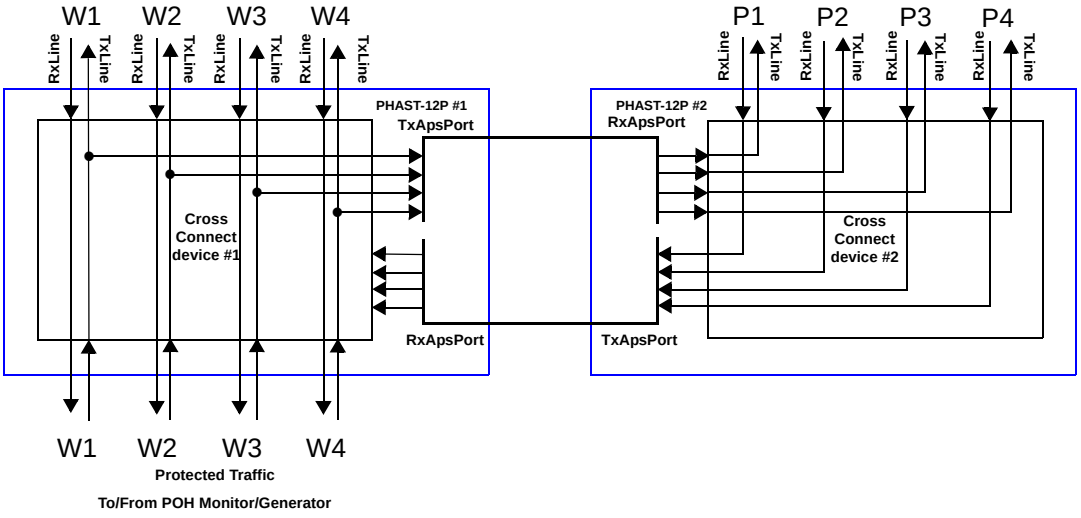


Figure 15. STM-1/OC-3, 1+1 APS Idle State

When the APS FSM detects a failure of one of the Worker lines, e.g., line #2 in Figure 16, the cross connect of the Worker PHAST-12P performs the protection switch. It connects the receive protected traffic of the failed line to the payload of its associated received Protection line available at the Receive APS Port interface.

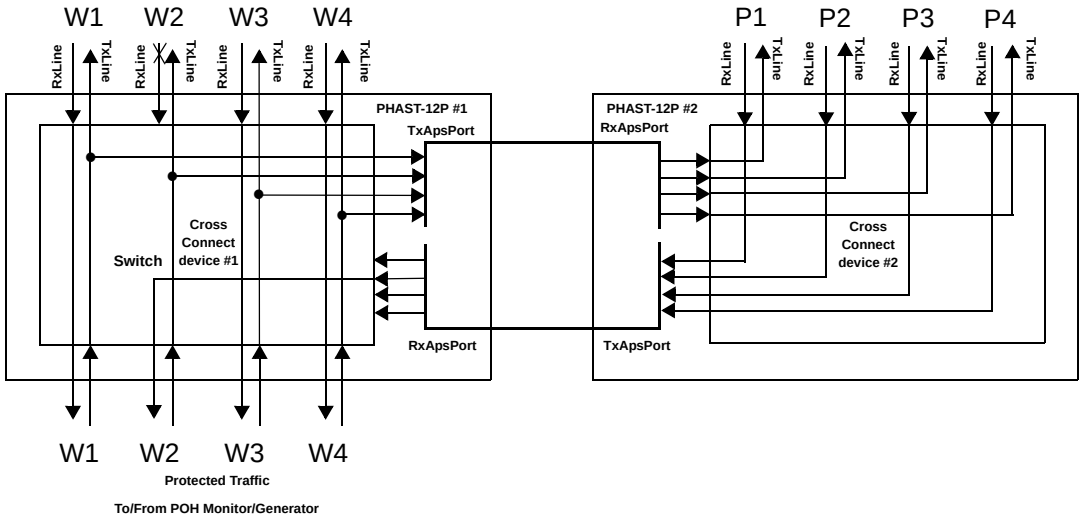


Figure 16. STM-1/OC-3, 1+1 APS Switch State

2.11.7 Example: STM-1 Mode, 1:1 APS Protection

Figure 17 shows an example of a 1:1 APS protection architecture in STM-1/OC-3 mode using two PHAST-12P devices. The setup is similar to the 1+1 case without the permanent bridge. This allows unprotected extra traffic to be transported over a Protection line while there is no protection request active at that line.

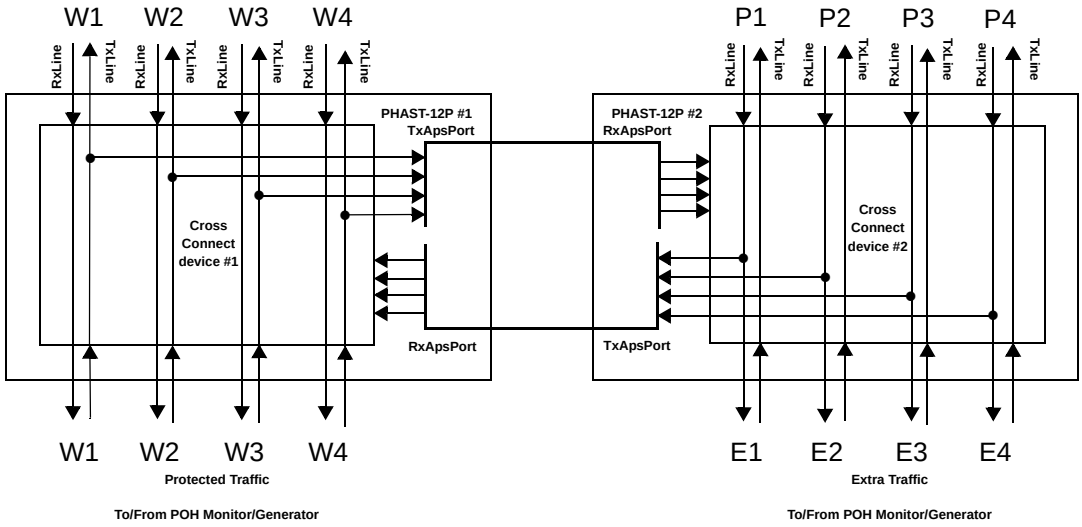


Figure 17. STM-1/OC-3, 1:1 APS Idle State

When the APS FSM detects a failure of one of the Worker lines, e.g., line #2 in Figure 18, the cross connect of the Protection PHAST-12P performs a protection bridge connecting the transmit protected traffic of the failed line to the transmit Protection line. The Worker PHAST-12P performs the protection switch. It connects the protected traffic of the failed line to the payload of its associated received Protection line available at the Receive APS Port interface. The unprotected extra traffic of that Protection line is no longer available and will be squelched.

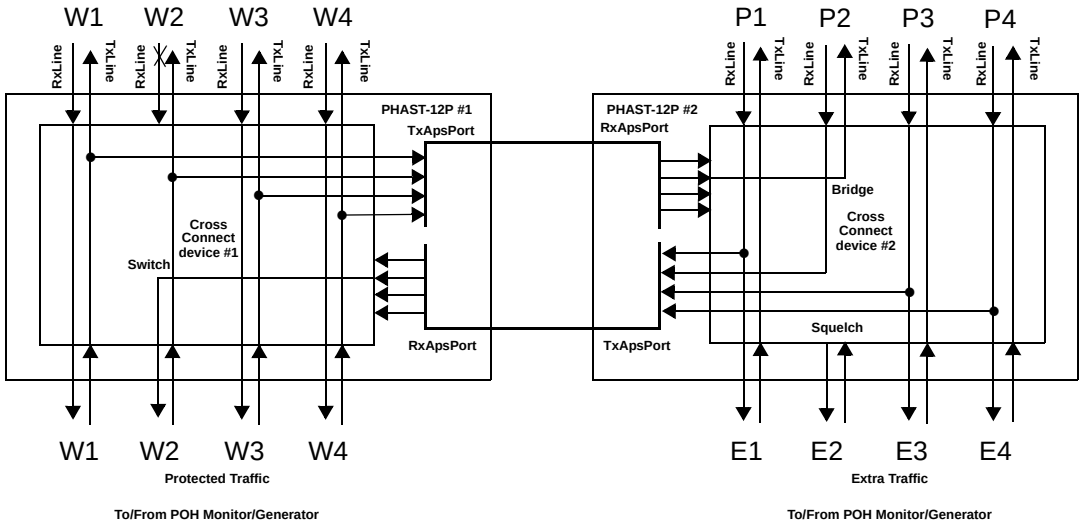


Figure 18. STM-1/OC-3, 1:1 APS Switch State

2.11.8 Example: STM-1 Mode, 1:n APS Protection

Figure 19 shows an example of a 1:n (n=7) APS protection architecture in STM-1/OC-3 mode using two PHAST-12P devices.

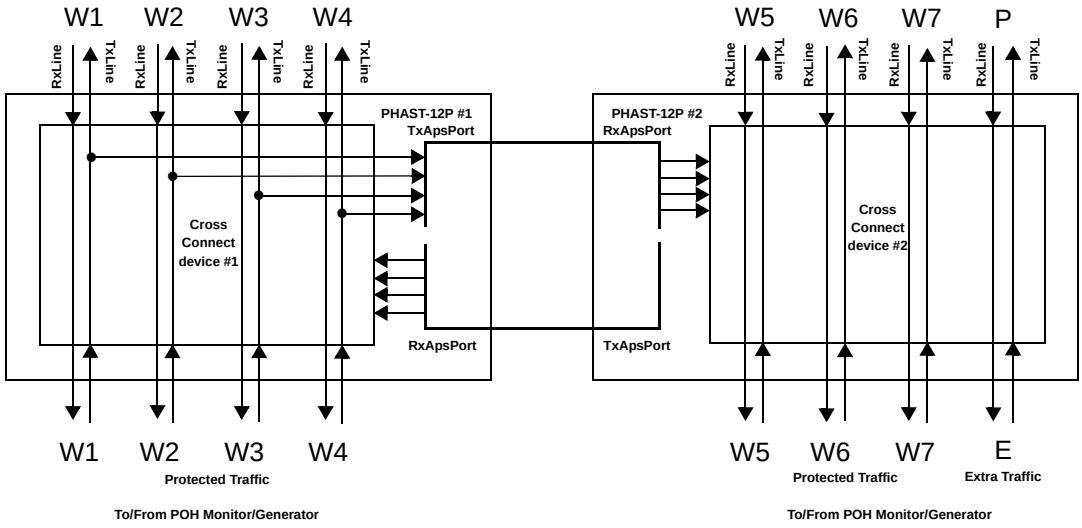


Figure 19. STM-1/OC-3, 1:7 APS Idle State

When the APS FSM detects a failure of one of the Worker lines, e.g., line #2 in Figure 20, the cross connect of PHAST-12P #2 performs a protection bridge connecting the transmit protected traffic of the failed line to the transmit Protection line. PHAST-12P #1 performs the protection switch. It connects the protected traffic of the failed line to the payload of its associated received Protection line available at the Receive APS Port interface. The unprotected extra traffic of that Protection line is no longer available and will be squelched.

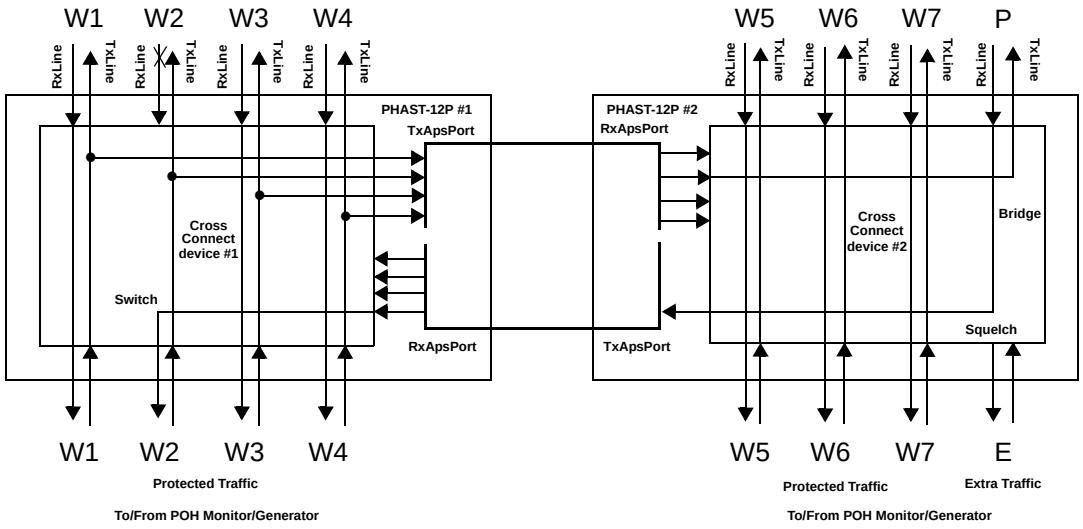


Figure 20. STM-1/OC-3, 1:7 APS Switch State

In case the failed line is terminated in PHAST-12P #2 itself, the cross connect of that PHAST-12P #2 will perform the protection switch without use of the APS port.

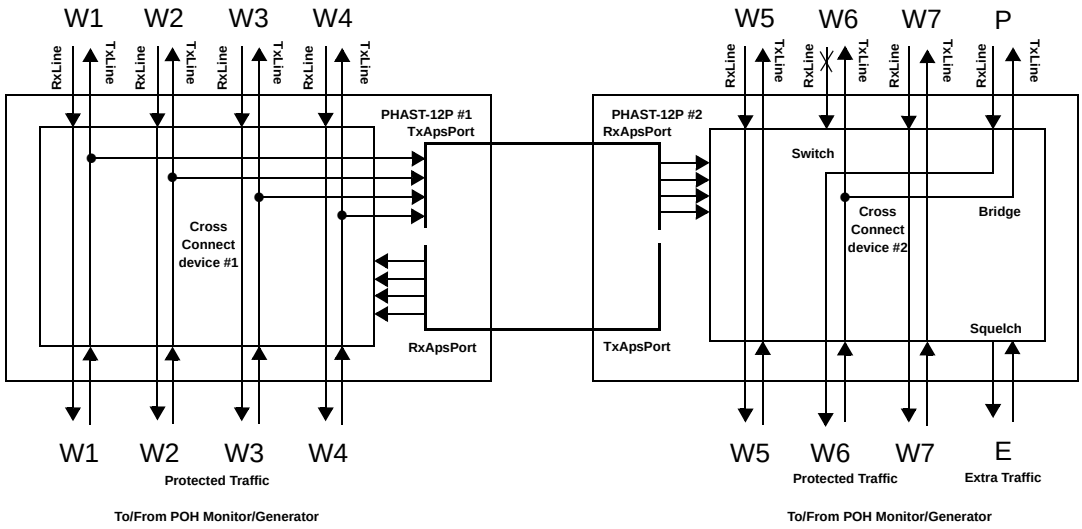


Figure 21. STM-1/OC-3, 1:7 APS Switch State

2.12 HIGH ORDER POINTER TRACKING, RETIMING AND POINTER GENERATION

2.13 LINE AND APS SIDE POINTER TRACKING, RETIMING AND POINTER GENERATION

The PHAST-12P will perform high order pointer processing and retiming on the H1/H2 pointer bytes from the received lines and from the APS Port.

The pointer tracking process will be performed according to the generic requirements for a SDH/SONET pointer tracker based on ETSI/ITU-T/ANSI standards.

The retiming process will retime the incoming STM-4/OC-12 or 4*STM-3/4*OC-3 lines and the received APS signal to the system clock.

The path AIS (dAIS), loss of pointer (dLOP) and FifoError defect will be detected per high order path.

The PHAST-12P pointer tracker and retimer will insert AIS per high order path towards the high order cross connect according to the following expression:

$$\begin{aligned} aAIS_{[path]} &= dAIS_{[path]} * \text{not AU\_AIS\_AIS\_Insert\_Disable} \\ &+ dLOP_{[path]} * \text{not LOP\_AIS\_Insert\_Disable} \\ &+ dTSF_{[path]} * \text{not TSF\_AIS\_Insert\_Disable} \\ &+ FifoError_{[path]} * \text{not FifoError\_AIS\_Insert\_Disable} \\ &+ AIS\_Force_{[path]} \end{aligned}$$

Incoming and outgoing pointer increments and decrements will be counted for performance monitoring.

Received SS bits are reported by the pointer tracking process. SS bits to be generated by the retiming process are configurable.

2.14 DETECTION OF CONCATENATED STRUCTURES

The incoming pointer bytes are analyzed for concatenation indicators (Y1*). A Concatenation configuration is set up and locked after four identical configurations. A (latched) indication is given to software when a new configuration has been detected and the entire detected configuration is reported by 12 bits. A ‘1’ means a concatenation indication (Y1*) has been detected on the pointer bytes of the corresponding timeslot.

Important note: This concatenation detector only detects the concatenation indicators of the incoming pointer bytes. The detected configuration only serves as status, reported to software and is never used to configure the pointer tracking process.

2.15 TERMINAL SIDE POINTER GENERATION

Sourced VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE channels will have a AU-3/AU-4/AU-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c pointer value fixed to 0 or 522. This value has to be configured in the Terminal Pointer Generator.

SS bits are configurable.

2.16 FRAME REFERENCE PULSES

A Frame Reference Pulse is necessary wherever timing has to be (re)generated in the PHAST-12P. The PHAST-12P can lock on an externally provided Frame Reference Pulse, making it possible to align with other devices, or generate the Frame Reference Pulse internally.

The (generated) System Frame Reference Pulse is available via the REFSYSFS lead.

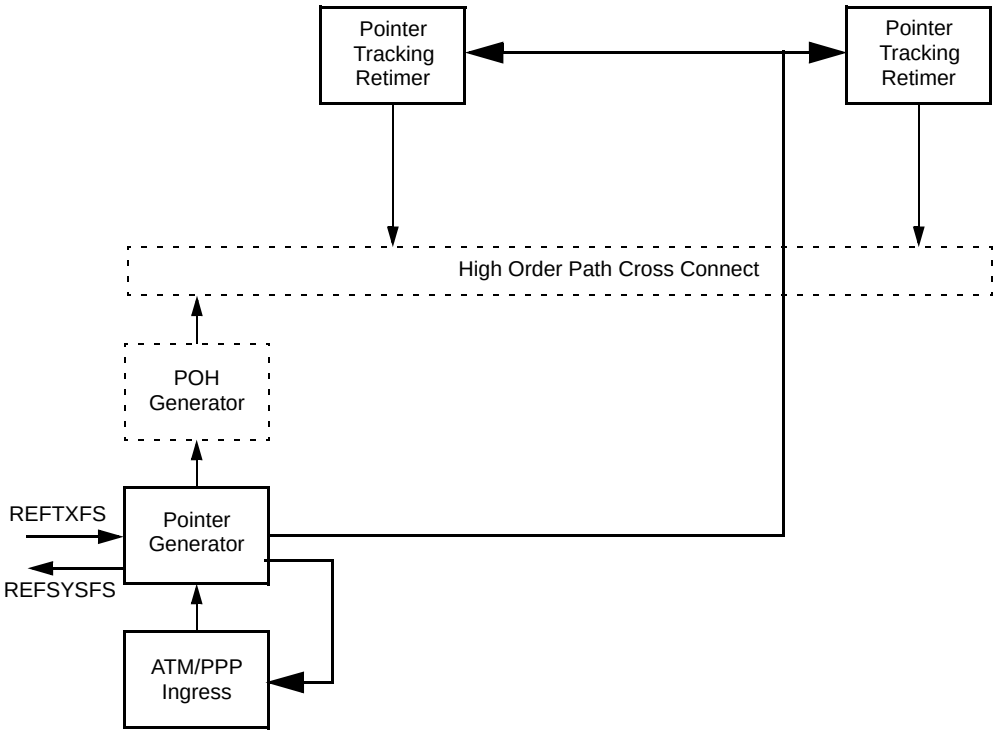


Figure 22. Frame Reference Pulse Generation

2.16.1 Generation of Frame Reference Pulse

A System Frame Reference Pulse is generated every 125 us (8 kHz) when **ExtFramePulseExpected** is deasserted. The generated System Frame Reference Pulse can be monitored or used by other devices in order to align with the PHAST-12P via the REFSYSFS lead.

2.16.2 Locking on External Frame Reference Pulse

When **ExtFramePulseExpected** is asserted, the PHAST-12P will lock on an external Frame Reference Pulse (REFTXFS lead) and will generate a System Frame Reference Pulse. When the distance between two consecutive Frame Reference Pulses is not exactly 125 us, a Loss Of Frame defect (LOF) will be generated.

This LOF defect is cleared as soon as two consecutive pulses with a distance of 125 us have been received. The System Frame Reference Pulse will still be generated during LOF state, locked on previously accepted Frame Pulse.

Sampling of the Frame Reference Pulse is configurable on the positive or the negative system clock edge (**ExtFramePulseNegEdge**).

Optionally an offset between the external Frame Reference Pulse and the internal System Frame Reference Pulse can be provided (**ExtFramePulseOffset**).

The generated System Frame Reference Pulse can be monitored via the REFSYSFS lead.

The relationship between REFTXFS and REFSYSFS is represented in Figure .

2.17 RETIMER FIFO LEAK REGISTERS

All Retimers in PHAST-12P are able to reduce the number of pointer justifications to reduce jitter on AU-3/AU-4/AU-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c pointers.

To provide this ability, the FIFO size is 29 words and the filling level of the FIFO is divided into several zones, as depicted in Figure 23. A FIFO word corresponds to one VC-n payload byte.

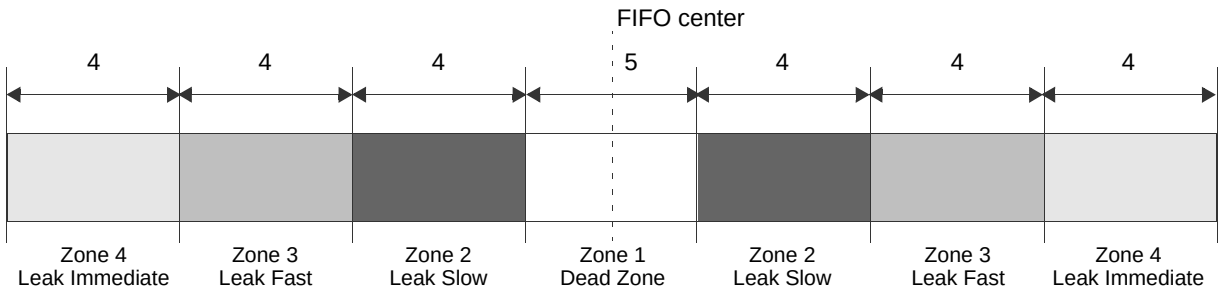


Figure 23. Retimer FIFO Filling Levels

The center zone is called Dead Zone and is 5 words wide. In this zone, the FIFO is at half filling and no pointer adjustments will be made.

If the FIFO is almost empty or almost full, immediate action is required. These filling levels are called Immediate Leak Zone. This zone is 4 words wide at each end of the filling level. If the FIFO filling level is in one of these zones, as much pointer justifications as allowed will be generated to adjust the filling level towards the dead zone, resulting in one justification generated every four SDH/SONET frames.

The remaining zones are the Slow Leak Zone and the Fast Leak Zone. Each of these zones is also 4 words wide. These are the zones that allow smoothing out jitter on the AU-3/AU-4/ AU-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c pointer values. The mechanism used to

obtain this uses a Justification Spacing counter per timeslot. This counter maintains a fixed distance between two consecutive Pointer Justifications and is used as long as the FIFO filling level is situated inside the Slow or Fast leak zones. The initial value for these countdown counters is set to the value provided by **SlowLeakRegister** or **FastLeakRegister**, according to the current zone.

Efficient smoothing out of the jitter can be obtained by providing accurate values for **SlowLeakRegister** and **FastLeakRegister**.

2.18 HIGH ORDER PATH OVERHEAD PROCESSING

The PHAST-12P device is compliant to the latest ITU/ETSI/ANSI standards and features regarding the generation and monitoring of the high order Path Overhead bytes.

2.18.1 High Order Path Overhead Generator

The PHAST-12P generates the high order path overhead bytes of all sourced VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STS-6c/STS-9c/STS-12c SPE channels.

- A single, 16 or 64 byte Trail Trace Identifier stored in the transmit POH RAM will be inserted in the J1 byte. Note that in case of a single or 16 byte Trail Trace Identifier the message must be repeated respectively 64 or 4 times.
- BIP-8 will be calculated over all bits of the preceding VC-n frame and will be inserted in the B3 byte of the current frame. The B3 byte in the transmit POH RAM is used as an errormask to corrupt the calculated B3 byte.
- The TSL signal label stored in the transmit POH RAM will be inserted in the C2 byte.
- Per high order path the REI can be sourced from
  - The transmit POH RAM
  - The transmit POH byte interface
  - The internal or external ring port
- The REI will be inserted into the G1 byte
- Per high order path the RDI can be sourced from
  - The transmit POH RAM
  - The transmit POH byte interface
  - The internal or external ring port
- The internal or external ring port can be selected as source for RDI/E-RDI.
  If **OneBitRDI** is deasserted, E-RDI will be encoded as follows (ordered from high to low priority):

E-RDI indication	b5	b6	b7
Server	1	0	1
Connectivity	1	1	0
Payload	0	1	0
None	0	0	1

If **OneBitRDI** is asserted, RDI will be generated as follows:

E-RDI indication	b5	b6	b7
Server	1	0	0
Connectivity	1	0	0
Payload	0	0	0
None	0	0	0

- The RDI will be inserted into the G1 byte.
- Per high order path the G1 spare bit can be sourced from
  - The transmit POH RAM
  - The transmit POH byte interface
- If the unidirectional option is active, 0x00 will be inserted in the G1 byte
- The F2 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- The H4 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- The F3 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- The K3 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- The N1 byte will be inserted from
  - The transmit POH RAM
  - The transmit POH byte interface
- Optionally insertion of VC-AIS, resulting in the insertion of all 1's in the entire VC
- Optionally insertion of Unequipped, resulting in the insertion of all 0's in the entire VC
- Optionally insertion of Supervisory Unequipped, resulting in the insertion of all 0's in the entire VC except for the POH bytes J1, B3 and G1
- Optionally bypass the POH generation: the entire high order path is just passed through

2.18.2 High Order Path Overhead Monitor

The PHAST-12P monitors the high order path overhead bytes on all incoming high order channels and terminates the path overhead bytes on all dropped channels.

- Optionally the single, 16 or 64 byte Trail Trace Identifier in the J1 byte will be monitored and the dTIM and dTTIZERO defects will be detected. For more information about the TTI process see “Trail Trace Identifier Process” on page 95.
- Optionally the accepted Trail Trace Identifier and stable indications will be reported for one configurable high order path. For more information about the reporting of TTI see “Trail Trace Identifier Process” on page 95.
- BIP-8 will be calculated over all bits of the preceding VC-n frame and will be compared to the B3 byte of the current frame
  - If one or more errors are detected, both a NearEndDefect_BlockCounter (1 block = 1 frame with 1 or more bit errors) and a NearEndDefect_BitCounter will be updated
  - The error counter per frame will be forwarded to the internal and external ring ports as REI indication
  - The dDEG defect will be detected for bursty or Poisson error distributions. For more information about these processes see “BER Supervision for B2/B3” on page 93.
  - The dEXC defect will be detected for Poisson error distribution. For more information about this process see “BER Supervision for B2/B3” on page 93.
  - During incoming SSF, the counters are not updated and the value 0 is forwarded to the ring ports
- Received C2 is debounced on a 5 frames basis
  - Accepted C2 is reported
  - Changes in accepted C2 are reported
  - The dUNEQ defect will be detected when the accepted C2 equals the unequipped activation pattern 0x00
  - The dAIS defect will be detected when the accepted C2 equals the AIS activation pattern 0xff
  - The dPLM defect will be detected when the accepted C2 does not equal the expected TSL code or the “equipped non-specific” 0x01
- If one or more errors are indicated by the REI G1, the FarEndDefect_Counter will be updated.
  - Optionally bit errors will be counted
  - During incoming SSF, the counter is not updated
- Received RDI (3 bit) is debounced on a configurable number of frames basis (ETSI: 3, 5 Telcordia: 10)

- The dRDI, E-RDI Server, E-RDI Connectivity and E-RDI Payload defects will be detected according to the following table:

b5	b6	b7	Defects
0	0	0	No defect
0	0	1	No defect
0	1	0	dRDI-P
0	1	1	No defect
1	0	0	dRDI and dRDI-S
1	0	1	dRDI and dRDI-S
1	1	0	dRDI and dRDI-C
1	1	1	dRDI and dRDI-S

  - During incoming SSF or when the unidirectional option is active, all RDI defects are cleared
- Received K3 is debounced on a 3 frame basis
  - Accepted K3 is reported
  - Changes in accepted K3 are reported
- AIS will be inserted per high order path according to the following expression:

$$\begin{aligned} \mathbf{aTSF_{[path]}} &= \mathbf{dAIS_{[path]} * not\ AIS\_AIS\_Insert\_Disable} \\ &+ \mathbf{dSSF_{[path]} * not\ SSF\_AIS\_Insert\_Disable} \\ &+ \mathbf{dEXC_{[path]} * not\ EXC\_AIS\_Insert\_Disable} \\ &+ \mathbf{dUNEQ_{[path]} * not\ UNEQ\_AIS\_Insert\_Disable} \\ &+ \mathbf{dTIM_{[path]} * not\ TIM\_AIS\_Insert\_Disable_{[path]}} \end{aligned}$$

$$\begin{aligned} \mathbf{aAIS_{[path]}} &= \mathbf{AI\_TSF_{[path]}} \\ &+ \mathbf{dPLM_{[path]} * not\ PLM\_AIS\_Insert\_Disable} \\ &+ \mathbf{AIS\_Force_{[path]}} \end{aligned}$$

- RDI will be inserted per high order path according to the following expressions:

$$\mathbf{aE\text{-}RDI\text{-}S_{[path]}} = \mathbf{dSSF_{[path]} * not\ SSF\_RDI\_Insert\_Disable}$$

$$\begin{aligned} \mathbf{aE\text{-}RDI\text{-}C_{[path]}} &= \mathbf{dUNEQ_{[path]} * not\ UNEQ\_RDI\_Insert\_Disable} \\ &+ \mathbf{dTIM_{[path]} * not\ TIM\_RDI\_Insert\_Disable} \end{aligned}$$

$$\begin{aligned} \mathbf{aE\text{-}RDI\text{-}P_{[path]}} &= \mathbf{dPLM_{[path]} * not\ PLM\_RDI\_Insert\_Disable} \\ &+ \mathbf{dLCD_{[path]} * not\ LCD\_RDI\_Insert\_Disable} \end{aligned}$$

$$aRDI_{[path]} = aE\text{-}RDI\text{-}S_{[path]} + aE\text{-}RDI\text{-}C_{[path]}$$

- The defect correlations are applied as follows:

$$cSSF_{[path]} = dSSF_{[path]} + dAIS_{[path]} * \text{not AIS\_SSF\_Contribution\_Disable}$$

$$cAIS_{[path]} = dAIS_{[path]}$$

$$cUNEQ_{[path]} = dUNEQ_{[path]} * (\text{not } dSSF_{[path]} + SSF\_UNEQ\_Inhibit\_Disable) * (dTTIZERO_{[path]} + TTIZERO\_UNEQ\_Contribution\_Disable) * (dTIM_{[path]} + TIM\_UNEQ\_Contribution\_Disable)$$

$$cTIM_{[path]} = dTIM_{[path]} * (\text{not } dSSF_{[path]} + SSF\_TIM\_Inhibit\_Disable) * (\text{not } dUNEQ_{[path]} * \text{not UNEQ\_TIM\_Inhibit\_Disable} + \text{not } dTTIZERO_{[path]} * \text{not TTIZERO\_TIM\_Inhibit\_Disable} + UNEQ\_TIM\_Inhibit\_Disable * TTIZERO\_TIM\_Inhibit\_Disable)$$

$$cTTIZERO_{[path]} = dTTIZERO_{[path]} * (\text{not } dSSF_{[path]} + SSF\_TTIZERO\_Inhibit\_Disable)$$

$$cDEG_{[path]} = dDEG_{[path]} * (\text{not } dSSF_{[path]} + SSF\_DEG\_Inhibit\_Disable) * (\text{not } dTIM_{[path]} + TIM\_DEG\_Inhibit\_Disable)$$

$$cEXC_{[path]} = dEXC_{[path]} * (\text{not } dSSF_{[path]} + SSF\_EXC\_Inhibit\_Disable) * (\text{not } dTIM_{[path]} + TIM\_EXC\_Inhibit\_Disable)$$

$$cPLM_{[path]} = dPLM_{[path]} * (\text{not } AI\_TSF_{[path]} + TSF\_PLM\_Inhibit\_Disable)$$

cE-RDI(-S)(-C)(-P)$_{[path]}$ = dE-RDI(-S)(-C)(-P)$_{[path]}$
*** (not dSSF$_{[path]}$ + SSF_RDI_Inhibit_Disable**
*** (not dUNEQ$_{[path]}$ * not UNEQ_RDI_Inhibit_Disable**
+ not dTTIZERO$_{[path]}$ * not TTIZERO_RDI_Inhibit_Disable
+ UNEQ_RDI_Inhibit_Disable * TTIZERO_RDI_Inhibit_Disable)
*** (not dTIM$_{[path]}$ + TIM_RDI_Inhibit_Disable)**

- Optionally bypass the POH monitor: the entire high order path is passed through without processing.
  Note: The High order POH Monitor should be bypassed for unused high-order paths.

2.19 TOH PORT INTERFACE

The transmit TOH port interface allows insertion of the RSOH and MSOH bytes into the TOH.

All received TOH bytes are output on the receive TOH port interface.

Each interface consists of clock, data, data enable, address and address enable lines.

The address is a 10-bit word according to the (a, b, c) format specified by ITU-T G.707/Y.1322 clause 9.2.1 and Figure 9-1:

<table>
<tr><th>A9</th><th>A8</th><th>A7</th><th>A6</th><th>A5</th><th>A4</th><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>Line Interface Mode</th></tr>
<tr><td colspan="4" rowspan="2">Row number
a-1
(Range 0 to 8)</td><td colspan="4" rowspan="2">(Multi-)Column number
b-1
(Range 0 to 8)</td><td colspan="2">STM-1/OC-3 Line
(Range 0 to 3)</td><td>STM-1/OC-3 Mode</td></tr>
<tr><td colspan="2">Multi-Column Interleave Depth
c-1
(Range 0 to 3)</td><td>STM-4/OC-12 Mode</td></tr>
</table>

2.19.1 Transmit TOH Port Interface

This port interface allows insertion of the RSOH and MSOH bytes into the TOH. The TOH port interface is used to request any of the TOH bytes for either one STM-4 or four STM-1 frames from the outside world. Note the BIP bytes (B1, B2) have a special meaning, these can be used as an error mask on the calculated BIP.

The Transmit TOH Port consists of following leads:

- Output Transmit TOH Port Clock TOHTXCLK
- Output Transmit TOH Port Address Latch Enable TOHTXALE
- Output Transmit TOH Port Address TOHTXADDR
- Output Transmit TOH Port Data Latch Enable TOHTXDLE
- Input Transmit TOH Port Data TOHTXDATA

The transmit TOH Port protocol is as follows (see Figure):

1. The 10-bit address for the requested byte is output on TOHTXADDR, most significant bit first. During this time the Address Latch Enable TOHTXALE is asserted.
2. A one cycle gap is left open.
3. The Data Latch Enable TOHTXDLE is asserted and the 8-bit data word is sampled on the input TOHTXDATA, most significant bit first.

Note: Configuration of the Transmit TOH Port interface is done in the memory map of the TOH Generator (see **Table 38**). Selection of the TOH Port as source for a TOH byte is done in the TOH bytes internal memory by setting the most significant bit of the corresponding memory entry to '1'.

2.19.2 Receive TOH Port Interface

All received RSOH and MSOH bytes are sent over a serial Receive TOH Port interface. The values sent out on this interface are the raw, unprocessed values, except for B1 and B2, where an error mask is calculated (ones indicate the errored bits).

The Receive TOH Port consists of following leads:

- Output Receive TOH Port Clock TOHRXCLK
- Output Receive TOH Port Address Latch Enable TOHRXALE
- Output Receive TOH Port Address TOHRXADDR
- Output Receive TOH Port Data Latch Enable TOHRXDLE
- Output Receive TOH Port Data TOHRXDATA

The Receive TOH Port protocol is as follows (see Figure 10):

1. The 10-bit address for the transmitted byte is output on TOHRXADDR, most significant bit first. During this time the Address Latch Enable TOHRXALE is asserted.
2. A one cycle gap is left open.
3. The 8-bit data of the transmitted TOH byte is output on TOHRXDATA. During this time the Data Latch Enable TOHRXDLE is asserted.

Note: Configuration of the Receive TOH Port interface is done in the memory map of the TOH and DCC Port (see Table 41). The Receive TOH Port interface has to be enabled by the **TOH_Port_Enable** setting. No bytes will be sent out when this port is disabled.

2.20 DCC PORT INTERFACE

The Transmit and the Receive DCC Port interfaces provide an interface to the RS or MS DCC bytes. The interface is a constant bit-rate serial interface, each consisting of a clock and a data line.

2.20.1 Transmit DCC Port Interface

The Transmit DCC ports are constant bit-rate ports that provide a possible source for either the RS or the MS DCC bytes in the outgoing STM-4 or the four STM-1 frames. In STM-4 mode, only the first DCC Port is active.

Each Transmit DCC port can be configured for RS DCC bytes or MS DCC bytes:

RSOH_DCC_Select	Mode
0 (Default)	MS DCC bytes mode: the Transmit DCC port will request the MS DCC bytes.
1	RS DCC bytes mode: the Transmit DCC port will request the RS DCC bytes.

The Transmit DCC Port consists of following leads:

- Inputs Transmit DCC Data DCCTXDATA1...4
- Outputs Transmit DCC Clock DCCTXCLK1...4

The index indicates the port, one per transmit line. The Transmit DCC Clocks DCCTXCLK1...4 have a constant frequency and depend on the configured mode, as indicated in following table:

RSOH_DCC_Select	DCCTXCLK frequency (kHz)
0	576
1	192

Note: Configuration of the Transmit DCC Port interface is done in the memory map of the TOH Generator (see Table 38). The Transmit DCC port has to be enabled by the **DCC_Port_Enable** setting. If the Transmit DCC Port is disabled, the Transmit Port Clock DCCTXCLK output will be held low.

2.20.2 Receive DCC Port Interface

The Receive DCC ports are constant bit-rate ports that provide either the received RS DCC bytes or the received MS from the incoming STM-4 or the four STM-1 frames. In STM-4 mode, only the first DCC Port is active.

Each Receive DCC port can be configured for RS DCC bytes or MS DCC bytes:

RSOH_DCC_Select	Mode
0 (Default)	MS DCC bytes mode: the Receive DCC port will send the MS DCC bytes.
1	RS DCC bytes mode: the Receive DCC port will send the RS DCC bytes.

The Receive DCC Port consists of following leads:

- Outputs Receive DCC Data DCCRXDATA1...4
- Outputs Receive DCC Clock DCCRXCLK1...4

The index indicates the port, one per receive line. The Receive DCC Clocks DCCRXCLK1...4 have a constant frequency and depend on the configured mode, as indicated in following table:

RSOH_DCC_Select	DCCTXCLK frequency (kHz)
0	576
1	192

Note: Configuration of the Receive DCC Port interface is done in the memory map of the TOH and DCC Port (see Table 41). The Receive DCC port has to be enabled by the **DCC_Port_Enable** setting. If the Receive DCC Port is disabled, the Receive Port Clock DCCRXCLK output will be held low.

2.21 LINE ALARM INDICATION (RING) PORT INTERFACE

The Line Alarm Indication (Ring) Port Interface transports the Remote Information (RI) from the TOH sink/monitor to the TOH source/generator. The Remote Information consists of the REI and RDI values to be inserted by the TOH generator.

The TOH monitors send the Remote Information of all SDH/SONET lines to the Receive Line Alarm Indication (Ring) Port Interface. This port multicasts the information internally to the POH generator and externally to the Receive Alarm Indication (Ring) Port Interface.

The source for the Remote Information can be selected in the TOH generator, per SDH/SONET line. When the Remote Information is taken from the Transmit Line Alarm Indication (Ring) Port Interface, it is possible to configure the Line Alarm Indication (Ring) Port Interface to use the internally or externally available information.

2.21.1 Internal Line Alarm Indication (Ring) Port Interface

When sink and source are handled on one device, the internal ring port can be used (**ExternalSourceSelect** deasserted). The Transmit Line Alarm Indication (Ring) Port Interface leads must then be connected to VSS.

Figure 24 shows the use of the internal Line Alarm Indication (Ring) Port Interface.

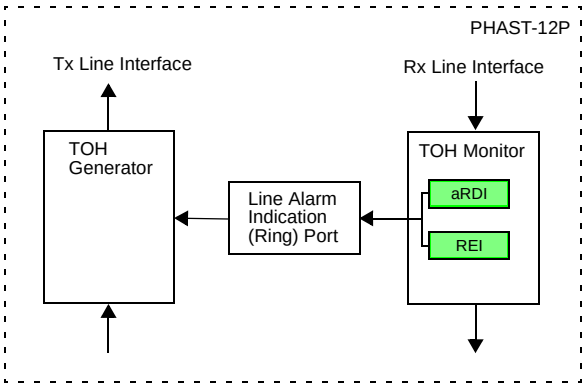


Figure 24. Internal Line Alarm Indication (Ring) Port Interface

2.21.2 External Line Alarm Indication (Ring) Port Interface

The external Line Alarm Indication (Ring) Port Interface is necessary when sink and source are processed on two different devices. The Receive Line Ring Port / Alarm Interface of the sink has to be connected to the Transmit Line Ring Port / Alarm Interface of the source and the external source mode has to be selected (**ExternalSourceSelect** asserted).

Figure 25 shows the use of the external Line Alarm Indication (Ring) Port Interface.

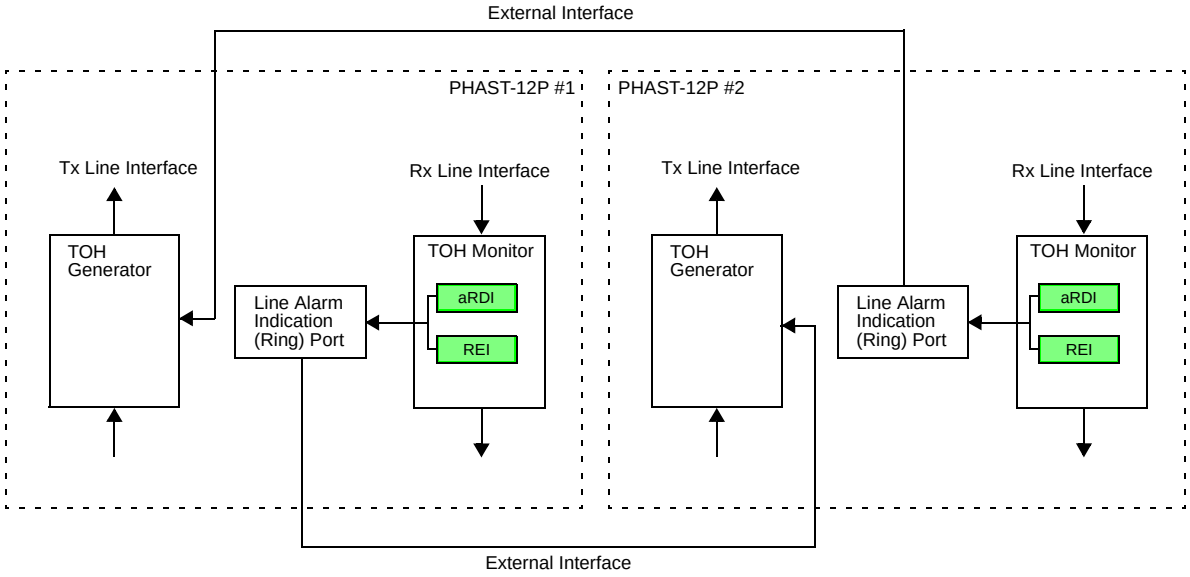


Figure 25. External Line Alarm Indication (Ring) Port Interface

Line	1								2								3								4							
Bit	11	10	...	4	3	2	1	0	11	10	...	4	3	2	1	0	11	10	...	4	3	2	1	0	11	10	...	4	3	2	1	0

Figure 26. TOH Ring Port Data Frame

Table 3: TOH Ring Port: Alarm Mappings, per Line

Bit position	Description
11	RDI[d]
10 down to 4	REI[ac]
3 down to 0	CRC4[b]

a. In STM-4/OC-12 mode REI located in Line 1 only.
b. The CRC4 polynomial is X4+X+1, initialized to all zeros and is transmitted MSB first. The corresponding RDI/REI are not accepted if a CRC4 error is detected.
c. Bit 2 to Bit 8 of the M1 byte is mapped to Bit 10 down to Bit 4 in the TOH Ring Port Data Frame.
d. Bit 11 is transmitted firat.

The external interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the Line Alarm Indication (Ring) Port data frame.

The data frame format is shown in above Figure 26 and the alarms are mapped per line as shown in above Table 3.

The Receive Line Alarm Indication (Ring) Port Interface consists of following leads:

- Output Receive Line Alarm Indication (Ring) Port clock LRPRXCLK
- Output Receive Line Alarm Indication (Ring) Port frame sync LRPRXFS
- Output Receive Line Alarm Indication (Ring) Port data LRPRXDATA

The Transmit Line Alarm Indication (Ring) Port Interface consists of following leads:

- Input Transmit Line Alarm Indication (Ring) Port clock LRPTXCLK
- Input Transmit Line Alarm Indication (Ring) Port frame sync LRPTXFS
- Input Transmit Line Alarm Indication (Ring) Port data LRPTXDATA

Refer to Figure 14 and Figure 15 for timing diagrams.

2.22 HIGH ORDER POH PORT INTERFACE

The transmit POH port interface allows insertion of the POH bytes.

All received High Order POH bytes are output on the receive High Order POH port interface.

Each interface consists of clock, data, data enable, address and address enable lines.

The address is an 8-bit word with following format:

A7	A6	A5	A4	A3	A2	A1	A0
High Order path number				POH byte identification			

The least significant nibble identifies the POH byte on the High Order POH Port Interface:

A3	A2	A1	A0	POH Byte
0	0	0	0	J1
0	0	0	1	B3
0	0	1	0	C2
0	0	1	1	G1
0	1	0	0	F2
0	1	0	1	H4
0	1	1	0	F3
0	1	1	1	K3
1	0	0	0	N1

The most significant nibble identifies the High Order path number:

A7	A6	A5	A4	Assigned to
0	0	0	0	VC-3/STS-1 SPE #1 or VC-4/STS-3c SPE #1
0	0	0	1	VC-3/STS-1 SPE #2
0	0	1	0	VC-3/STS-1 SPE #3

A7	A6	A5	A4	Assigned to
0	0	1	1	VC-3/STS-1 SPE #4 or VC-4/STS-3c SPE #2
0	1	0	0	VC-3/STS-1 SPE #5
0	1	0	1	VC-3/STS-1 SPE #6
0	1	1	0	VC-3/STS-1 SPE #7 or VC-4/STS-3c SPE #3
0	1	1	1	VC-3/STS-1 SPE #8
1	0	0	0	VC-3/STS-1 SPE #9
1	0	0	1	VC-3/STS-1 SPE #10 or VC-4/STS-3c SPE #4
1	0	1	0	VC-3/STS-1 SPE #11
1	0	1	1	VC-3/STS-1 SPE #12
1	1	0	0	NA
1	1	0	1	NA
1	1	1	0	NA
1	1	1	1	NA

Note the address corresponding to the master VC is used for concatenated structures. E.g., when mapping four VC-4/STS-3c's SPE in a STM-4/OC-12, only 0x0, 0x3, 0x6 and 0x9 will be valid values for A[7:4].

2.22.1 Transmit High Order POH Port Interface

The transmit High Order POH port interface allows inserting most High Order Path Overhead bytes into the High Order POH. J1 and C2 cannot be selected from the transmit High Order POH port interface, while the B3 BIP-8 can be used as error mask on the calculated BIP-8 for test purposes.

The Transmit POH Port consists of following leads:

- Output Transmit POH Port Clock POHTXCLK
- Output Transmit POH Port Address Latch Enable POHTXALE
- Output Transmit POH Port Address POHTXADDR
- Output Transmit POH Port Data Latch Enable POHTXDLE
- Input Transmit TOH Port Data POHTXDATA

The Transmit POH Port protocol is as follows (see Figure 13):

1. The 8-bit address for the requested byte is output on POHTXADDR, most significant bit first. During this time the Address Latch Enable POHTXALE is asserted.
2. A one cycle gap is left open.
3. The Data Latch Enable POHTXDLE is asserted and the 8-bit data word is sampled on the input POHTXDATA, most significant bit first.

Note: No configuration is necessary for the Transmit POH Port. The source of the POH bytes can be configured in the memory map of the POH Generator (see Table 92).

2.22.2 Receive High Order POH Port Interface

All received High Order Path Overhead bytes are sent over a serial Receive POH Port interface. The values sent out on this interface are the raw, unprocessed values, except for B3, where an error mask is calculated (ones indicates the errored bits).

The Receive POH Port consists of following leads:

- Output Receive POH Port Clock POHRXCLK
- Output Receive POH Port Address Latch Enable POHRXALE
- Output Receive POH Port Address POHRXADDR
- Output Receive POH Port Data Latch Enable POHRXDLE
- Output Receive POH Port Data POHRXDATA

The Receive POH Port protocol is as follows (see Figure 12):

1. The 8-bit address for the transmitted byte is output on POHRXADDR, most significant bit first. During this time the Address Latch Enable POHRXALE is asserted.
2. A one cycle gap is left open.
3. The 8-bit data of the transmitted TPOH byte is output on POHRXDATA. During this time the Data Latch Enable POHRXDLE is asserted.

Note: No configuration is necessary for this POH Port.

2.23 HIGH ORDER ALARM INDICATION (RING) PORT INTERFACE

The High Order Alarm Indication (Ring) Port Interface transports the Remote Information (RI) from the High Order POH sink/monitor to the POH source/generator. The Remote Information consists of the REI and (enhanced) RDI values to be inserted by the POH generator.

The High Order POH monitor sends the Remote Information of all High Order path channels to the Receive High Order Alarm Indication (Ring) Port Interface. This port multicasts the information internally to the POH generator and externally to the Receive Alarm Indication (Ring) Port Interface.

The source for the Remote Information can be selected in the POH generator, per high order path. When the Remote Information is taken from the Transmit High Order Alarm Indication (Ring) Port Interface, it is possible to configure the High Order Alarm Indication (Ring) Port Interface to use the internally or externally available information.

When the **ExtendRDI** option is asserted, the RDI insertion will be extended to minimum 20 frames.

2.23.1 Internal High Order Alarm Indication (Ring) Port Interface

When sink and source are handled on one device, the internal ring port can be used (**SelectExternalSource** deasserted). The Transmit High Order Alarm Indication (Ring) Port Interface leads must then be connected to VSS.

Figure 27 shows the use of the internal High Order Alarm Indication (Ring) Port Interface.

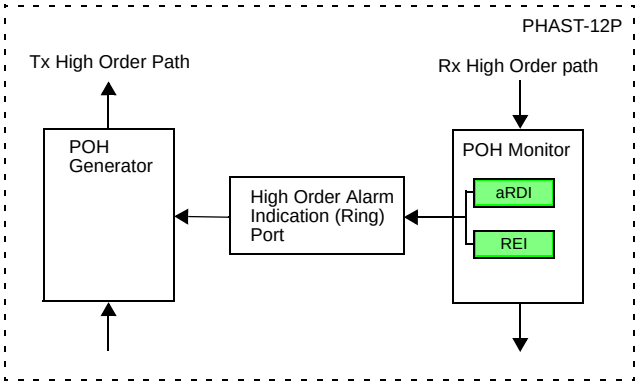


Figure 27. Internal High Order Alarm Indication (Ring) Port Interface

2.23.2 External High Order Alarm Indication (Ring) Port Interface

The external High Order Alarm Indication (Ring) Port Interface is necessary when sink and source are processed on two different devices. The Receive High Order Path Ring Port / Alarm Interface of the sink has to be connected to the Transmit High Order Path Ring Port / Alarm Interface of the source and the external source mode has to be selected (**SelectExternalSource** asserted).

Figure 28 shows the use of the external High Order Alarm Indication (Ring) Port Interface.

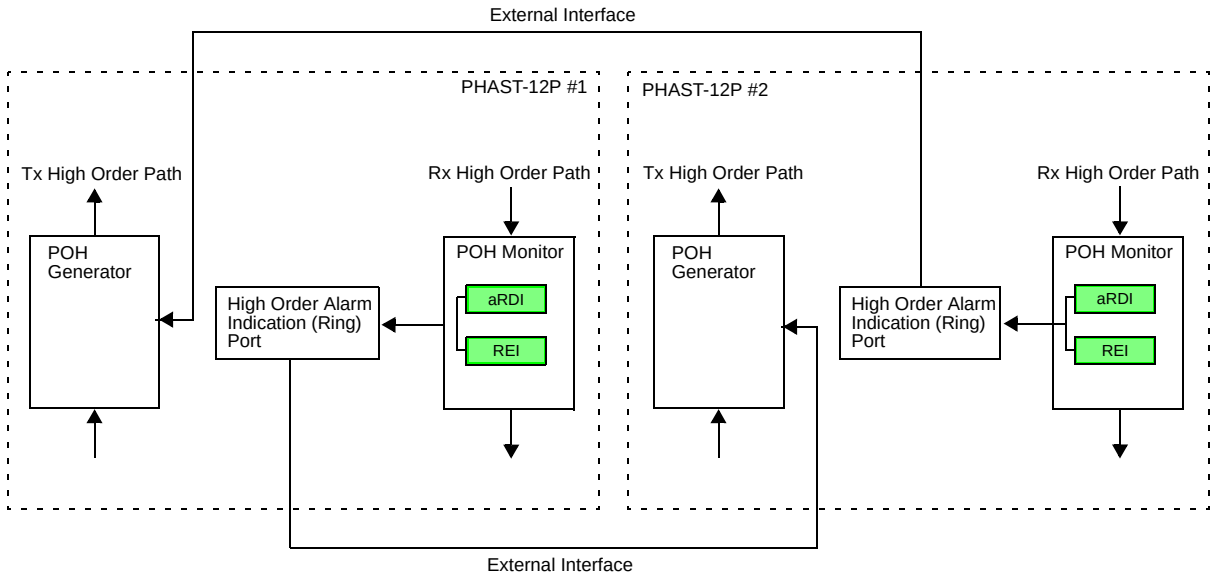


Figure 28. External High Order Alarm Indication (Ring) Port Interface

Timeslot	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit	31-0	31-0	31-0	31-0	31-0	31-0	31-0	31-0	31-0	31-0	31-0	31-0	Not Used			

Figure 29. High Order Ring Port Data Frame

Note: (Time slots 0-2) is output first, followed by Line 2 (Time slots 3-5), etc. Time slot 0 is the first VC-3 or VC-4 of Line 1, while Time slot 3 is the first VC-3 or VC-4 of Line 2, etc.

Table 4. High Order Ring Port: Alarm Mapping in Timeslot

Timeslot Bit number	Bit Name
31	REI_Valid[a]
30 down to 27	REI
26	Reserved
25	RDI_Valid
24	RDI_S
23	RDI_C
22	RDI_P
21	Reserved
20	Reserved
19	Reserved
18	Reserved
17	Reserved
16	Reserved
15 down to 4	Reserved
3 down to 0	CRC4

a.REI_Valid is set to 1 whenever the REI field carries a non-zero value.

The external interface consists of a clock, data and start of frame line. A start of frame pulse coincides with the first bit of the High Order Alarm Indication (Ring) Port data frame.

The data frame format is shown in above Figure 29 and the alarms are mapped per line as shown in above Table 4.

The Receive High Order Alarm Indication (Ring) Port Interface consists of following leads:

- Output Receive High Order Alarm Indication (Ring) Port clock PRPRXCLK
- Output Receive High Order Alarm Indication (Ring) Port frame sync PRPRXFS
- Output Receive High Order Alarm Indication (Ring) Port data PRPRXDATA

The Transmit High Order Alarm Indication (Ring) Port Interface consists of following leads:

- Input Transmit High Order Alarm Indication (Ring) Port clock PRPTXCLK
- Input Transmit High Order Alarm Indication (Ring) Port frame sync PRPTXFS
- Input Transmit High Order Alarm Indication (Ring) Port data PRPTXDATA

Refer to Figure 16 and Figure 17 for timing diagrams.

2.24 ATM CELL HANDLING

The PHAST-12P performs the following ATM PHY layer functions, according to [ITU-T I.432]:

- Egress: ATM cell demapping from SDH/SONET streams
  - Cell delineation including header error detection and correction
  - HEC checking
  - Filtering of idle cells, unassigned cells, user defined pattern cells, cells with uncorrected HEC error
  - Loss of Cell Delineation (LCD) detection and Tx RDI-P insertion
  - Rx FIFO overflow detection
  - Performance counters
- Ingress: ATM cell mapping into SDH/SONET streams
  - HEC checking, calculation and insertion
  - Insertion of idle, unassigned and user defined pattern cells
  - Performance counters

Cells are only passed to the ATM layer while processed in the SYNC state. Remark that the DELTAth cell that triggers the transition to the SYNC state will further be processed as in the SYNC state, this means filtering, descrambling and passing to ATM layer. The same applies to the ALPHAth cell that triggers the transition to the HUNT state, this cell will be further processed as in the HUNT state, i.e., no descrambling and no passing to the ATM layer.

Loss of Cell Delineation (LCD) signaling towards Tx path (through internal or external Ring port). During LCD, the SDH/SONET POH Generator will insert E-RDI Payload in the G1 byte, unless the insertion is disabled for that path.

Up to 12 ATM streams can be handled concurrently. On SDH/SONET, each ATM stream corresponds to a VC-3/VC-4/VC-4-Xc/STS-1/STS-3c/STC-6c/STS-9c/STS-12c SPE. On the UTOPIA interface, each ATM stream corresponds to a PHY.

2.24.1 Egress Direction

2.24.1.1 Shared Settings for all ATM streams

- Loss of Cell Delineation (LCD) integration time (0, 1, 2, 3 or 4 milliseconds)
- Enable/disable one second performance monitoring mechanism (shared with egress PPP)
- Number of free words which needs to be available before it is allowed to start writing a new cell to the Rx FIFO (shared with egress PPP). For ATM cell handling it is mandatory to set this value to 27.

2.24.1.2 Per ATM Stream Settings

- Enable/disable demapping (shared with egress PPP)
- Cell delineation
  - Threshold for leaving SYNC-state = ALPHA (1. . . 15)
  - Threshold for entering SYNC-state = DELTA (1. . . 15)
  - Enable/disable transition from Correction- to Detection-state while in SYNC: when disabled, single-bit HEC errors in consecutive cells are all corrected
  - Enable/disable single-bit HEC error correction
  - HEC offset (coset) pattern (0x00. . . 0xFF)
- Cell filtering (discard)
  - Match header pattern
  - Match header mask: to indicate don't care bits in the matching process
  - Enable/disable cell filtering for matched cells
  - Enable/disable cell filtering for ITU-T I.432 idle cells
  - Enable/disable cell filtering for ITU-T I.361 unassigned cells
  - Enable/disable cell filtering for cells with uncorrected HEC error

2.24.1.3 Per ATM Stream Status & Alarms

- Out of Cell Delineation (OCD)
- Loss of Cell Delineation (LCD)
- Overflow (shared with egress PPP)

2.24.1.4 Per ATM Stream Counters

- Number of cells (0. . . 2^{24}-1) forwarded towards Rx FIFO (shared with egress PPP)
- Number of cells (0. . . 2^{24}-1) discarded due to cell filtering (discards due to HEC errors are not counted)
- Number of cells (0. . . 2^{16}-1) with corrected HEC error
- Number of cells (0. . . 2^{16}-1) with uncorrected HEC error
- Number of cells (0. . . 2^{16}-1) discarded due to Rx FIFO overflow

The counters are only incremented while in the SYNC state.

The relationship between the ATM stream counters depends on whether or not cells with an uncorrected HEC error are filtered.

In case these cells are filtered, the sum of the number of cells forwarded towards Rx FIFO, the number of cells discarded due to cell filtering, the number of cells with uncorrected HEC error and the number of cells discarded due to Rx FIFO overflow is equal to the total number of cells received.

In case these are not filtered, the sum of the number of cells forwarded towards Rx FIFO, the number of cells discarded due to cell filtering and the number of cells discarded due to Rx FIFO overflow is equal to the total number of cells received.

Translation of the ATM cell stream addresses (0, 1,. . ., 11) into 12 configurable 5-bit UTOPIA PHY addresses is done in the UTOPIA interface block.

2.24.2 Ingress Direction

2.24.2.1 Shared Settings for all ATM streams

- Enable/disable one second performance monitoring mechanism (shared with ingress PPP)
- Number of words which needs to be available before it is allowed to start reading a new cell from the Tx FIFO (shared with ingress PPP). For ATM cell handling it is mandatory to set this value to 27

2.24.2.2 Per ATM Stream Settings

- Enable/disable mapping (shared with ingress PPP)
- HEC calculation and insertion
  - Enable/disable HEC calculation and insertion for ATM layer cells
  - Enable/disable HEC calculation and insertion for inserted idle/unassigned/user defined pattern cells. If disabled the HEC byte in the 5 bytes header value is used
  - HEC offset (coset) pattern (0x00. . . 0xFF)
  - HEC corruption mask (0x00. . . 0xFF): the HEC is EXORed with this mask
  - UDF1 / HEC manipulation (none, HEC EXOR UDF1, HEC AND UDF1, HEC OR UDF1)
- Idle/Unassigned/user defined pattern cell insertion
  - 5 bytes header value
  - Payload mode:
    - Fixed to configured payload value
    - Incremented each cell
    - Incremented each byte and start each cell with the configured payload value
    - Incremented each byte and cross cell boundaries

2.24.2.3 Per ATM Stream Counters

- Number of cells (0. . . 2^{24}-1) received from Tx FIFO (shared with ingress PPP)
- Number of Idle/unassigned/user defined pattern cells (0. . . 2^{24}-1) inserted
- Number of corrupted cells (0. . . 2^{8}-1) received from Tx FIFO (cells with HEC error)

The sum of the number of cells received from Tx FIFO and the number of idle/unassigned/user defined pattern cells inserted is equal to the total number of cells forwarded.

Translation of the 12 configurable 5-bit UTOPIA PHY addresses into ATM cell stream addresses (0, 1,. . , 11) is done in the UTOPIA interface block.

When mapping into a certain SDH/SONET stream is disabled, software has to configure the POH Generator to insert the UNEQUIPPED activation pattern in the corresponding path.

2.25 PPP PACKET HANDLING

The PHAST-12P performs the following PPP PHY layer functions:

- Egress: PPP packet demapping from SDH/SONET streams
  - Descrambling
  - Address/Control fields checking and stripping
  - HDLC framing and byte destuffing (including escape character discarding)
  - FCS checking and stripping
  - 32/16 bit FCS
  - Rx FIFO overflow detection
  - Discarding of too short and too long frames
  - Discarding of frames with abort sequence
  - Frames with FCS error are not discarded, but passed to the POS-PHY interface with the RXERR signal asserted
  - Performance counters
  - Optional Transparent mapping
- Ingress: PPP packet mapping into SDH/SONET streams
  - Address/Control fields insertion
  - FCS insertion
  - 32/16 bit FCS
  - HDLC flag insertion and byte stuffing (including escape character insertion)
  - Optional multiple flag insertion
  - Scrambling
  - Tx FIFO underflow detection
  - Detection of errored packets and insertion of abort sequence
  - Performance counters
  - Optional Transparent mapping

The PHAST-12P will support octet-synchronous[1] mapping and demapping of HDLC-like PPP frames into and from SDH/SONET, as specified in [RFC2615] and [RFC1662].

Up to 12 PPP streams can be handled concurrently. Following modes are supported:

- One VC-4-4C/STS-12c, corresponding to one PHY
- Four VC-4/STS-3c, corresponding to four PHY's
- 12 VC-3/STS-1, corresponding to 12 PHY's

The PHAST-12P does not support Async-Control-Character-Map (ACCM) handling.

1. PPP octet boundaries are aligned with SDH High Order VC/SONET STS-SPE byte boundaries.

2.25.1 Egress Direction

2.25.1.1 Shared Settings for all PPP streams

The Frame Length is defined as the number of bytes between two flags (including the optional header and FCS 16 or 32).

- Minimum Frame Length (0. . . 127 bytes)
- Maximum Frame Length (0. . . 65535 bytes): all longer frames are always discarded
- Transparent fragment size (64, 128, 256 or 1024 bytes): size of each fixed-length POS-PHY “packet” (only used for PPP streams for which transparent mode is enabled)
- Enable/disable one second performance monitoring mechanism (shared with egress ATM)
- FIFO Threshold: the number of free words which has to be available in the synchronization FIFO in the Rx direction before the POS/ATM Demapper starts writing data from the SDH/SONET line to that FIFO. This value must always be greater than 4. Note that setting this value to X means that once writing of a packet to the FIFO is started, at least 2X-1 (2X-5 in Transparent mode) number of bytes can be written (shared with egress ATM).

2.25.1.2 Per PPP Stream Settings

- Enable/disable demapping (shared with egress ATM)
- Enable/disable descrambling
- Enable/disable transparent mode: when enabled, the HDLC functionality is bypassed, i.e., all payload bytes are passed through transparently (no framing, no byte destuffing, no abort detection, no FCS processing).
- Enable/disable Address and Control fields check: when enabled, packets of which the Address field does not equal 0xFF and/or the Control field does not equal 0x03 are filtered (discarded). (don’t care in transparent mode).
- Enable/disable Address and Control fields stripping: when enabled, Address and Control fields are stripped if their value is equal to 0xFF03 (don’t care in transparent mode)
- Enable/disable FCS check: when disabled, all consequent actions: status incl. counters & interrupts and signaling on POS-PHY interface are also disabled - see below (don’t care in transparent mode)
- Enable/disable FCS stripping (don’t care in transparent mode)
- FCS size (16 or 32 bit) (don’t care in transparent mode)

2.25.1.3 Per PPP Stream Status & Alarms

- FIFO Overflow: overflow occurred in Rx FIFO while a packet is being received (shared with egress ATM)

2.25.1.4 Per PPP Stream Counters

- Number of packets (0. . . 2^{24}-1) forwarded towards Rx FIFO (shared with egress ATM)
- Number of frames (0. . . 255) with FCS error, abort (0x7D7E) or mismatched Address/ Control fields
- Number of frames (0. . . 255) longer than Maximum Frame Length
- Number of frames (0. . . 255) shorter than Minimum Frame Length

Translation of the PPP packet stream addresses (0, 1,. . ., 11) into 12 configurable 5-bit POS-PHY addresses is done in the POS-PHY interface block.

2.25.2 Ingress Direction

When the Tx FIFO underruns during a frame transfer, the abort sequence (0x7D7E) is inserted.

2.25.2.1 Shared Settings for all PPP Streams

- Enable/disable one second performance monitoring mechanism (shared with ingress ATM)
- FIFO Threshold: the number of free words which has to be available in the synchronization FIFO in the Tx direction before the POS/ATM Mapper starts reading data from that FIFO. This value must always be different from 0. Note that setting this value to X means that once reading of a packet from the FIFO is started, at least X+1 number of words can be read (shared with ingress ATM).

2.25.2.2 Per PPP Stream Settings

- Enable/disable mapping (shared with Ingress ATM): when disabled, flag characters (0x7E) are inserted as payload (shared with ingress ATM)
- Enable/disable transparent mode. When enabled, the HDLC functionality is bypassed, i.e., all “packets” are transparently mapped into the payload (no interframe flag insertion, no byte stuffing, no abort handling, no FCS defined). Note that the transparent packets must always have an even number of bytes.
- Enable/disable Address (0xFF) and Control (0x03) Fields insertion (don’t care in transparent mode)
- Enable/disable FCS calculation (don’t care in transparent mode)
- FCS size (16 or 32 bit) (don’t care in transparent mode)
- Multiple Flag: selects the minimum number of flag characters (0x7E) that are inserted between 2 frames (one or two) (don’t care in transparent mode)
- Enable/disable scrambling

2.25.2.3 Per PPP Stream Alarms

- FIFO Underflow: underflow occurred in Tx FIFO while a packet is being transmitted

Note that in transparent mode an underflow error is only reported when it occurs in the middle of a packet (this means between a SOP and an EOP indication). Underflow error is not reported when it occurs in between packets (this means after an EOP indication but before the next SOP indication).

2.25.2.4 Per PPP Stream Counters

- Number of packets (0. . . 2^{24}-1) received from Tx FIFO (shared with ingress ATM)
- Number of frames (0. . . 255) for which a Tx FIFO underflow occurred while the frame is being transmitted
- Number of packets (0. . . 255) for which the error signal on the POS-PHY interface was asserted during the last word transfer of that frame

The sum of the number of packets received from Tx FIFO, the number of frames for which a Tx FIFO underflow occurred and the number of packets for which the error indication was asserted is equal to the total number of packets forwarded.

All PPP packets must have a minimum length of 10 bytes.

Translation of the 12 configurable 5-bit POS-PHY addresses into PPP packet stream addresses (0, 1,. . , 11) is done in the POS-PHY interface block.

When mapping into a certain SDH/SONET stream is disabled, software has to configure the POH Generator to insert the UNEQUIPPED activation pattern in the corresponding path.

2.26 UTOPIA INTERFACE

This is an UTOPIA Level 2 interface with cell level handshaking for up to twelve VC-3/STS-1 SPE cell streams, four VC-4/STS-3c SPE cell streams, or a single VC-4-4c/STS-12c SPE cell stream.

Each stream corresponds to a PHY port, to which a unique 5-bit address between 0x00 and 0x1E can be assigned. 0x1F is the null-PHY address.

Note: the UTOPIA Level 1 (single PHY) standard specifies both cell-level and octet-level handshaking. In single PHY mode, the PHAST-12P can be connected to and ATM layer device that is Level 1 compliant which does either cell-level or octet-level handshaking.

2.26.1 Transmit Interface

The transmit interface consists of the following leads:

- Input clock PPUTTXCLK
- Input address PPUTTXADDR(4-0)
- Input data PPUTTXDATA(15-0)
- Input parity PPUTTXPRTY
- Input start of cell PPUTTXSOPC
- Input write enable $\overline{\text{PPUTTXENB}}$
- Output cell available PPUTPTPACLAV(3-0)

The maximum clock frequency is 50 MHz and the data and control signals are transferred on the rising edge of this clock.

2.26.1.1 Shared Settings for all UTOPIA PHY Ports

- Enable/disable entire interface (shared with Tx POS-PHY)
- PHY Mode: single-PHY or multi-PHY (shared with Tx POS-PHY)
- Status Indication Mode: (shared with Tx POS-PHY)
- Direct status: at most 4 CLAV's are used, at most 4 PHY's are possible
- Multiplexed status with full addressing: 1 CLAV signal (CLAV0) is used, at most 31 PHY's are possible
- Multiplexed status with group addressing: 4 CLAV's are used, at most 31 PHY's are possible
- Odd or even parity (shared with Tx POS-PHY)
- Parity over data or data and control signals (shared with Tx POS-PHY)

- 16-bit databus width
- FIFO threshold high: the number of free words which has to be available in the Tx FIFO to trigger the high assertion of the related CLAV signal (shared with Tx POS-PHY). For UTOPIA it is mandatory to set this value to 27

2.26.1.2 Per UTOPIA PHY Port Settings

- Enable/disable PHY port (shared with Tx POS-PHY). Note this setting is only evaluated on selection of a PHY.
- PHY Port address (shared with Tx POS-PHY)

2.26.1.3 Per CLAV Setting

- Timeslot for direct status (shared with Tx POS-PHY)

2.26.1.4 Per UTOPIA PHY Port Status & Alarms

- Late SOC
- Early SOC
- Parity error (shared with Tx POS-PHY)
- Overflow Error (shared with Tx POS-PHY)

2.26.2 Receive Interface

The receive interface consists of the following leads:

- Input clock PPUTRXCLK
- Input address PPUTRXADDR(4-0)
- Output data PPUTRXDATA(15-0)
- Output parity PPUTRXPRTY
- Output start of cell PPUTRXSOPC
- Input read enable $\overline{\text{PPUTRXENB}}$
- Output cell available PPUTPRPACLAV(3-0)

The maximum clock frequency is 50 MHz and the data and control signals are transferred on the rising edge of this clock.

2.26.2.1 Shared Settings for all UTOPIA PHY Ports

- Enable/disable entire interface (shared with Rx POS-PHY)
- PHY Mode: single-PHY or multi-PHY (shared with Rx POS-PHY)
- Status Indication Mode: (shared with Rx POS-PHY)
  - Direct status: at most 4 CLAV's are used, at most 4 PHY's are possible
  - Multiplexed status with full addressing: 1 CLAV (CLAV0) signal is used, at most 31 PHY's are possible
  - Multiplexed status with group addressing: 4 CLAV's are used, at most 31 PHY's are possible
- Odd or even parity (shared with Rx POS-PHY)
- Parity over data or data and control signals (shared with Rx POS-PHY)

- 16-bit databus width
- FIFO threshold: the number of words which has to be available in the Rx FIFO to trigger the high assertion of the related CLAV signal (shared with Rx POS-PHY). For UTOPIA it is mandatory to set this value to 27

2.26.2.2 Per UTOPIA PHY Port Settings

- Enable/disable PHY port (shared with Rx POS-PHY)
- PHY Port address (shared with Rx POS-PHY)

2.26.2.3 Per CLAV Setting

- Timeslot for direct status (shared with Rx POS-PHY)

2.27 POS-PHY INTERFACE

This is a POS-PHY Level 2 interface with packet level handshaking for up to twelve VC-3/STS-1 SPE cell streams, four VC-4/STS-3c SPE cell streams, or a single VC-4-4c/STS-12c SPE cell stream.

Each stream corresponds to a PHY port, to which a unique 5-bit address between 0x00 and 0x1E can be assigned. 0x1F is the null-PHY address.

2.27.1 Transmit Interface

The transmit interface consists of the following leads:

- Input clock PPUTTXCLK
- Input address PPUTTXADDR(4-0)
- Input data PPUTTXDATA(15-0)
- Input parity PPUTTXPRTY
- Input start of packet PPUTTXSOPC
- Input end of packet PPUTTXEOP
- Input word modulo PPTXMOD
- Input error PPTXERR
- Input write enable $\overline{\text{PPUTTXENB}}$
- Output selected PHY packet available PPTXSTPA
- Output polled PHY packet available PPUTPTPACLAV(3-0)

The maximum clock frequency is 50 MHz and the data and control signals are transferred on the rising edge of this clock.

All incoming packets must be larger than 6 bytes.

2.27.1.1 Shared Settings for all POS-PHY Ports

- Enable/disable entire interface (shared with Tx UTOPIA)
- PHY Mode: single-PHY or multi-PHY (shared with Tx UTOPIA)
- Following two Status indication Modes are possible (mix is not supported - shared with Tx UTOPIA):
  - Direct status: at most 4 DTPA's are used, at most 4 PHY's are possible
  - Multiplexed status with full addressing: 1 PTPA (PTPA0) signal is used, at most 31 PHY's are possible
- Odd or even parity (shared with Tx UTOPIA)
- Parity over data or data and control signals (shared with Tx UTOPIA)
- FIFO threshold high: the number of free words which has to be available in the Tx FIFO to trigger the assertion of the related PTPA signal.
- FIFO threshold low: if there are equal or less free words available in the Tx FIFO, the related PTPA signal is deasserted
- Threshold: if there are equal or less free words available in the Tx FIFO, the related STPA signal is deasserted

2.27.1.2 Per POS-PHY Port Settings

- Enable/disable PHY port (shared with Tx UTOPIA)
- PHY Port address (shared with Tx UTOPIA)

2.27.1.3 Per CLAV Setting

- Timeslot for direct status (shared with Tx UTOPIA)

2.27.1.4 Per POS-PHY Port Status & Alarms

- SOP-EOP error
- Parity error (shared with Tx UTOPIA)
- Overflow error (shared with Tx UTOPIA)

2.27.2 Receive Interface

The receive interface consists of the following leads:

- Input clock PPUTRXCLK
- Input address PPUTRXADDR(4-0)
- Output data PPUTRXDATA(15-0)
- Output parity PPUTRXPRTY
- Output start of packet PPUTRXSOPC
- Output end of packet PPRXEOP
- Output word modulo PPRXMOP
- Output error PPRXERR
- Input read enable $\overline{\text{PPUTRXENB}}$
- Output data valid PPRXVAL
- Output polled PHY packet available PPUTPRPACLAV(3-0)

The maximum clock frequency is 50 MHz and the data and control signals are transferred on the rising edge of this clock.

2.27.2.1 Shared Settings for all POS-PHY Ports

- Enable/disable entire interface (shared with Rx UTOPIA)
- PHY Mode: single-PHY or multi-PHY (shared with Rx UTOPIA)
- Following two Status indication Modes are possible (mix is not supported - shared with Tx UTOPIA):
  - Direct status: at most 4 DRPA's are used, at most 4 PHY's are possible
  - Multiplexed status with full addressing: 1 PRPA (PRPA0) signal is used, at most 31 PHY's are possible
- Odd or even parity (shared with Rx UTOPIA)
- Parity over data or data and control signals (shared with Rx UTOPIA)
- FIFO threshold: the number of words which has to be available in the Rx FIFO to trigger the high assertion of the related CLAV signal. This value must always be larger than 0. Not that setting this value to X means that once the reading of a packet from the FIFO is started, at least X number of words can be read (shared with Rx UTOPIA)

2.27.2.2 Per POS-PHY Port Settings

- Enable/disable PHY port (shared with Rx UTOPIA). Note this setting is only evaluated on selection of a PHY.
- PHY Port address (shared with Rx UTOPIA)

2.27.2.3 Per CLAV Setting

- Timeslot for direct status (shared with Rx UTOPIA)

2.28 RELATIONSHIPS BETWEEN THRESHOLDS FOR PPP/POS-PHY MODE

Both in Rx and Tx direction the threshold at the Mapper/Demapper side (Thr1) and the threshold at the Interface side (Thr2) must obey to: Thr1 + Thr2 < 130.

2.29 LOOPBACKS

The PHAST-12P provides the following diagnostic loopbacks:

- receive line interface looped back to the transmit line interface
- transmit line interface looped back to the receive line interface

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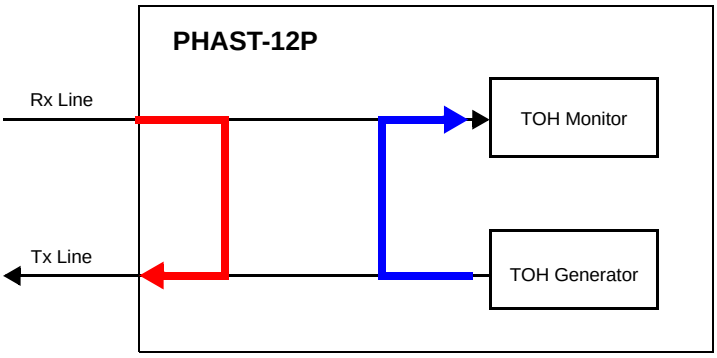


2.30 BER SUPERVISION FOR B2/B3

The PHAST-12P supports detection of the degraded signal (dDEG) and the excessive error (dEXC) defects for both line (B2 BIP-96 in STM-4/OC-12 mode, B2 BIP-24 in STM-1/OC-3 mode) and path (B3 BIP-8).

The assumed distribution of errors needs to be configured:

PoissonErrorCheck	Description
0 (Default)	Bursty distribution of errors is assumed (SDH).
1	Poisson distribution of errors is assumed (SONET).

2.30.1 Bursty Distribution of Errors

If a bursty distribution of errors is assumed, the excessive error defect is assumed to be false. The degraded signal defect detection is based on one second performance monitoring block error count.

Two sets of configuration registers are provided: one for setting the defect, one for clearing (to allow some hysteresis).

The degraded signal defect (dDEG) is declared if **DEG_DetectionWindowSize** consecutive bad intervals are detected - an interval is the one second period used for performance monitoring. For B2 (MSOH) an interval is declared bad if the number of errored blocks in that

interval is greater than or equal to **DEG_DetectionErrorThreshold**. For B3 (POH) an interval is declared bad if the number of errored blocks in that interval is greater than **DEG_DetectionErrorThreshold**. Remark the slight difference between the B2 (MSOH) and B3 (POH) detectors configuration!

The degraded signal defect (dDEG) is cleared if **DEG_RecoveryWindowSize** consecutive good intervals are detected. An interval is declared good if the number of errored blocks in that interval is smaller than **DEG_RecoveryErrorThreshold**.

The parameters **DEG_DetectionWindowSize** and **DEG_RecoveryWindowSize** are provisionable in the range 2 to 10.

The threshold parameters **DEG_DetectionErrorThreshold** and **DEG_RecoveryErrorThreshold** are to be provisioned as a number of errored blocks in the range of 0 < threshold <= Number of blocks in the interval.

2.30.2 Poisson Distribution of Errors

If a Poisson distribution of errors is assumed, both the degraded signal and the excessive error defects need to be detected based on the accumulated BIP errors during intervals of configurable duration.

For each defect, two sets of configuration registers are provided: one for setting the defect, one for clearing (to allow some hysteresis).

The monitoring intervals for the degraded signal defect (dDEG) can be configured in steps of time base T. The value of time base T can be set to 500 µs or 125 µs via the **DEG_Use125usCounter** configuration.

The degraded signal defect (dDEG) is declared if the accumulated BIP error count since the start of the detection interval is greater than or equal to **DEG_DetectionErrorThreshold** errors. The interval duration is **DEG_DetectionWindowSize** * T.

The degraded signal defect (dDEG) is cleared if the accumulated BIP error count during the clearing interval is less than **DEG_RecoveryErrorThreshold** errors. The interval duration is **DEG_RecoveryWindowSize** * T.

The monitoring intervals for the excessive error defect (dEXC) can be configured in steps of time base T. The value of time base T can be set to 500 µs or 125 µs via the **EXC_Use125usCounter** configuration.

The excessive signal defect (dEXC) is declared if the accumulated BIP error count since the start of the detection interval is greater than or equal to **EXC_DetectionErrorThreshold** errors. The interval duration is **EXC_DetectionWindowSize** * T.

The excessive signal defect (dEXC) is cleared if the accumulated BIP error count during the clearing interval is less than **EXC_RecoveryErrorThreshold** errors. The interval duration is **EXC_RecoveryWindowSize** * T.

The Poisson detector can be configured to work in **BurstProtection** mode, in that case the configured error threshold needs to be exceeded during 2 consecutive intervals before the defect is declared. This way one can protect the state machine against a burst of BER errors.

For B3 (POH) the BIP error counters have a overflow behavior (instead of saturation). For those counters a large DetectionErrorThreshold combined with a large DetectionWindowSize can lead to an overflow and avoid correct detection of the DEG/EXC signal defects.

DetectionErrorThreshold and DetectionWindowSize (both for DEG and EXC detection) must always be configured in such way no overflow of the BIP error counter can occur. For B2 (TOH) the BIP error counters have a saturating behavior and are thus not vulnerable to this.

2.31 TRAIL TRACE IDENTIFIER PROCESS

2.31.1 TTI Formats

The following TTI formats or modes are supported:

- 16-byte trace message: 16-byte repeating pattern consisting of a 15-byte APId preceded by a one byte header. The most significant bits of the TTI bytes form a 16-bit TFAS with a 1 in the most significant bit of the first TTI byte (header byte) and a 0 in the most significant bit of the APId bytes.
- 64-byte trace message: a 64-byte repeating pattern consisting of a 63-byte APId preceded by a one byte header. The most significant bits of the TTI bytes form a 64-bit TFAS with a 1 in the most significant bit of the first TTI byte (header byte) and a 0 in the most significant bit of the APId bytes.
- 64-byte trace message with CR/LF: a 64-byte repeating pattern consisting of a 62-byte APId followed by a two byte trailer. The trailer consists of the <CR> and <LF> ASCII characters.
- Repeating non-specific byte: a repeating single byte with fixed (constant), but unspecified value.
- Repeating specific byte: a repeating single byte with fixed (constant) value. The remote end user knows in advance which value is expected.

Note: *The user has to specify TFAS, CRC or CR/LF both for monitoring (mismatch detection) and generation.

*The repeating specific byte is handled as a 16-byte trace message without TFAS.

The following TTI message types are supported:

J0	Repeating non-specific byte
	Repeating specific byte
	16-byte trace message
J1	Repeating non-specific byte
	16-byte trace message
	64-byte trace message with TFAS
	64-byte trace message with CR/LF

2.31.2 TTI Mismatch Process

The TTI framer frames on TFAS or CR/LF. The framer freewheels when not locked to allow mismatch detection when expecting a repeating specific byte.

The TIM defect is set when the received TTI does not match the format or value of the expected TTI during a configurable number of consecutive multiframes[1]. The TIM defect is

1. A multiframe is 16 or 64 frames, depending on the TTI format.

cleared when the received TTI has the same format and value as the expected TTI during a configurable number of consecutive multiframes.

In case of repeating non-specific byte mode, the defined expected value will be ignored. Comparisons are made with the previous samples.

2.31.3 TTI Report Process

The received TTI value is accepted when 3 subsequent identical 16 respectively 64 byte multiframes are received. Note that when both 16-byte and 64-byte trace message modes are supported as is the case for path overhead monitoring (J1), the received 16-byte trace message is only accepted when 4 subsequent identical 16 byte multiframes are received. This condition when the received TTI equals the accepted TTI is indicated as stable.

If the new multiframe TTI message is the same as the previously accepted message, only 1 multiframe is required to assert the Stable_1 indication. For the Stable_64 indication, 3 multiframes are needed and for the Stable_16 indication, 3 multiframes are needed in case no 64-byte trace message mode is supported, otherwise 4 multiframes are needed.

Latched registers are provided for the Stable indications. This guarantees consistency when the reported TTI message is being read out by software:

1. Clear the Stable indication latch (clear-on-write-1).
2. Read out the reported TTI message.
3. The Stable indication latch must still be deasserted. If not, the stable indication (and the reported message) may have changed during software read accesses.

Notes:

1: Stable_1 is the inverse of TIM1

2: Stable_16 will inhibit Stable_64

3: Stable_16 will also indicate stable one byte messages. In this case software has to compare the reported message bytes.

2.32 PERFORMANCE COUNTERS

2.32.1 SDH/SONET Related Performance Counters

The PHAST-12P supports the following SDH/SONET related performance counters:

- RS/section counters per line interface:
  - B1 error count, configurable to count either BIP errors or errored frames
- RS/section counters APS interface:
  - B1 errored frame count,
- MS/line counters per line interface:
  - B2 near-end errored BIP count
  - B2 near-end errored frame count
  - M1 far-end Error count, configurable to count either REI errors or errored blocks
  - Near-end defect second
  - Far-end defect second

- Pointer adjustment counters per high order path:
  - Incoming positive pointer adjustment count
  - Incoming negative pointer adjustment count
  - Outgoing positive pointer adjustment count
  - Outgoing negative pointer adjustment count
- POH counters per high order path:
  - B3 near-end errored BIP count
  - B3 near-end errored block count
  - G1 far-end error count, configurable to count either REI errors or errored blocks
  - Near-end defect second
  - Far-end defect second

All these performance counters are one second shadow counters: at the one second boundary the contents of each performance counter is latched into its one second shadow register, after which the performance counter is cleared. These one second shadow registers will hold their value during the entire period between two subsequent one second boundaries.

The one second shadow registers are available for software read-only access.

All errored BIP and Block counters are dimensioned to cover the maximum count value during a one second interval meaning they can never reach saturation.

The one second boundary is generated by the internal one second clock which is either derived from the PHAST-12P system clock or from the external REFONESECCLK input lead.

The performance counters can be reset by writing 0x91 into the **ResetCounters** register.

2.32.2 ATM/PPP Related Performance Counters

The PHAST-12P supports the following ATM/PPP related performance counters:

- ATM demapping:
  - Number of cells forwarded to the FIFO
  - Number of cells discarded due to cell filtering
  - Number of cells discard due to FIFO overflow
  - Number of cells with corrected HEC error
  - Number of cells with uncorrected HEC error
- ATM mapping:
  - Number of good cells received from the FIFO
  - Number of idle/unassigned cells inserted
  - Number of corrupted cells received from the FIFO
- PPP demapping:
  - Number of packets forwarded to the FIFO
  - Number of frames with an FCS error, abort sequence or mismatched Address/Control fields
  - Number of frames longer than the maximum frame length
  - Number of frames shorter than the minimum frame length

- PPP mapping
  - Number of good packets received from the FIFO
  - Number of frames for which a FIFO underflow occurs while the frame is being transmitted
  - Number of packets for which the error signal on the POS-PHY Level 2 interface was asserted during the last word transfer of that packet

The behavior of the ATM/PPP related counters depends on wether or not the one second mechanism is enabled.

When the one second mechanism is enabled the counters behave in the same manner as the SDH/SONET counters. This means that at the one second boundary, the contents of each counter is latched into its one second shadow register and the counter is cleared. The one second shadow registers will hold their value during the entire period between two subsequent one second boundaries.

When the one second mechanism is disabled, the software has full control over the moment a counter is copied to its shadow register. If the software does a read access to a shadow register, the content of the related counter is copied to this shadow register and the counter is cleared. The shadow register will hold its value until the software again does a read access to it. Note that only the counter related to the accessed shadow register will be copied and cleared, all other counters are left untouched. Note also that in case of a 24-bit counter, the software first has to read the 2 least significant bytes. At this moment the counter is copied into its shadow registers and cleared. Reading the most significant byte will not clear the counter.

The latching mechanism can be configured for the ATM/PPP Mapper and the ATM/PPP Demapper separately.

OneSecondPM_Enable	Description
0 (Default)	Clear-on-read mechanism: the counters are copied to the shadow registers and cleared upon a read access.
1	One second mechanism: the counters are copied to the shadow registers and cleared every second.

All these counters are saturating: counting will stop when the maximum count value is reached.

The one second boundary is generated by the internal one second clock which is either derived from the PHAST-12P system clock or from the external REFONESECCLK input lead.

The performance counters can be reset by writing 0x91 into the **ResetCounters** register.

2.33 DEFECTS AND INTERRUPTS

2.33.1 Unlatched Defects (Correlated)

Defects representing the current status of the device are correlated to fault causes (correlated defects). This inhibition process avoids the unnecessary generation of interrupts, when a defect that is at an high hierarchy leads to the generation of multiple lower order defects. Unlatched defects are read-only.

2.33.2 Latched Defects

Changes in the state of defects are latched by the PHAST-12P. The edge on which latching occurs is configurable through the **LatchForIntCtrl** control register:

- Both rising and falling edges are latched (default)
- Only rising edges are latched, or
- Only falling edges are latched

Latched defects are cleared by a clear-on-write-1 mechanism (COW-1). This way software/ firmware can clear a defect when it will be handled. Software must never write a '1' to a latched defect that was previously read to be '0', because between the read and the write the defect may become active and will be cleared without software knowing it was active.

2.33.3 Defects Mask

Each latched defect can optionally contribute to the device hardware interrupt. The contribution of each individual latched defect can be enabled/disabled by clearing/setting the corresponding mask[1]:

$$\text{Summary} \leftarrow \Sigma\,(\text{Defect\_Latch}_i \text{ AND not Defect\_Mask}_i)$$

2.33.4 Interrupts

The contribution of groups of latches can in turn be combined into a summary latch with associated mask, forming an interrupt tree:

$$\text{device interrupt} \leftarrow \Sigma\,(\text{Summary}_i \text{ AND not Summary\_Mask}_i)$$

At the device top level, the general interrupt summary latches and the APS interrupt summary latches contribute to the interrupt:

$$\textbf{HINT} \leftarrow \Sigma\,(\text{General\_Interrupt}_i \text{ AND not General\_Mask}_i)$$

OR

$$\Sigma\,(\text{APS\_Interrupt}_k \text{ AND not APS\_Mask}_k)$$

The hardware interrupt capability is enabled by setting the **HINTEN** control bit. While disabled, the hardware interrupt indication INT/IRQ output lead is inactive. When enabled, the device top level hardware interrupt is

$$\text{INT/}\overline{\text{IRQ}}\text{ output lead} \leftarrow (\textbf{HINT} \text{ AND } \textbf{HINTEN})$$

1. $\Sigma\,(x)$ is used to indicate a logical 'OR' of a number of logical expressions (x).

2.34 ALARM INTERRUPT TREE

Following legend is used:

[dim] = array of dimension “dim”, directly accessible

{dim} = array of dimension “dim”, which has to be accessed indirectly

(i) = the i'th element of the array (direct access)

\+ = OR

& = AND

~ = NOT

index ranges:

ho = range 0 to 11 (= #VCs)

li = range 0 to 3 (= #lines)

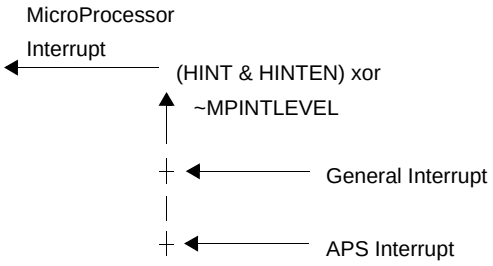


Figure 30. HINT

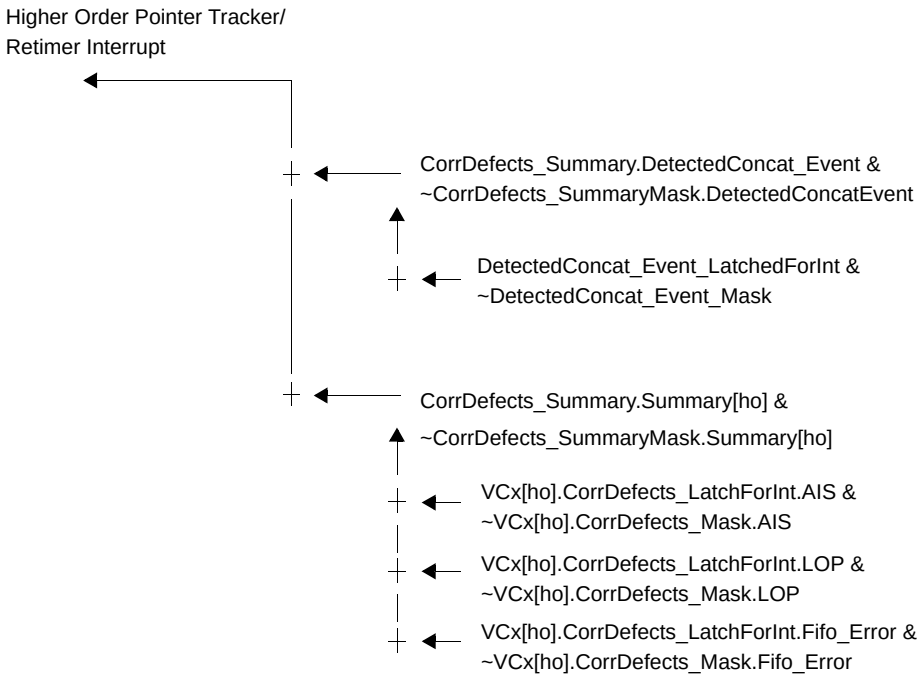


Figure 31. High Order Point Tracker Retimer Interrupt Tree

Figure 32. POH Monitor Interrupt Tree

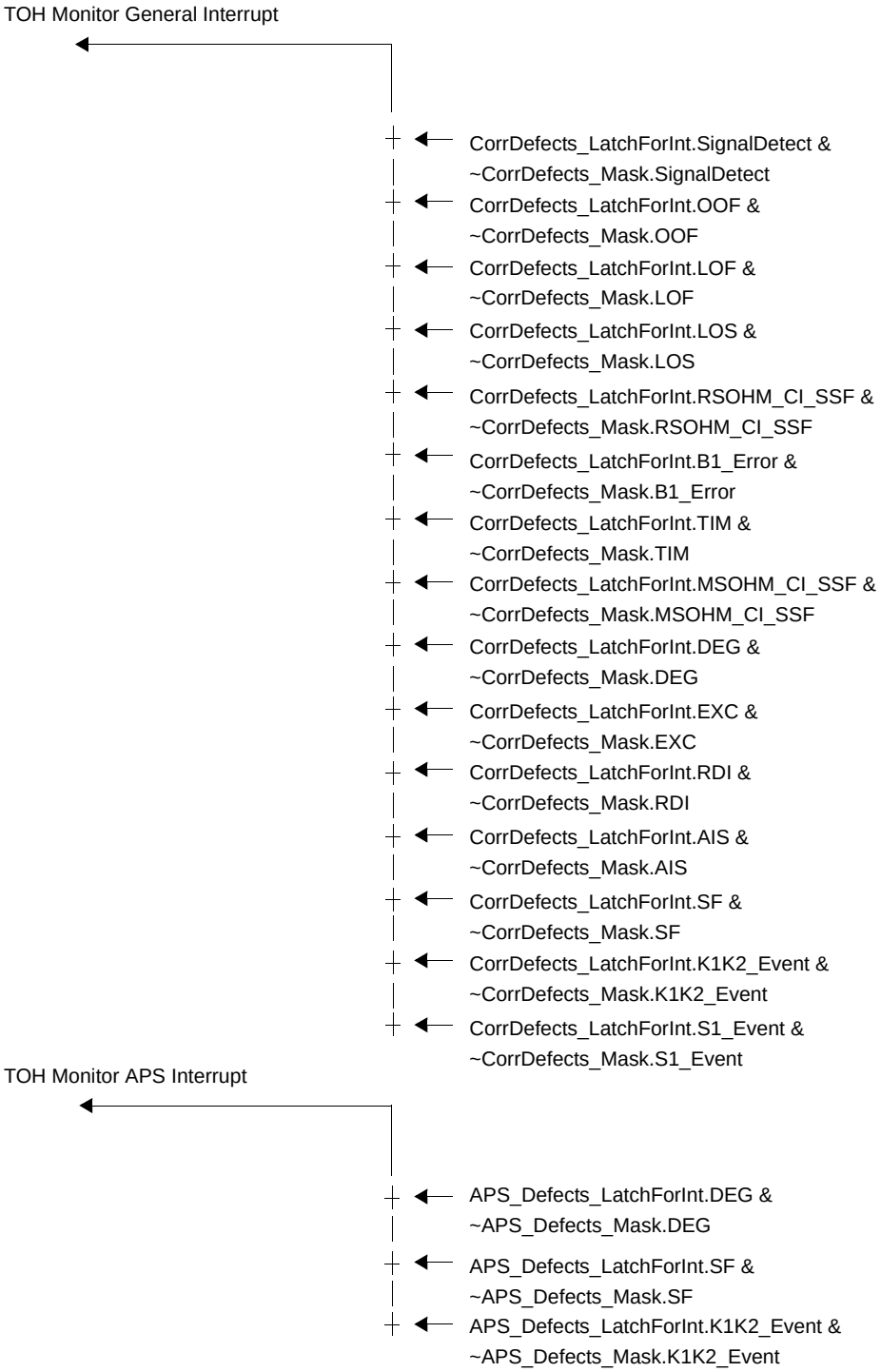


Figure 33. TOH Monitor Interrupt Tree

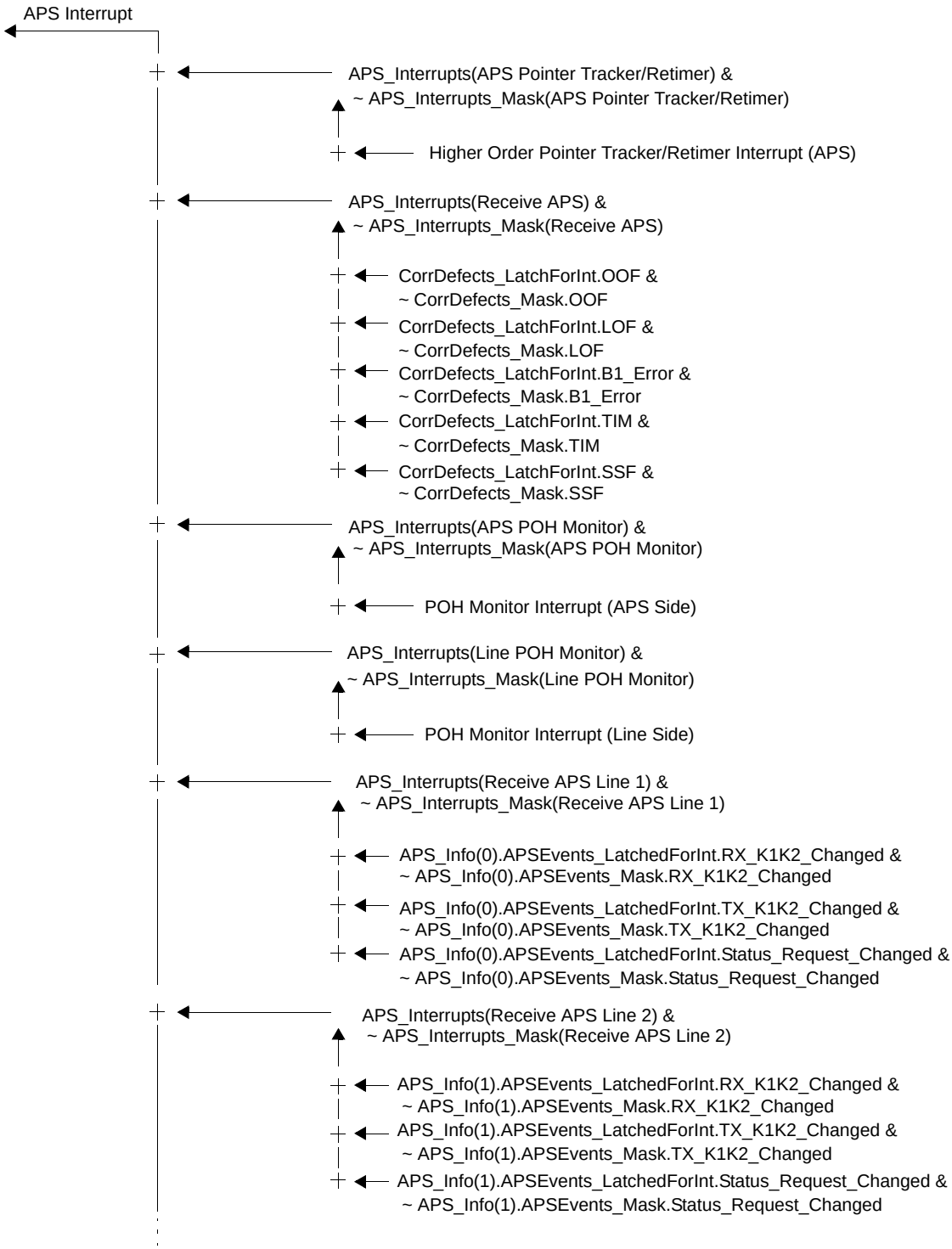


Figure 34. APS Interrupt Tree (part 1)

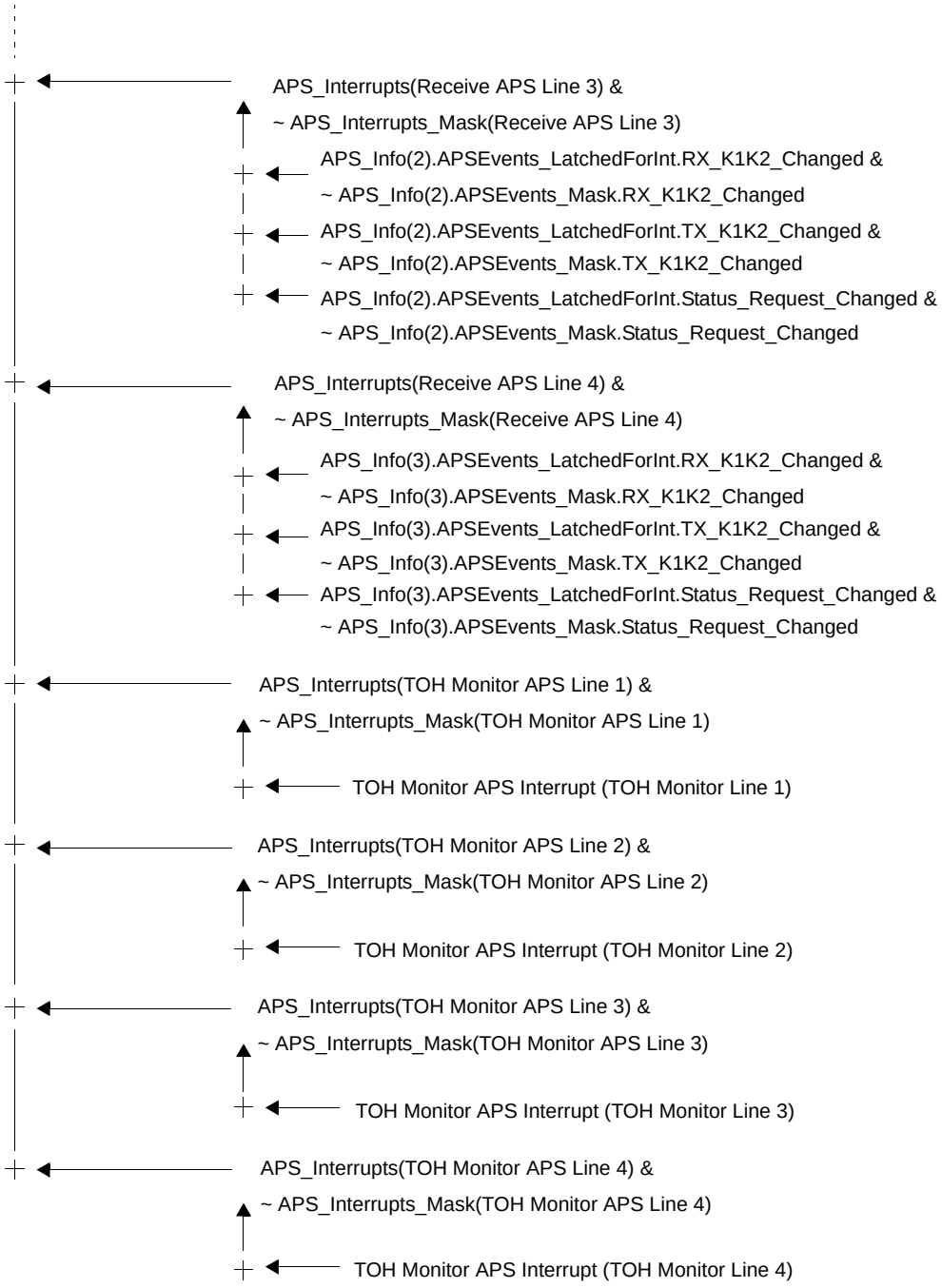


Figure 35. APS Interrupt Tree (part 2)

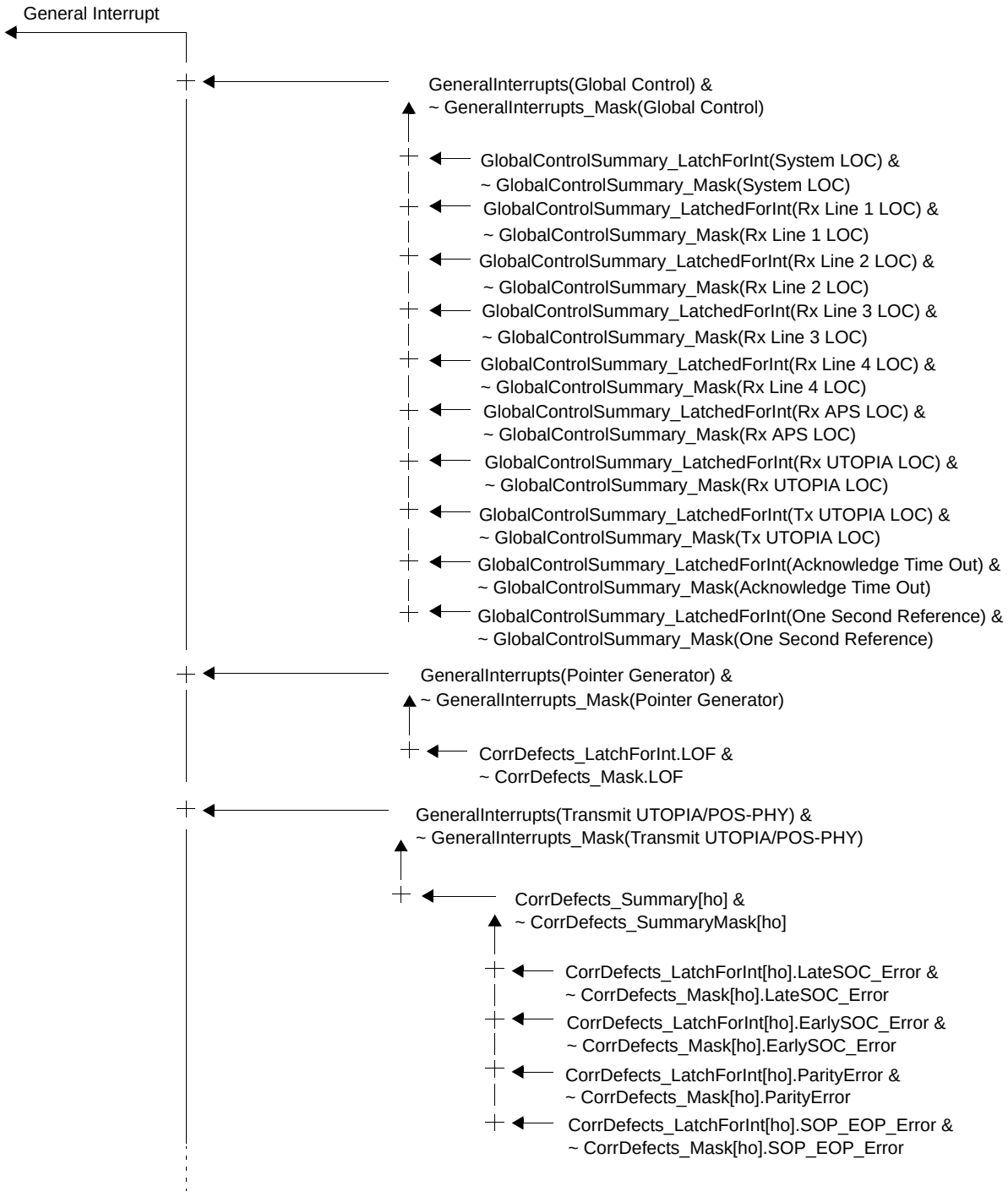


Figure 36. General Interrupt Tree (part 1)

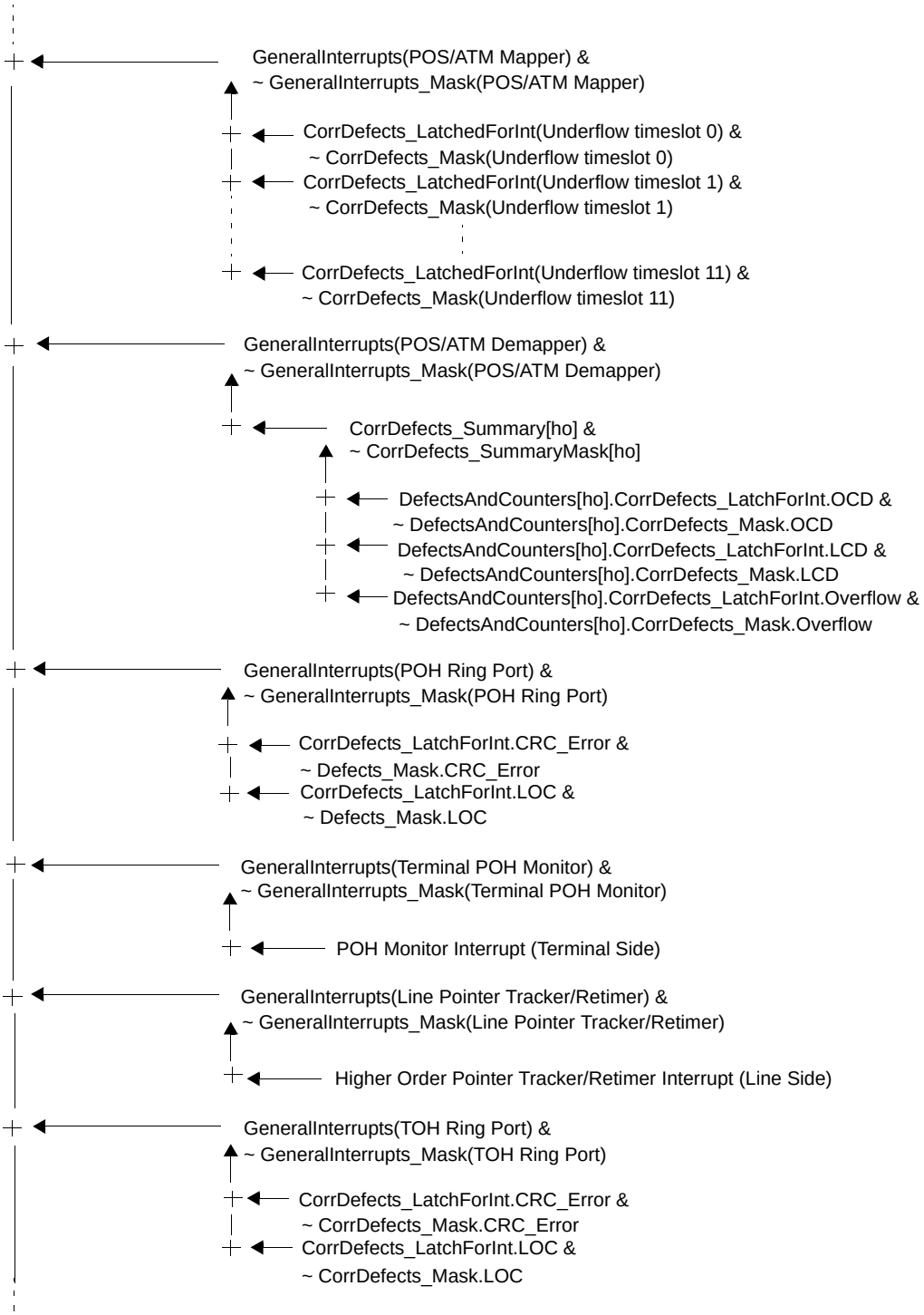


Figure 37. General Interrupt Tree (part 2)

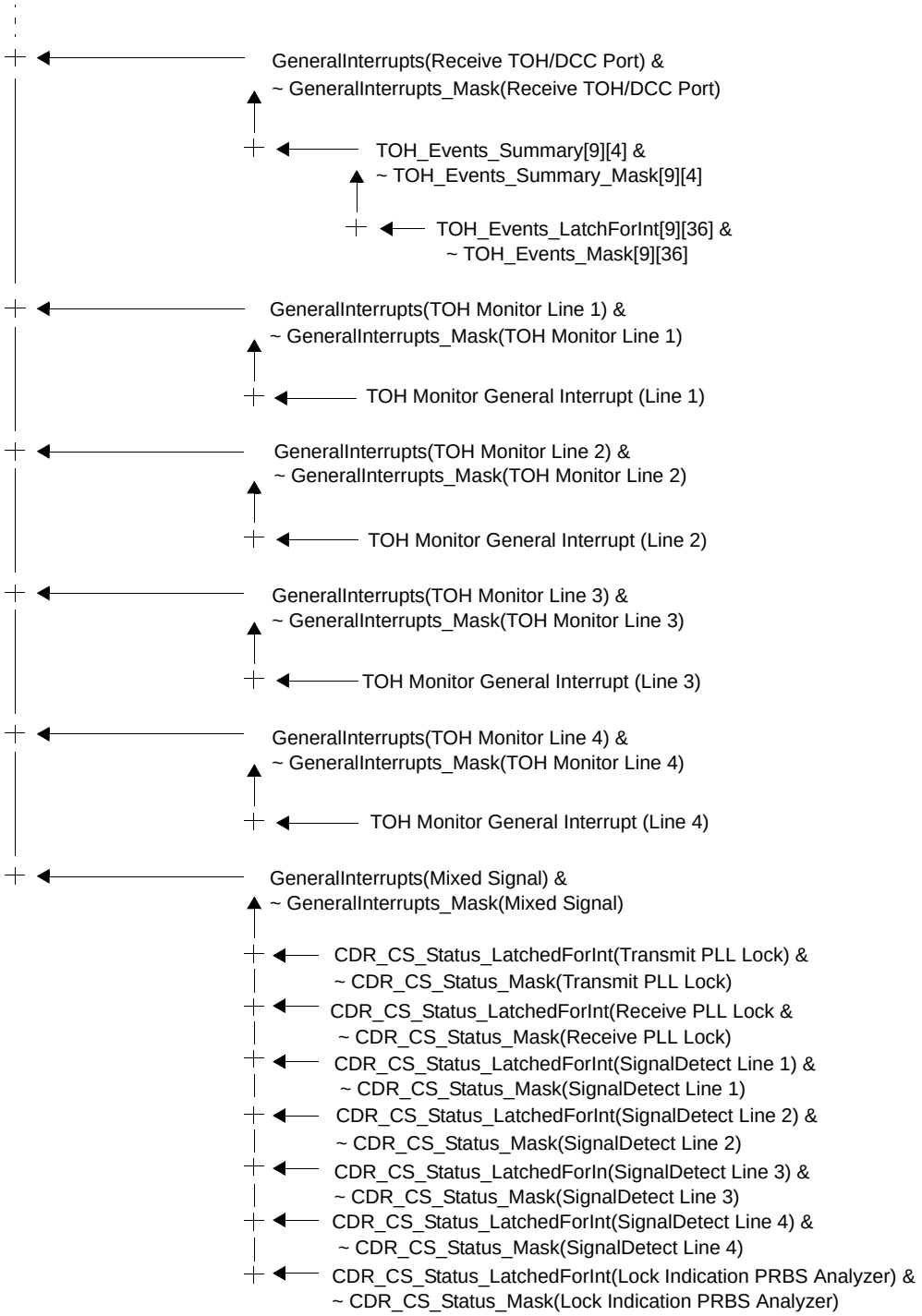


Figure 38. General Interrupt Tree (part 3)

3.0 BOUNDARY SCAN

3.1 INTRODUCTION

The Boundary Scan Interface Block provides a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in Figure 39, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure .

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 39.

The boundary scan function can be reset and disabled by holding lead $\overline{\text{TRS}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the PHAST-12P device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

3.2 BOUNDARY SCAN OPERATION

The maximum frequency the PHAST-12P device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 39.

The instruction register contains three bits. The PHAST-12P device performs the following three boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the PHAST-12P device to external circuitry.

The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the PHAST-12P boundary scan and instruction registers.

3.3 BOUNDARY SCAN RESET

Specific control of the $\overline{TRS}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the PHAST-12P. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value must be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the 'Input, Output and Input/Output Parameters' section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

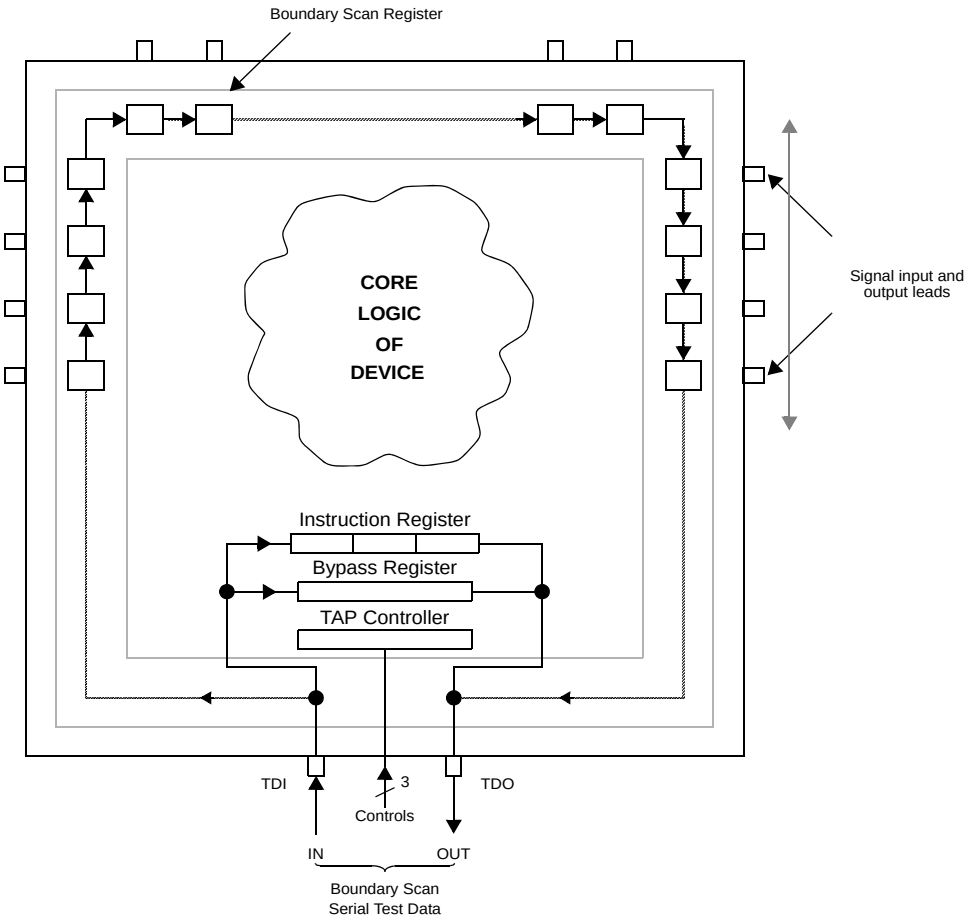
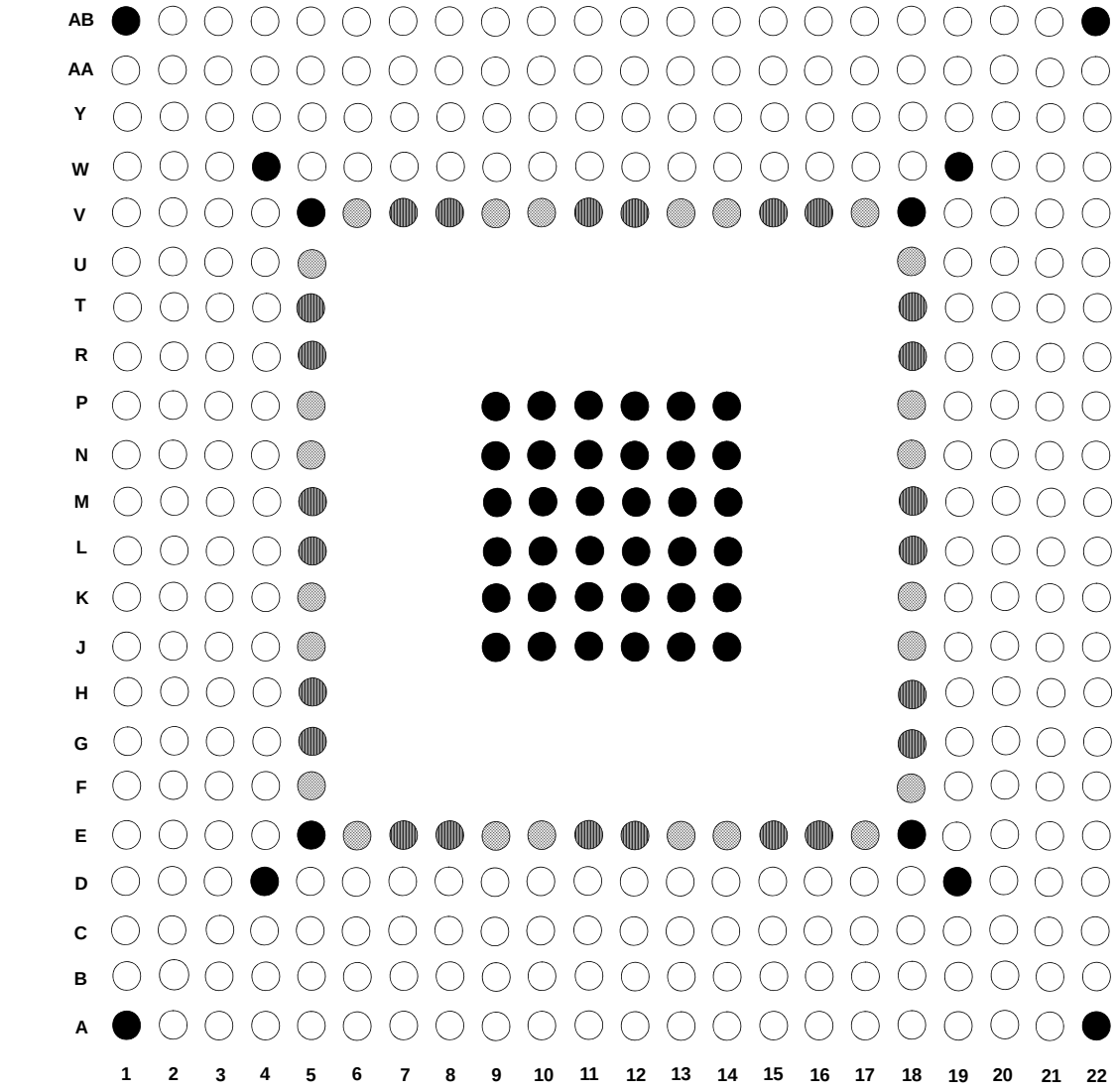


Figure 39. Boundary Scan Schematic

3.4 BOUNDARY SCAN CHAIN

A boundary scan description language (BSDL) source file is available via the Products page of the TranSwitch Internet World Wide Web site at www.transwitch.com.

4.0 TECHNICAL CHARACTERISTICS



Note: This is the bottom view. The leads are solder balls. See Figure 68 for package information. This view is rotated relative to the bottom view in Figure 68. Some signal Symbols have been abbreviated to fit the space available. The Symbols are shown in full in the Lead Description section.

Figure 40. PHAST-12P TXC-06412B 376-Lead Plastic Ball Grid Array Package Lead Diagram

4.1 LEAD DESCRIPTION

In the I/O/P column of the following tables, I = Input, O = Output, P = Power, T = Tristateable during normal operation. Entries in the Type column are defined in the Input, Output and Input/Output Parameters section.

All single-ended inputs (= LVTTL inputs) that are not used, must be connected to a low level.

Differential inputs (= LVPECL and LVDS inputs) that are not used can be left floating. They must be left in power-down mode, which is the default mode of these pads, after reset.

4.1.1 Power Supply, Ground, and No Connect Leads

Symbol	Lead No.	I/O/P	Name/Function
VDD18	E7, E8, E11, E12, E15, E16, G5, G18, H5, H18, L5, L18, M5, M18, R5, R18, T5, T18, V7, V8, V11, V12, V15, V16	P	**Digital Core 1.8V supply:** +1.8V +/-5%
VDDA18RPA	AB15, W16	P	**Rx PLL / Clock Recovery & Rx LVPECL analog 1.8V supply**
VDDA18TPA	AB13, Y9	P	**Tx PLL / Clock Synthesis & Tx LVPECL analog 1.8V supply**
VDD33	E6, E9, E10, E13, E14, E17, F5, F18, J5, J18, K5, K18, N5, N18, P5, P18, U5, U18, V6, V9, V10, V13, V14, V17	P	**Digital I/O 3.3V supply:** +3.3V +/-5%
VDDA33LVPCDRV	AB11, W10	P	**LVPECL driver analog 3.3V supply**
VDDA33LVPCIO	AA17, W11	P	**LVPECL pre-drive analog 3.3V supply**
VSS	A1, A22, AB1, AB22, D19, D4, E18, E5, J10, J11, J12, J13, J14, J9, K10, K11, K12, K13, K14, K9, L10, L11, L12, L13, L14, L9, M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, V18, V5, W19, W4	P	**Digital Core 1.8V & Digital I/O 3.3V returns**
VSSA18RPA	AA16, AB16	P	**Rx PLL / Clock Recovery & Rx LVPECL analog 1.8V return**
VSSA18TPA	AA8, AB12	P	**Tx PLL / Clock Synthesis & Tx LVPECL analog 1.8V return**
VSSA33LVPCPST	AA14, AA15	P	**LVPECL driver & pre-drive analog 3.3V returns**
NC	AA9, AB7, AB17, B6, C7, D3, F21, F22, G20, G21, G22, H19, H20, H21, H22, J19, J20, K19, L22, M21, M22, Y20		**No Connect:** These leads MUST not be connected, not even to another no connect lead, and must be left floating. Connection of an NC lead may impair the device performance or cause permanent damage to the device. NC leads may be assigned functions in future versions of the device, affecting its usability in current or future applications.
Reserved_Low	E22, J21, J22, K20, K21, K22, L19, L20, L21, M20		**For Future Use:** These leads are reserved for future use and should be tied to VSS.

4.1.2 Reference Voltages

Symbol	Lead No.	I/O/P	Type	Name/Function
VREF	W12			**1.2V Reference Voltage:** 1.2V reference voltage for all LVPECL and LVDS output drivers, and to bias the Rx and Tx PLLs.
VTERM	AB10			**1.2V Termination Voltage:** optional 1.2V termination voltage for the LVDS input buffer.

4.1.3 SDH/SONET Receive Line Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
LINERXDATA1P LINERXDATA1N	Y14 W13	I	LVPECL	**Serial SDH/SONET Receive Data #1:** 622.08/155.52 Mbit/s bit-serial data from electro/optical transceivers. Only LINERXDATA1P/N can be used in STM-4/OC-12 mode.
LINERXDATA2P LINERXDATA2N	Y15 W14	I	LVPECL	**Serial SDH/SONET Receive Data #2:** 155.52 Mbit/s bit-serial data from electro/optical transceivers. Can not be used in STM-4/OC-12 mode.
LINERXDATA3P LINERXDATA3N	W15 Y16	I	LVPECL	**Serial SDH/SONET Receive Data #3:** 155.52 Mbit/s bit-serial data from electro/optical transceivers. Can not be used in STM-4/OC-12 mode.
LINERXDATA4P LINERXDATA4N	AB18 AB19	I	LVPECL	**Serial SDH/SONET Receive Data #4:** 155.52 Mbit/s bit-serial data from electro/optical transceivers. Can not be used in STM-4/OC-12 mode.
LINERXSIGDET1	AA18	I	LVTTL	**Signal Detect #1:** Signal from the optical receiver for line #1 indicating signal presence. It is recommended to use this lead for LOS detection due to some fiber optic modules outputting noise during LOS.
LINERXSIGDET2	AB20	I	LVTTL	**Signal Detect #2:** Signal from the optical receiver for line #2 indicating signal presence. Not used in STM-4/OC-12 mode. It is recommended to use this lead for LOS detection due to some fiber optic modules outputting noise during LOS.
LINERXSIGDET3	W17	I	LVTTL	**Signal Detect #3:** Signal from the optical receiver for line #3 indicating signal presence. Not used in STM-4/OC-12 mode. It is recommended to use this lead for LOS detection due to some fiber optic modules outputting noise during LOS.
LINERXSIGDET4	Y18	I	LVTTL	**Signal Detect #4:** Signal from the optical receiver for line #4 indicating signal presence. Not used in STM-4/OC-12 mode. It is recommended to use this lead for LOS detection due to some fiber optic modules outputting noise during LOS.
LINERXCLK1	AA19	O	LVCMOS 8mA	**Receive Divided Clock #1:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA1P/N. The clock rate is programmable to be either 19.44 or 77.76 MHz.
LINERXCLK2	AB21	O	LVCMOS 8mA	**Receive Divided Clock #2:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA2P/N. The clock rate is fixed to 19.44 MHz.
LINERXCLK3	W18	O	LVCMOS 8mA	**Receive Divided Clock #3:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA3P/N. The clock rate is fixed to 19.44 MHz.

Symbol	Lead No.	I/O/P	Type	Name/Function
LINERXCLK4	Y19	O	LVCMOS 8mA	**Receive Divided Clock #4:** Clock output derived from the clock recovered from the serial data stream on LINERXDATA4P/N. The clock rate is fixed to 19.44 MHz.
LINERXCAP	Y17		Analog	**Capacitor for the Receive Line & APS Clock Recovery:** Optional external capacitor. Do not install.

4.1.4 SDH/SONET Transmit Line Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
LINETXDATA1P LINETXDATA1N	AA10 Y10	O	LVPECL	**Serial SDH/SONET Transmit Data #1:** 622.08/155.52 Mbit/s bit-serial data to electro/optical transceivers. Only LINETXDATA1P/N is valid in STM-4/OC-12 mode.
LINETXDATA2P LINETXDATA2N	AA11 Y11	O	LVPECL	**Serial SDH/SONET Transmit Data #2:** 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid in STM-4/OC-12 mode.
LINETXDATA3P LINETXDATA3N	Y12 AA12	O	LVPECL	**Serial SDH/SONET Transmit Data #3:** 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid in STM-4/OC-12 mode.
LINETXDATA4P LINETXDATA4N	Y13 AA13	O	LVPECL	**Serial SDH/SONET Transmit Data #4:** 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid in STM-4/OC-12 mode.
LINETXCLK	Y7	O	LVCMOS 8mA	**Transmit Divided Clock:** Clock output derived from the synthesized transmit lock. The clock rate is programmable to be either 19.44 MHz or 77.76 MHz.
LINETXCAP	AB14		Analog	**Capacitor for the Transmit Line & APS Clock Synthesizer:** Optional external capacitor. Advised capacitor value: **STM-1/OC-3 application**: External Timing: N/A; Line/Loop - Timing: 1.0 µF **STM-4/OC-12 application**: External Timing: N/A; Line/Loop - Timing: 1.0 µF

4.1.5 Receive APS Port

Symbol	Lead No.	I/O/P	Type	Name/Function
APSRXDATAP APSRXDATAN	W9 Y8	I	LVDS	**Serial APS Port Receive Data:** 622.08 Mbit/s bit-serial data from mate PHAST-12P.
APSRXCLK	AA6	O	LVCMOS 8mA	**Receive Divided APS Port Clock:** Clock output derived from the clock recovered from the serial APS port data stream on APSRXDATAP/N. The clock rate is programmable to be either 19.44 or 77.76 MHz.

4.1.6 Transmit APS Port

Symbol	Lead No.	I/O/P	Type	Name/Function
APSTXDATAP APSTXDATAN	AA7 AB6	O	LVDS	**Serial APS Port Transmit Data:** 622.08 Mbit/s bit-serial data to mate PHAST-12P.

4.1.7 Clock/Timing Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
REFTXCLK1	AA20	I	LVTTL	**Transmit Reference Clock #1:** Reference clock for the transmit clock synthesizer. The clock rate is programmable to be either 19.44 or 77.76 MHz. The frequency tolerance for this clock is ± 20 ppm. The maximum allowed jitter on this clock should be confined to the same limits as indicated below for the REFTXCLK2P/ REFTXCLK2N leads.
REFTXCLK2P REFTXCLK2N	AB9 AB8	I	LVPECL	**Transmit Reference Clock #2:** Reference clock for the transmit clock synthesizer. The clock rate is programmable to be 19.44, 77.76 or 155.52 MHz. A 622.08 MHz clock can be provided when the Tx PLL is bypassed. The frequency tolerance for this clock is ± 20 ppm. The maximum jitter on this clock should be confined to a bandwidth of 5 kHz - 5 MHz and to the values shown below depending on the selected frequency as indicated:
REFRXCLK	W8	I	LVTTL	**Receive Reference Clock:** Optional Reference clock for the receive clock and data recovery units. This clock is required for line/loop-time applications, when REFTXCLK1 and REFTXCLK2P/N are not present. The clock rate is programmable to be either 19.44 or 77.76 MHz. The frequency tolerance for this clock is ± 100 ppm.
REFONESECCLK	R1	I	LVTTL	**One Second Clock:** Optional one second reference for performance monitoring counters. This is a 1.0 Hz ± 32 ppm clock input which is asynchronous with other clock inputs/outputs, and has a minimum pulse width of 2 77.76 MHz clock cycles = 25.72 ns (because synchronized). If used, the one second counters are shadowed after detection of the rising edge of this input.

Applied Reference Clock Frequency (MHz)	Maximum Reference Clock Jitter			
	OC-3		OC-12	
	ps RMS	ps pp	ps RMS	ps pp
19.44	40	280	8	56
77.76	40	280	8	56
155.52	40	280	8	56
622.08	40	280	8	56

Symbol	Lead No.	I/O/P	Type	Name/Function
REFTXFS	R2	I	LVTTL	**Transmit Reference Frame Sync:** Optional 8 kHz reference frame sync pulse. If present, this input must be synchronous to LINETXCLK and shall be at least 1 77.76 MHz clock cycle wide = 12.86 ns. This input can be used to roughly align the transmitted SONET/SDH frame.
REFSYSFS	B21	O	LVCMOS 8mA	**System Reference Frame Sync:** 8 kHz reference frame sync pulse. This output has a pulse width of 1 77.76 MHz clock cycle (12.86 ns) and shall be synchronous to the LINETXCLK when this last one is not divided down to 19.44 MHz.
$\overline{\text{RESET}}$	A4	I	LVTTLp	**Hardware Reset (Active Low):** The use of this lead at power-up is mandatory. This lead is held low for at least 50 ns causing all registers in the device to be reset. Maintained low for 50 ns, this lead is set high just prior to using boundary scan interface.

4.1.8 Receive DCC Interfaces

Symbol	Lead No.	I/O/P	Type	Name/Function
DCCRXDATA1	V2	O	LVCMOS 4mA	**Receive DCC Data #1:** Bit-serial data from the TOH monitor of receive line interface #1 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCRXDATA2	Y1	O	LVCMOS 4mA	**Receive DCC Data #2:** Bit-serial data from the TOH monitor of receive line interface #2 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCRXDATA3	U4	O	LVCMOS 4mA	**Receive DCC Data #3:** Bit-serial data from the TOH monitor of receive line interface #3 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCRXDATA4	V3	O	LVCMOS 4mA	**Receive DCC Data #4:** Bit-serial data from the TOH monitor of receive line interface #4 to an external LAPD interface controller or similar device. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCRXCLK1	V1	O	LVCMOS 8mA	**Receive DCC Clock #1:** The DCCRXDATA1 signal is clocked out by the PHAST-12P on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA1, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA1, the frequency is 192 kHz.
DCCRXCLK2	W1	O	LVCMOS 8mA	**Receive DCC Clock #2:** The DCCRXDATA2 signal is clocked out by the PHAST-12P on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA2, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA2, the frequency is 192 kHz.
DCCRXCLK3	T4	O	LVCMOS 8mA	**Receive DCC Clock #3:** The DCCRXDATA3 signal is clocked out by the PHAST-12P on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA3, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA3, the frequency is 192 kHz.

Symbol	Lead No.	I/O/P	Type	Name/Function
DCCRXCLK4	U3	O	LVCMOS 8mA	**Receive DCC Clock #4:** The DCCRXDATA4 signal is clocked out by the PHAST-12P on positive transitions of this clock. If MS/Line DCC is selected for DCCRXDATA4, the frequency is 576 kHz, if RS/Section DCC is selected for DCCRXDATA4, the frequency is 192 kHz.

4.1.9 Transmit DCC Interfaces

Symbol	Lead No.	I/O/P	Type	Name/Function
DCCTXDATA1	U1	I	LVTTL	**Transmit DCC Data #1:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #1. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXDATA2	R4	I	LVTTL	**Transmit DCC Data #2:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #2. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXDATA3	T3	I	LVTTL	**Transmit DCC Data #3:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #3. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXDATA4	U2	I	LVTTL	**Transmit DCC Data #4:** Bit-serial data from an external LAPD interface controller or similar device to the TOH Generator of transmit line interface #4. This data can be optionally selected to provide D1-D3 (RS/Section DCC) or D4-D12 (MS/Line DCC).
DCCTXCLK1	T1	O	LVCMOS 8mA	**Transmit DCC Clock #1:** The DCCTXDATA1 signal is clocked into the PHAST-12P on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA1, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA1, the frequency is 192 kHz.
DCCTXCLK2	P4	O	LVCMOS 8mA	**Transmit DCC Clock #2:** The DCCTXDATA2 signal is clocked into the PHAST-12P on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA2, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA2, the frequency is 192 kHz.
DCCTXCLK3	R3	O	LVCMOS 8mA	**Transmit DCC Clock #3:** The DCCTXDATA3 signal is clocked into the PHAST-12P on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA3, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA3, the frequency is 192 kHz.

Symbol	Lead No.	I/O/P	Type	Name/Function
DCCTXCLK4	T2	O	LVCMOS 8mA	**Transmit DCC Clock #4:** The DCCTXDATA4 signal is clocked into the PHAST-12P on negative transitions of this clock. If MS/Line DCC is selected for DCCTXDATA4, the frequency is 576 kHz, if RS/Section DCC is selected for DCCTXDATA4, the frequency is 192 kHz.

4.1.10 Transmit UTOPIA Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
PPUTTXCLK	C17	I	LVTTL	**Transmit UTOPIA Clock:** This clock is used for the transmit UTOPIA interface. The data and control signals are transferred on the rising edge of this clock. Maximum clock frequency is 50 MHz. **UTOPIA Standard notation: TxClk**
PPUTTXADDR4 PPUTTXADDR3 PPUTTXADDR2 PPUTTXADDR1 PPUTTXADDR0	D15 A17 B16 C15 D14	I	LVTTL	**Transmit PHY Address Bus:** In multi-PHY mode, these leads indicate the address of the PHY being selected and polled. Note that the null-PHY address is not responded to. In single-PHY mode, this address is not used and these leads must be tied to VSS. **UTOPIA Standard notation: TxAddr[4:0]**
PPUTTXDATA15 PPUTTXDATA14 PPUTTXDATA13 PPUTTXDATA12 PPUTTXDATA11 PPUTTXDATA10 PPUTTXDATA09 PPUTTXDATA08 PPUTTXDATA07 PPUTTXDATA06 PPUTTXDATA05 PPUTTXDATA04 PPUTTXDATA03 PPUTTXDATA02 PPUTTXDATA01 PPUTTXDATA00	E20 D21 B22 E19 D20 C21 C20 B20 C19 D18 A21 B19 C18 D17 A20 B18	I	LVTTL	**Transmit Cell Data Bus:** Data input, valid when $\overline{\text{PPUTTXENB}}$ is asserted low. **UTOPIA Standard notation: TxData[15:0]**
PPUTTXPRTY	D22	I	LVTTL	**Transmit Bus Parity:** Odd or even parity over data, or data and control signals. Evaluated only when $\overline{\text{PPUTTXENB}}$ is asserted low. **UTOPIA Standard notation: TxPrty**
PPUTTXSOPC	F20	I	LVTTL	**Transmit Start of Cell:** Indicates the start of cell. Valid only when $\overline{\text{PPUTTXENB}}$ is asserted low. **UTOPIA Standard notation: TxSOC**
$\overline{\text{PPUTTXENB}}$	D16	I	LVTTL	**Transmit Write Enable (Active Low):** Used along with PPUTTXADDR to initiate writes to the Tx FIFOs. Selection phase when $\overline{\text{PPUTTXENB}}$ is asserted high and transfer phase when $\overline{\text{PPUTTXENB}}$ is asserted low. During transfer phase PPUTTXADDR is used for polling. **UTOPIA Standard notation: TxEnb***

Symbol	Lead No.	I/O/P	Type	Name/Function
PPUTPTPACLAV3 PPUTPTPACLAV2 PPUTPTPACLAV1 PPUTPTPACLAV0	A19 A18 B17 C16	O(T)	LVCMOS 24mA	**Transmit Cell Available signals:** Tristateable signal indicating that a complete cell can be transferred. Both direct status and multiplexed status are supported. It is driven when a matching PHY address is presented on PPUTTXADDR. Tristated when either the null-PHY address or a not matching PHY address is presented on PPUTTXADDR. **UTOPIA Standard notation: TxClav[3:0]**
PPTXMOD PPTXEOP PPTXERR	G19 E21 C22	I	LVTTL	**Not Applicable Inputs:** These leads must be tied to VSS.
PPTXSPTA	F19	O(T)	LVCMOS 24mA	**Not Applicable Output:** This lead must be left unconnected.

Note: The Transmit UTOPIA Interface and the Transmit POS-PHY Interface share the same leads.

4.1.11 Receive UTOPIA Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
PPUTRXCLK	C11	I	LVTTL	**Receive UTOPIA Clock:** This clock is used for the receive UTOPIA interface. The data and control signals are transferred on the rising edge of this clock. Maximum clock frequency is 50 MHz. **UTOPIA Standard notation: RxClk**
PPUTRXADDR4 PPUTRXADDR3 PPUTRXADDR2 PPUTRXADDR1 PPUTRXADDR0	C12 B12 A12 A11 B11	I	LVTTL	**Receive PHY Address Bus:** In multi-PHY mode, these leads indicate the address of the PHY being selected and polled. Note that the null-PHY address is not responded to. In single-PHY mode, this address is not used and these leads must be tied to VSS. **UTOPIA Standard notation: RxAddr[4:0]**
PPUTRXDATA15 PPUTRXDATA14 PPUTRXDATA13 PPUTRXDATA12 PPUTRXDATA11 PPUTRXDATA10 PPUTRXDATA09 PPUTRXDATA08 PPUTRXDATA07 PPUTRXDATA06 PPUTRXDATA05 PPUTRXDATA04 PPUTRXDATA03 PPUTRXDATA02 PPUTRXDATA01 PPUTRXDATA00	A10 D11 B10 A9 C10 B9 D10 C9 A8 B8 A7 D9 C8 B7 A6 D8	O(T)	LVCMOS 16mA	**Receive Cell Data Bus:** Tristateable data bus, enabled only in cycles following those with PPUTRXENB asserted low. Tristated when PPUTRXENB is asserted high in the previous cycle or when either the null-PHY address or a not matching PHY address has been selected. **UTOPIA Standard notation: RxData[15:0]**
PPUTRXPRTY	A16	O(T)	LVCMOS 16mA	**Receive Bus Parity:** Odd or even parity over data, or over data and control signals. This is a tristateable output, asserted only in cycles following those with PPUTRXENB asserted low. Tristated when PPUTRXENB is asserted high in the previous cycle or when either the null-PHY address or a not matching PHY address has been selected. **UTOPIA Standard notation: RxPrty**
PPUTRXSOPC	A15	O(T)	LVCMOS 16mA	**Receive Start of Cell:** Indicates the start of each cell. This is a tristateable output, asserted only in cycles following those with PPUTRXENB asserted low. Tristated when PPUTRXENB is asserted high in the previous cycle or when either the null-PHY address or a not matching PHY address has been selected. **UTOPIA Standard notation: RxSOC**

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{PPUTRXENB}}$	A14	I	LVTTL	**Receive Read Enable (Active Low):** Used along with PPUTRXADDR to initiate reads from the Rx FIFOs. Selection phase when $\overline{\text{PPUTRXENB}}$ is asserted high and transfer phase when $\overline{\text{PPUTRXENB}}$ is asserted low. During transfer phase PPUTRXADDR is used for polling **UTOPIA Standard notation: RxEnb***
PPUTPRPACLAV3 PPUTPRPACLAV2 PPUTPRPACLAV1 PPUTPRPACLAV0	A13 D12 B13 C13	O(T)	LVCMOS 24mA	**Receive Cell Available signals:** Tristateable signal indicating that a complete cell is available for transfer. Both direct status and multiplexed status are supported. It is driven when a matching PHY address is presented on PPUTRXADDR. Tristated when either the null-PHY address or a not matching PHY address is presented on PPUTRXADDR. **UTOPIA Standard notation: RxClav[3:0]**
PPRXMOD PPRXEOP PPRXERR PPRXVAL	B15 C14 D13 B14	O(T)	LVCMOS 16mA	**Not Applicable Outputs:** These leads must be left unconnected.

Note: The Receive UTOPIA Interface and the Receive POS-PHY Interface share the same leads.

4.1.12 Transmit POS-PHY Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
PPUTTXCLK	C17	I	LVTTL	**Transmit POS-PHY Clock:** This clock is used for the Transmit POS-PHY interface. The data and control signals are transferred on the rising edge of this clock. Maximum clock frequency is 50 MHz. **POS-PHY Standard notation: TFCLK**
PPUTTXADDR4 PPUTTXADDR3 PPUTTXADDR2 PPUTTXADDR1 PPUTTXADDR0	D15 A17 B16 C15 D14	I	LVTTL	**Transmit PHY Address Bus:** In multi-PHY mode, these leads indicate the address of the PHY being selected and polled. Note that the null-PHY address is not responded to. In single-PHY mode, this address is not used and these leads must be tied to VSS. **POS-PHY Standard notation: TADR[4:0]**
PPUTTXDATA15 PPUTTXDATA14 PPUTTXDATA13 PPUTTXDATA12 PPUTTXDATA11 PPUTTXDATA10 PPUTTXDATA09 PPUTTXDATA08 PPUTTXDATA07 PPUTTXDATA06 PPUTTXDATA05 PPUTTXDATA04 PPUTTXDATA03 PPUTTXDATA02 PPUTTXDATA01 PPUTTXDATA00	E20 D21 B22 E19 D20 C21 C20 B20 C19 D18 A21 B19 C18 D17 A20 B18	I	LVTTL	**Transmit Packet Data Bus:** Data input, valid when PPUTTXENB is asserted low. **POS-PHY Standard notation: TDAT[15:0]**
PPUTTXPRTY	D22	I	LVTTL	**Transmit Bus Parity:** Odd or even parity over data, or data and control signals. Evaluated only when PPUTTXENB is asserted low. **POS-PHY Standard notation: TPRTY**
PPTXMOD	G19	I	LVTTL	**Transmit Word Modulo:** Indicates the size of the current word. When low, it indicates a 2-byte word. When high, it indicates a 1-byte word (present on the MSBs, LSBs are discarded). Evaluated only when PPTXEOP is asserted high (i.e., during the last word transfer of a packet). **POS-PHY Standard notation: TMOD**
PPUTTXSOPC	F20	I	LVTTL	**Transmit Start of Packet:** Indicates the first word of a packet. Valid only when PPUTTXENB is asserted low. **POS-PHY Standard notation: TSOP**

Symbol	Lead No.	I/O/P	Type	Name/Function
PPTXEOP	E21	I	LVTTL	**Transmit End of Packet:** Indicates the last word of a packet. Note: Can be asserted high together with PPUTTXSOPC, in case of a 1- or 2- byte packet. Valid only when PPUTTXENB is asserted low. **POS-PHY Standard notation: TEOP**
PPTXERR	C22	I	LVTTL	**Transmit Error:** Indicates the current packet is aborted: the PHAST-12P will insert the abort sequence. Evaluated only when PPTXEOP is asserted high (i.e., during the last word transfer of a packet). **POS-PHY Standard notation: TERR**
PPUTTXENB	D16	I	LVTTL	**Transmit Write Enable (Active Low):** Used along with PPUTTXADDR to initiate writes to the Tx FIFOs. Selection phase when PPUTTXENB is asserted high and transfer phase when PPUTTXENB is asserted low. During transfer phase PPUTTXADDR is used for polling. **POS-PHY Standard notation: TENB**
PPTXSTPA	F19	O(T)	LVCMOS 24mA	**Selected-PHY Transmit Packet Available:** High when a predefined minimum number of free words (SpaceAV_Threshold_Low) is available in the selected Tx FIFO, otherwise low. It always provides status info for the selected PHY, in order to avoid Tx FIFO overflows while polling is performed. Tristated when PPUTTXENB is asserted high in the previous cycle, or when either the null-PHY address or a not matching PHY address has been selected. **POS-PHY Standard notation: STPA**
PPUTPTPACLAV3 PPUTPTPACLAV2 PPUTPTPACLAV1 PPUTPTPACLAV0	A19 A18 B17 C16	O(T)	LVCMOS 24mA	**Polled-PHY Transmit Packet Available:** Transitions high when a predefined (user programmable) number of free words is available in the polled Tx FIFO. Once high, it indicates that the polled Tx FIFO has a predefined minimum number of free words (SpaceAV_Threshold_Low) available. Transitions low when the polled Tx FIFO has less than the predefined minimum number of free words available. It is driven when a matching PHY address is presented on PPUTTXADDR. Tristated when either the null-PHY address or a not matching PHY address is presented on PPUTTXADDR. **POS-PHY Standard notation: PTPA**

Note: The Transmit UTOPIA Interface and the Transmit POS-PHY Interface share the same leads.

4.1.13 Receive POS-PHY Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
PPUTRXCLK	C11	I	LVTTL	**Receive POS-PHY Clock:** This clock is used for the receive POS-PHY interface. The data and control signals are transferred on the rising edge of this clock. Maximum clock frequency is 50 MHz. **POS-PHY Standard notation: RFCLK**
PPUTRXADDR4 PPUTRXADDR3 PPUTRXADDR2 PPUTRXADDR1 PPUTRXADDR0	C12 B12 A12 A11 B11	I	LVTTL	**Receive PHY Address Bus:** In multi-PHY mode, these leads indicate the address of the PHY being selected and polled. Note that the null-PHY address is not responded to. In single-PHY mode, this address is not used and these leads must be tied to VSS. **POS-PHY Standard notation: RADR[4:0]**
PPUTRXDATA15 PPUTRXDATA14 PPUTRXDATA13 PPUTRXDATA12 PPUTRXDATA11 PPUTRXDATA10 PPUTRXDATA09 PPUTRXDATA08 PPUTRXDATA07 PPUTRXDATA06 PPUTRXDATA05 PPUTRXDATA04 PPUTRXDATA03 PPUTRXDATA02 PPUTRXDATA01 PPUTRXDATA00	A10 D11 B10 A9 C10 B9 D10 C9 A8 B8 A7 D9 C8 B7 A6 D8	O(T)	LVCMOS 16mA	**Receive Packet Data Bus:** Tristateable data bus, enabled only in cycles following those with PPUTRXENB asserted low. Tristated when PPUTRXENB is asserted high in the previous cycle or when either the null-PHY address or a not matching PHY address has been selected. **POS-PHY Standard notation: RDAT[15:0]**
PPUTRXPRTY	A16	O(T)	LVCMOS 16mA	**Receive Bus Parity:** Odd or even parity over data, or data and control signals**.** This is a tristateable output, asserted only in cycles following those with PPUTRXENB asserted low. Tristated when PPUTRXENB is asserted high in the previous cycle, or when either the null-PHY address or a not matching PHY address has been selected. **POS-PHY Standard notation: RPRTY**

Symbol	Lead No.	I/O/P	Type	Name/Function
PPRXMOD	B15	O(T)	LVCMOS 16mA	**Receive Word Modulo:** Indicates the size of the current word. When low, it indicates a 2-byte word. When high, it indicates a 1-byte word (present on the MSBs, LSBs are discarded). Can only be asserted when PPRXEOP is asserted high (i.e., during the last word transfer of a packet). Tristated when PPUTRXENB is asserted high in the previous cycle, or when either the null-PHY address or a not matching PHY address is has been selected. **POS-PHY Standard notation: RMOD**
PPUTRXSOPC	A15	O(T)	LVCMOS 16mA	**Receive Start of Packet:** Indicates the first word of a packet. Tristated when PPUTRXENB is asserted high in the previous cycle, or when either the null-PHY address or a not matching PHY address has been selected. **POS-PHY Standard notation: RSOP**
PPRXEOP	C14	O(T)	LVCMOS 16mA	**Receive End of Packet:** Indicates the last word of a packet. Note: Can be asserted high together with PPUTRXSOPC, in case of a 1- or 2- byte packet. Tristated when PPUTRXENB is asserted high in the previous cycle, or when either the null-PHY address or a not matching PHY address has been selected. **POS-PHY Standard notation: REOP**
PPRXERR	D13	O(T)	LVCMOS 16mA	**Receive Error:** Indicates the current packet is aborted and must be discarded by the Link Layer Device. Can only be asserted when PPRXEOP is asserted high (i.e., during the last word transfer of a packet). Conditions that cause PPRXERR to be asserted high are Rx FIFO overflow, abort sequence detection, FCS error, too short and too long frames. Tristated when PPUTRXENB is asserted high in the previous cycle, or when either the null-PHY address or a not matching PHY address has been selected. **POS-PHY Standard notation: RERR**
$\overline{\text{PPUTRXENB}}$	A14	I	LVTTL	**Receive Write Enable (Active Low):** Used along with PPUTRXADDR to initiate reads from the Rx FIFOs. Selection phase when $\overline{\text{PPUTRXENB}}$ is asserted high and transfer phase when $\overline{\text{PPUTRXENB}}$ is asserted low. During transfer phase PPUTRXADDR is used for polling. **POS-PHY Standard notation: RENB**

Symbol	Lead No.	I/O/P	Type	Name/Function
PPRXVAL	B14	O(T)	LVCMOS 16mA	**Receive Data Valid:** Indicates the validity of the received data signals. When high, PPUTRXDATA, PPUTRXSOPC, PPRXEOP, PPRXMOD, PPUTRXPRTY, PPRXERR are valid. When low, these signals are invalid and must be disregarded by the link layer device. Transitions low on an Rx FIFO empty condition or on an end of packet. No data will be removed from the Rx FIFO while PPRXVAL is asserted low. Once asserted low, PPRXVAL will remain asserted low until the current PHY has been deselected. PPRXVAL allows to monitor the selected PHY during a data transfer, while monitoring or polling other PHYs is done using PPUTPRPACLAV. Tristated when PPUTRXENB is asserted high in the previous cycle, or when either the null-PHY address or a not matching PHY address has been selected. **POS-PHY Standard notation: RVAL**
PPUTPRPACLAV3 PPUTPRPACLAV2 PPUTPRPACLAV1 PPUTPRPACLAV0	A13 D12 B13 C13	O(T)	LVCMOS 24mA	**Receive Polled-PHY Packet Available:** High when a predefined minimum number of words or a complete packet is available in the polled Rx FIFO, otherwise low. It is driven when a matching PHY address is presented on PPUTRXADDR. Tristated when either the null-PHY address or a not matching PHY address is presented on PPUTRXADDR. **POS-PHY Standard notation: PRPA**

Note: The Receive UTOPIA Interface and the Receive POS-PHY Interface share the same leads.

4.1.14 Receive Line Ring Port/Alarm Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
LRPRXCLK	T22	O	LVCMOS 4mA	**Receive Line Ring Port Clock:** The LRPRXFS and LRPRXDATA signals are clocked out on the rising edges of this clock. Its frequency is 19.44 MHz.
LRPRXFS	R21	O	LVCMOS 4mA	**Receive Line Ring Port Frame Sync:** An active high, one LRPRXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on LRPRXDATA.
LRPRXDATA	P19	O	LVCMOS 4mA	**Receive Line Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals.

4.1.15 Transmit Line Ring Port/Alarm Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
LRPTXCLK	P20	I	LVTTL	**Transmit Line Ring Port Clock:** The LRPTXFS and LRPTXDATA signals are clocked in on the rising edges of this clock. Its frequency is 19.44 MHz. When this lead is not connected to LRPRXCLK of a mate PHAST-12P device, it must be tied to VSS.
LRPTXFS	N19	I	LVTTL	**Transmit Line Ring Port Frame Sync:** An active high, one LRPTXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on LRPTXDATA. When this lead is not connected to LRPRXFS of a mate PHAST-12P device, it must be tied to VSS.
LRPTXDATA	R22	I	LVTTL	**Transmit Line Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals. When this lead is not connected to LRPRXDATA of a mate PHAST-12P device, it must be tied to VSS.

4.1.16 Receive High Order Path Ring Port/Alarm Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
PRPRXCLK	M19	O	LVCMOS 4mA	**Receive HO Ring Port Clock:** The PRPRXFS and PRPRXDATA signals are clocked out on the rising edges of this clock. Its frequency is 19.44 MHz.
PRPRXFS	N21	O	LVCMOS 4mA	**Receive HO Ring Port Frame Sync:** An active high, one PRPRXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on PRPRXDATA.
PRPRXDATA	N22	O	LVCMOS 4mA	**Receive HO Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals.

4.1.17 Transmit High Order Path Ring Port/Alarm Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
PRPTXCLK	P22	I	LVTTL	**Transmit HO Ring Port Clock:** The PRPTXFS and PRPTXDATA signals are clocked in on the rising edges of this clock. Its frequency is 19.44 MHz. When this lead is not connected to LRPRXCLK of a mate PHAST-12P device, it must be tied to VSS.
PRPTXFS	P21	I	LVTTL	**Transmit HO Ring Port Frame Sync:** An active high, one PRPTXCLK clock-cycle wide frame sync pulse that identifies the first bit in the data stream present on PRPTXDATA. When this lead is not connected to LRPRXFS of a mate PHAST-12P device, it must be tied to VSS.
PRPTXDATA	N20	I	LVTTL	**Transmit HO Ring Port Data:** A serial frame containing the remote information, REI and RDI, for the individual high order path signals. When this lead is not connected to PRPRXDATA of a mate PHAST-12P device, it must be tied to VSS.

4.1.18 Receive TOH Byte Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
TOHRXCLK	U19	O	LVCMOS 8mA	**Receive TOH Port Clock:** The TOHRXALE, TOHRXDLE, TOHRXADDR and TOHRXDATA signals are clocked out on the falling edges of this clock. Its frequency is 77.76 MHz.
TOHRXALE	V20	O	LVCMOS 8mA	**Receive TOH Port Address Latch Enable:** An active high, 10 TOHRXCLK clock-cycle wide pulse indicating that a valid address is present on TOHRXADDR.
TOHRXADDR	W21	O	LVCMOS 8mA	**Receive TOH Port Address:** The 10 consecutive states clocked out while TOHRXALE is high form the address of the subsequent TOH byte sent on the TOHRXDATA lead.
TOHRXDLE	V21	O	LVCMOS 8mA	**Receive TOH Port Data Latch Enable:** An active high, 8 TOHRXCLK clock-cycle wide pulse indicating that valid data is present on TOHRXDATA.
TOHRXDATA	Y22	O	LVCMOS 8mA	**Receive TOH Port Data:** The 8 consecutive states clocked out while TOHRXDLE is high form the value of the TOH byte addressed by TOHRXADDR.

4.1.19 Transmit TOH Byte Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
TOHTXCLK	W20	O	LVCMOS 16mA	**Transmit TOH Port Clock:** The TOHTXALE, TOHTXDLE and TOHTXADDR signals are clocked out on the falling edges of this clock. TOHTXDATA is clocked in on the rising edge of this clock. Its frequency is 77.76 MHz.
TOHTXALE	Y21	O	LVCMOS 8mA	**Transmit TOH Port Address Latch Enable:** An active high, 10 TOHTXCLK clock-cycle wide pulse indicating that a valid address is present on TOHTXADDR.
TOHTXADDR	AA21	O	LVCMOS 8mA	**Transmit TOH Port Address:** The 10 consecutive states clocked out while TOHTXALE is high form the address of the subsequent TOH byte requested on the TOHTXDATA lead.
TOHTXDLE	AA22	O	LVCMOS 8mA	**Transmit TOH Port Data Latch Enable:** An active high, 8 TOHTXCLK clock-cycle wide pulse indicating that valid data is present on TOHTXDATA.
TOHTXDATA	V19	I	LVTTL	**Transmit TOH Port Data:** The value of the TOH byte requested by TOHTXADDR is clocked in as the 8 consecutive states while TOHTXDLE is high. When the Transmit TOH Byte Interface is not used, this lead must be tied to VSS.

4.1.20 Receive High Order POH Byte Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
POHRXCLK	W22	O	LVCMOS 8mA	**Receive HO POH Port Clock:** The POHRXALE, POHRXDLE, POHRXADDR and POHRXDATA signals are clocked out on the falling edges of this clock. Its frequency is 77.76 MHz.
POHRXALE	V22	O	LVCMOS 8mA	**Receive HO POH Port Address Latch Enable:** An active high, 8 POHRXCLK clock-cycle wide pulse indicating that a valid address is present on POHRXADDR.
POHRXADDR	U21	O	LVCMOS 8mA	**Receive HO POH Port Address:** The 8 consecutive states clocked out while POHRXALE is high form the address of the subsequent High Order POH byte sent on the POHRXDATA lead.
POHRXDLE	U20	O	LVCMOS 8mA	**Receive HO POH Port Data Latch Enable:** An active high, 8 POHRXCLK clock-cycle wide pulse indicating that valid data is present on POHRXDATA.
POHRXDATA	T19	O	LVCMOS 8mA	**Receive HO POH Port Data:** The 8 consecutive states clocked out while POHRXDLE is high form the value of the High Order POH byte addressed by POHRXADDR.

4.1.21 Transmit High Order POH Byte Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
POHTXCLK	U22	O	LVCMOS 16mA	**Transmit HO POH Port Clock:** The POHTXALE, POHTXDLE and POHTXADDR signals are clocked out on the falling edges of this clock. POHTXDATA is clocked in on the rising edge of this clock. Its frequency is 77.76 MHz.
POHTXALE	T21	O	LVCMOS 8mA	**Transmit HO POH Port Address Latch Enable:** An active high, 8 POHTXCLK clock-cycle wide pulse indicating that a valid address is present on POHTXADDR.
POHTXADDR	R20	O	LVCMOS 8mA	**Transmit HO POH Port Address:** The 8 consecutive states clocked out while POHTXALE is high form the address of the subsequent High Order POH byte requested on the POHTXDATA lead.
POHTXDLE	T20	O	LVCMOS 8mA	**Transmit HO POH Port Data Latch Enable:** An active high, 8 POHTXCLK clock-cycle wide pulse indicating that valid data is present on POHTXDATA.
POHTXDATA	R19	I	LVTTL	**Transmit HO POH Port Data:** The value of the High Order POH byte requested by POHTXADDR is clocked in as the 8 consecutive states while POHTXDLE is high. When the Transmit High Order POH Byte Interface is not used, this lead must be tied to VSS.

4.1.22 General Purpose Input/Output

Symbol	Lead No.	I/O/P	Type	Name/Function
GPIN1	N1	I	LVTTL	**General Purpose Input #1:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.
GPIN2	M4	I	LVTTL	**General Purpose Input #2:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.
GPIN3	N2	I	LVTTL	**General Purpose Input #3:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.
GPIN4	N3	I	LVTTL	**General Purpose Input #4:** Active high input, e.g., to monitor the external electro/optical transceiver. This input is mapped in a read-only register for software access. When not used, this lead must be tied to VSS.
GPOUT1	P1	O	LVCMOS 4mA	**General Purpose Output #1:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.
GPOUT2	P2	O	LVCMOS 4mA	**General Purpose Output #2:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.
GPOUT3	N4	O	LVCMOS 4mA	**General Purpose Output #3:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.
GPOUT4	P3	O	LVCMOS 4mA	**General Purpose Output #4:** Active high output, e.g., to control the external electro/optical transceiver. This lead can be driven via a software writable register.

4.1.23 Host Processor Interface Selection

Symbol	Lead No.	I/O/P	Type	Name/Function
MPMODE1 MPMODE0	M2 M3	I	LVTTL	**Microprocessor Interface Select:** These leads select the Host Processor interface mode:
MPINTLEVEL	A2	I	LVTTLd	**Microprocessor Interrupt Level:** This lead selects the polarity of the MPINTR lead. If MPINTLEVEL is low, the interrupt on the MPINTR lead is active low, if MPINTLEVEL is high, the interrupt on the MPINTR lead is active high. This lead is evaluated in all modes (MPMODE[1:0] = '00', '01', '10' and '11').
MPACKLEVEL	D5	I	LVTTLd	**Microprocessor Acknowledge Level:** This lead selects the polarity of the MPACK lead. If MPACKLEVEL is low, an acknowledge is indicated by a falling edge of MPACK, if MPACKLEVEL is high, an acknowledge is indicated by a rising edge of MPACK. This lead is only evaluated in Generic Intel Mode (MPMODE[1:0] = '00') and Generic Motorola Mode (MPMODE[1:0] = '01'). This lead must be tied to VSS when MPMODE[1:0] = '10' or '11'.

MPMODE1	MPMODE0	Interface
0	0	Generic Intel
0	1	Generic Motorola
1	0	Motorola MPC860
1	1	Motorola MPC8260 Local Bus

Note: The Generic Intel, Generic Motorola, Motorola MPC860 and Motorola MPC8260 Local Bus - Host Processor interfaces are shared on the same leads.

4.1.24 Generic Intel - Host Processor Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Interface Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Intel notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12P for a read or write cycle. MPA13 is the most significant bit in the location's address. **Intel notation: A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12P and the host processor. MPD15 is the most significant bit. **Intel notation: D[ ]**
$\overline{\text{MPSEL}}$	K1	I	LVTTL	**PHAST-12P Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12P through a read or write cycle. **Intel notation: $\overline{\text{CS}}$**
$\overline{\text{MPTS}}$	L3	I	LVTTL	**Read Strobe (Active low):** This active low lead initiates a read transfer between the host processor and the PHAST-12P. **Intel notation: $\overline{\text{RD}}$**

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{MPWR}}$	L2	I	LVTTL	**Write Strobe (Active Low):** This active low lead initiates a write transfer between the host processor and the PHAST-12P. **Intel notation: $\overline{\text{WR}}$**
$\overline{\text{MPACK}}$	L1	O(T)	LVCMOS 24mA	**Ready:** For a write access, an active edge on this lead indicates that data is written to the addressed memory location. For a read access, an active edge on this lead indicates that the data to be read from the addressed memory location is available on the data bus. Active level depends on MPACKLEVEL. **Intel notation: $\overline{\text{RDY}}$**
$\overline{\text{MPINTR}}$	B3	O	LVCMOS 8mA	**Interrupt:** This lead signals an interrupt request to the host processor. Active level depends on MPINTLEVEL.

4.1.25 Generic Motorola - Host Processor Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12P for a read or write cycle. MPA13 is the most significant bit in the location's address. **Motorola notation: A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12P and the host processor. MPD15 is the most significant bit. **Motorola notation: D[ ]**
$\overline{\text{MPSEL}}$	K1	I	LVTTL	**PHAST-12P Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12P through a read or write cycle. **Motorola notation: $\overline{\text{CS}}$**
$\overline{\text{MPTS}}$	L3	I	LVTTL	**Data Strobe (Active Low):** This active low lead initiates a (read or write) transfer between the host processor and the PHAST-12P. **Motorola notation: $\overline{\text{DS}}$**

$\overline{\text{MPWR}}$	L2	I	LVTTL	**Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the PHAST-12P is a write transfer. **Motorola notation: R/W**
$\overline{\text{MPACK}}$	L1	O(T)	LVCMOS 24mA	**Data Transfer Acknowledge:** For a write access, an active edge on this lead indicates that data is written to the addressed memory location. For a read access, an active edge on this lead indicates that the data to be read from the addressed memory location is available on the data bus. Active level depends on MPACKLEVEL. **Motorola notation: DSACK**
$\overline{\text{MPINTR}}$	B3	O	LVCMOS 8mA	**Interrupt Request:** This lead signals an interrupt request to the host processor. Active level depends on MPINTLEVEL.

4.1.26 Motorola MPC860 - Host Processor Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola MPC860 notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12P for a read or write cycle. MPA13 is the most significant bit in the location's address. **Motorola MPC860 notation: A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12P and the host processor. MPD15 is the most significant bit. **Motorola MPC860 notation: D[ ]**
$\overline{\text{MPSEL}}$	K1	I	LVTTL	**PHAST-12P Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12P through a read or write cycle. **Motorola MPC860 notation: $\overline{\text{CS}}$**
$\overline{\text{MPTS}}$	L3	I	LVTTL	**Transfer Start (Active Low):** This active low lead initiates a (read or write) transfer between the host processor and the PHAST-12P. It is active low only during the first cycle of the access. **Motorola MPC860 notation: $\overline{\text{TS}}$**

$\overline{\text{MPWR}}$	L2	I	LVTTL	**Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the PHAST-12P is a write transfer. **Motorola MPC860 notation: RD/WR**
$\overline{\text{MPACK}}$	L1	O(T)	LVCMOS 24mA	**Transfer Acknowledge (Active Low):** This active low lead is used to acknowledge a host processor access. It is synchronous to the MPCLK. To acknowledge an access, MPACK is asserted during 1 MPCLK cycle. For a write access, an acknowledge indicates that data is written to the addressed memory location. For a read access, an acknowledge indicates that the data to be read from the addressed memory location is available on the data bus. **Motorola MPC860 notation: $\overline{\text{TA}}$**
$\overline{\text{MPINTR}}$	B3	O	LVCMOS 8mA	**Interrupt:** This lead signals an interrupt request to the host processor. Active level depends on MPINTLEVEL. Note: MPC860 expects active low interrupt, requiring MPINTLEVEL to be low.

4.1.27 Motorola MPC8260 Local Bus - Host Processor Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
MPCLK	M1	I	LVTTL	**Microprocessor Clock:** This lead is the clock sourced by the microprocessor being interfaced to this device. Its max. frequency is 50 MHz. **Motorola MPC8260 Notation: CLK**
MPA13 MPA12 MPA11 MPA10 MPA09 MPA08 MPA07 MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00	B1 E4 E3 C2 D2 C1 F4 B2 E2 F3 G4 D1 E1 F2	I	LVTTL	**Local Address Bus:** These leads are the address bus used by the host processor for accessing the PHAST-12P for a read or write cycle. MPA13 is the most significant bit in the location's address. **Motorola MPC8260 Notation: L_A[ ]**
MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00	G3 H4 F1 G2 H3 J4 G1 H2 H1 J3 K4 J2 K3 J1 K2 L4	I/O(T)	LVTTL/ LVCMOS 8mA	**Local Data Bus:** These leads are the bidirectional data bus used for transferring data between the PHAST-12P and the host processor. MPD15 is the most significant bit. **Motorola MPC8260 Notation: LCL_D[ ]**
$\overline{\text{MPSEL}}$	K1	I	LVTTL	**PHAST-12P Chip Select (Active Low):** This active low lead enables data transfers between the host processor and the PHAST-12P through a read or write cycle. **Motorola MPC8260 notation: CS**
$\overline{\text{MPTS}}$	L3	I	LVTTL	**Not Applicable Input:** This lead must be tied to VSS.

$\overline{\text{MPWR}}$	L2	I	LVTTL	**Local Bus Read/Write (Active Low):** This active low lead indicates that the actual transfer between the host processor and the PHAST-12P is a write transfer. **Motorola MPC8260 notation: LWR**
$\overline{\text{MPACK}}$	L1	O(T)	LVCMOS 24mA	**Local Bus GPCM Transfer Acknowledge (Active Low):** This lead is used to acknowledge a host processor access. It is synchronous to the MPCLK. To acknowledge an access, MPACK is asserted during 1 MPCLK cycle and then de-asserted during 3 MPCLK cycles before going in tristate. For a write access, an acknowledge indicates that data is written to the addressed memory location. For a read access, an acknowledge indicates that the data to be read from the addressed memory location is available on the data bus. **Motorola MPC8260 notation: LGTA**
$\overline{\text{MPINTR}}$	B3	O	LVCMOS 8mA	**Interrupt Request (Active low):** This lead signals an interrupt request to the host processor. Note: MPC8260 Local Bus expects active low interrupt, requiring MPINTLEVEL to be low.

4.1.28 Boundary Scan

Symbol	Lead No.	I/O/P	Type	Name/Function
TCK	A3	I	LVTTL	**Test Boundary Scan Clock:** This signal is used to shift data into TDI on its rising edge and out of TDO on its falling edge. The maximum clock frequency is 10 MHz.
TDI	D6	I	LVTTLp	**Test Boundary Scan Data Input:** Serial test instructions and data are clocked into this lead on the rising edge of TCK. This lead has an internal pull-up resistor.
TDO	C5	O(T)	LVCMOS 4mA	**Test Boundary Scan Data Output:** Serial test instructions and data are clocked onto this lead on the falling edge of TCK. When inactive, this lead goes into a high impedance state.
TMS	B4	I	LVTTLp	**Test Boundary Scan Mode Select:** This input lead is sampled on the rising edge of TCK. It is used to place the Test Access Port controller into various states, as defined in [IEEE 1149.1]. This lead has an internal pull-up resistor.
$\overline{\text{TRS}}$	B5	I	LVTTLp	**Test Boundary Scan Reset:** An active low signal that asynchronously resets the Test Access Port controller. The reset must be present for a minimum of 250 ns. This lead has an internal pull-up resistor. This lead must be tied to VSS for normal operation.

4.1.29 SDH/SONET Receive BYPASS Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
BYPRXCLK	W5	I	LVTTL	**Receive Line Bypass Clock:** For TranSwitch testing purposes. This lead must be tied to VSS.
BYPRXSEQ	AA2	I	LVTTL	**Receive Line Bypass Sequence:** For TranSwitch testing purposes. This lead must be tied to VSS.
BYPRXDATA7 BYPRXDATA6 BYPRXDATA5 BYPRXDATA4 BYPRXDATA3 BYPRXDATA2 BYPRXDATA1 BYPRXDATA0	Y4 AA3 Y3 Y2 W3 V4 AA1 W2	I	LVTTL	**Receive Line Bypass Data:** For TranSwitch testing purposes. These leads must be tied to VSS.

4.1.30 SDH/SONET Transmit BYPASS Interface

Symbol	Lead No.	I/O/P	Type	Name/Function
BYPTXCLK	AB5	I	LVTTL	**Transmit Line Bypass Clock:** For TranSwitch testing purposes. This lead must be tied to VSS.
BYPTXC1	AB4	O	LVCMOS 8mA	**Transmit Line Bypass C1 Indication:** For TranSwitch testing purposes. This lead must be left unconnected.
BYPTXDATA7 BYPTXDATA6 BYPTXDATA5 BYPTXDATA4 BYPTXDATA3 BYPTXDATA2 BYPTXDATA1 BYPTXDATA0	W7 Y6 AA5 AB3 W6 Y5 AA4 AB2	O	LVCMOS 8mA	**Transmit Line Bypass Data:** For TranSwitch testing purposes. These leads must be left unconnected.

4.1.31 Test

Symbol	Lead No.	I/O/P	Type	Name/Function
DEVHIGHZ	C4	I	LVTTLd	**Device High-Z:** For TranSwitch testing purposes. All LVCMOS outputs and all bi-dirs are tristated when this lead is high. This lead must be tied to VSS.
TEST1	C3	I	LVTTLd	**TEST1:** For TranSwitch testing purposes. This lead must be tied to VSS.
PLLBYPASS	A5	I	LVTTLd	**PLL Bypass:** For TranSwitch testing purposes. This lead must be tied to VSS.
SCANEN	D7	I	LVTTLd	**Scan Enable:** For TranSwitch testing purposes. This lead must be tied to VSS.
SCANMODE	C6	I	LVTTLd	**Scan Mode:** For TranSwitch testing purposes. This lead must be tied to VSS.

5.0 SELECTED PARAMETER VALUES

5.1 ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	V_{DD1}	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	V_{DD2}	-0.3	3.9	V	Notes 1, 4
DC input voltage	VIN	-0.5	5.5	V	Notes 1, 4, 5
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft./min. linear airflow
Moisture Exposure Level	ME	5		Level	per IPC/JEDEC J-STD-020C
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per JEDEC JESD22-A114D.
4. Device core is 1.8V only.
5. All LVDS and LVPECL inputs, LINERXCAP and LINETXCAP are excluded.

5.2 THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		14.7		^{0}C/W	0 ft./min. linear airflow

5.3 POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
VDD18	1.71	1.8	1.89	V	
IDD18			591	mA	
VDD18RPA	1.71	1.8	1.89	V	
IDD18RPA			72	mA	
VDD18TPA	1.71	1.8	1.89	V	
IDD18TPA			42	mA	
VDD33	3.13	3.3	3.47	V	
IDD33			194	mA	
VDDA33LVPCDRV	3.13	3.3	3.47	V	
IDDA33LVPCDRV			130	mA	
VDDA33LVPCIO	3.13	3.3	3.47	V	
IDDA33LVPCIO			7	mA	
VREF	1.14	1.2	1.26	V	
IREF			10	uA	
VTERM	1.14	1.2	1.26	V	
ITERM			see text		
P_{TOTAL}			2.5	W	

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C. Maximum values are based on measurements made at maximum voltages at 85° C.
2. All four line interfaces are operational in STM-1/OC-3 mode, and the APS port is operational.

5.4 POWER SUPPLY SHARING, FILTERING AND OTHER REQUIREMENTS

VDD33 may be combined with other 3.3V card supplies.

VDDA33LVPCDRV and VDDA33LVPCIO may share a supply, but should each be filtered. VDDA33LVPCDRV must use the same supply as the Tx side of the optical transceiver(s) (also filtered), for LVPECL threshold tracking.

VREF should have an isolated 1.2V supply.

VTERM (optional) should have an isolated 1.2V supply, when used.

All VSS pins may be combined on a strong ground plane with appropriate decoupling.

The following power pins supply I/O ESD structures and must either lead other supplies or be simultaneous with other supplies: VDD33 and VDDA33LVPCIO.

Device inputs may not be driven until the core supplies are up.

The use of VREF is mandatory. It is the reference voltage for the four LVPECL Tx pads (LINETXDATA1P/N, LINETXDATA2P/N, LINETXDATA3P/N, LINETXDATA4P/N) and the LVDS Tx pad (APSTXDATAP/N). In addition, it is used to bias the Rx and Tx PLLs.

The use of VTERM is optional, and in fact not recommended: It serves as the termination voltage for the LVDS Rx pad (APSRXDATAP/N).

VTERM must only be supplied, when the potential difference between the grounds of the two PHAST-12P devices (connected using the APS port) is large and does not meet LVDS standard: [IEEE Std 1596.3-1996]. In this case, the VTERM current can get larger than 20mA. If the grounds are equal, no current will be drawn and VTERM is not needed (can be left floating).

When the APS port is not used, VTERM can be left floating as well.

VDD18 may be combined with other 1.8V card supplies, but should be each filtered.

VDDA18TPA supplies the Tx PLL / Clock Synthesis and Tx LVPECL analog supplies. VDDA18RPA supplies the Rx PLL / Clock Recovery and Rx LVPECL analog supplies. They are the most sensitive supplies in the device. Noise on these supplies result in deteriorated jitter performance at the Line side. The recommendation is to have separate 1.8V supplies for VDDA18TPA and VDDA18RPA, each one carefully filtered.The power supply noise requirement for both VDDA18TPA and VDDA18RPA is 20 mVpp max.

5.5 LVPECL I/O RECOMMENDATIONS:

LVPECL - Line Interfaces:

It is required to provide a pull-up and a pull-down resistor as close as possible to the LINERXDATAxP and LINERXDATAxN (x = 1...4) pins on the PHAST-12P:

- pull-up value (towards +3.3V) = 130 Ω for DC-coupling, 82 Ω for AC-coupling
- pull-down value (towards VSS) = 82 Ω for DC-coupling, 130 Ω for AC-coupling

It is required to provide a pull-up and a pull-down resistor at the LINETXDATAxP and LINETXDATAxN (x = 1...4) pins on the PHAST-12P:

- pull-up value (towards +3.3V) = 130 Ω for DC-coupling, 82 Ω for AC-coupling
- pull-down value (towards VSS) = 82 Ω for DC-coupling, 130 Ω for AC-coupling

The placement of these resistors should be near the PHAST-6P in AC coupled mode and near the optical transceiver in DC coupled mode.

Provide optional 0.1 μF series capacitors on all P and N lines between the PHAST-12P and each optical transceiver. This allows for both AC- and DC-coupling: 0 Ω resistors can be mounted in case of DC coupling.

At the optical transceiver side, one should carefully follow the recommendations in the data sheet of the optical transceiver. This should satisfy most vendors' data sheets:

- Provide pull-up and pull-down resistors as close as possible to the optical transceiver's Rx output, on both P and N (Usually, only pull-down resistors are required).
- Provide pull-up and pull-down resistors as close as possible to the optical transceiver's Tx input, on both P and N.
- Provide a resistor between P and N as close as possible to the optical transceiver's Tx input.
- Provide enough resistors in the schematic. Some of them may not be required, and can be treated as 'do not install'.

LVPECL - Tx Reference Clock:

It is required to provide a pull-up and a pull-down resistor as close as possible to the REFTXCLK2P & REFTXCLK2N pins on the PHAST-12P:

- pull-up value (towards +3.3V) = 130 Ω for DC-coupling, 82 Ω for AC-coupling
- pull-down value (towards VSS) = 82 Ω for DC-coupling, 130 Ω for AC-coupling

One should follow the recommendations in the data sheet of the device providing REFTXCLK2.

- Typically, pull-down resistors of approx. 150 Ω on both P and N are required, close to the outputs.
- Provide enough resistors in the schematic. Some of them may not be required, and can be treated as 'do not install'.

To achieve optimal jitter performance, it is recommended to use REFTXCLK2P/N (LVPECL), instead of the single-ended REFTXCLK1 (LVTTL).

LVPECL - PCB guidelines:

The differential pairs (P and N) will be routed together, have a controlled impedance of 50 Ω and be the same length. Make them as short as possible and in as straight a path as possible. Vias should be avoided if practicable.

LVPECL - Unused pins:

All unused LVPECL inputs can be left floating (no resistors required).

All unused LVPECL outputs can be left floating (no resistors required).

The following Figure 41 through Figure 44 summarize the recommendations above.

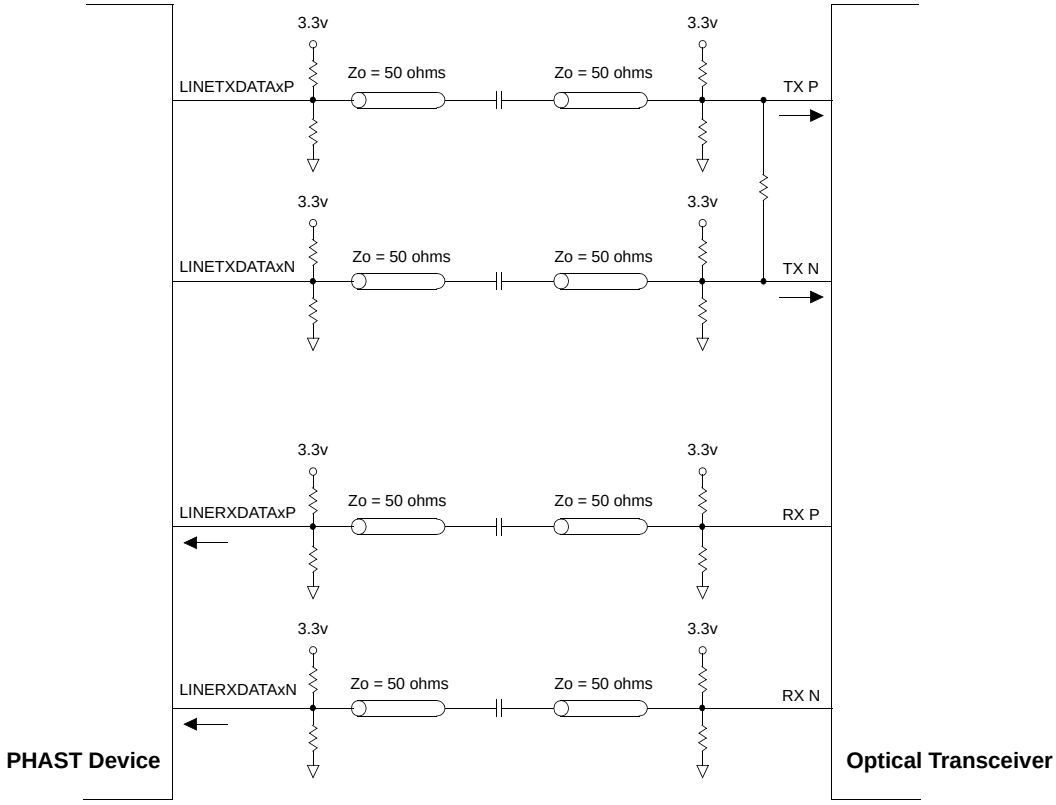


Figure 41. Multi-Purpose PCB Layout

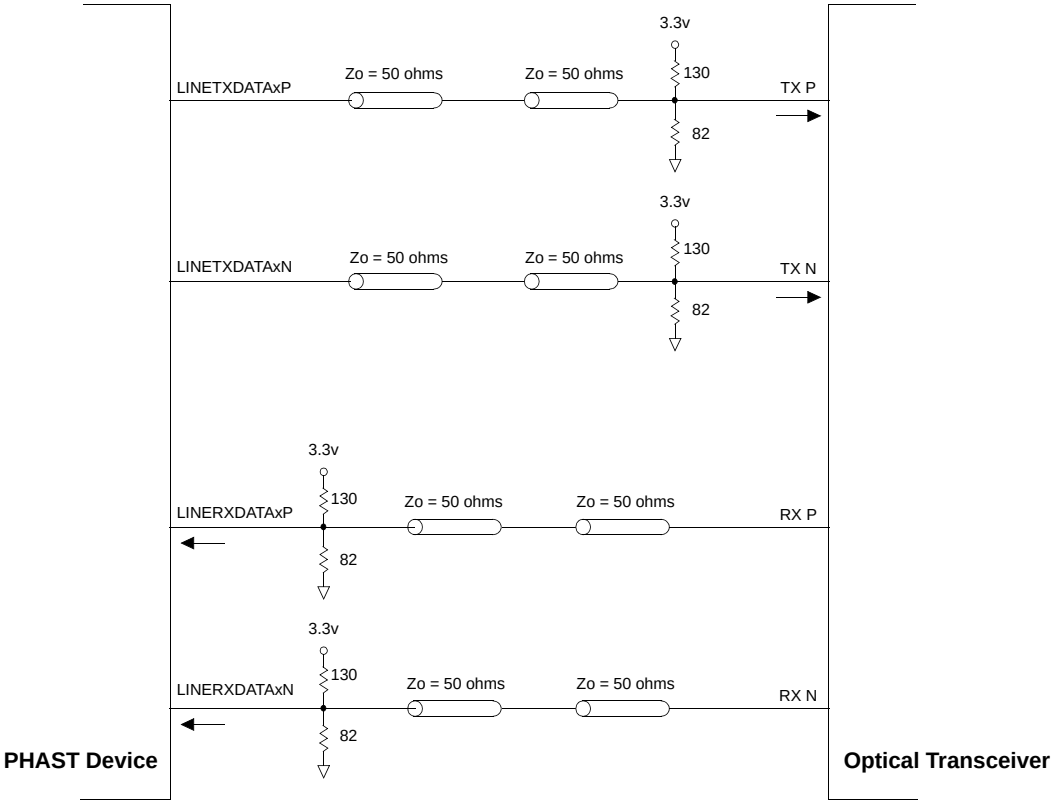
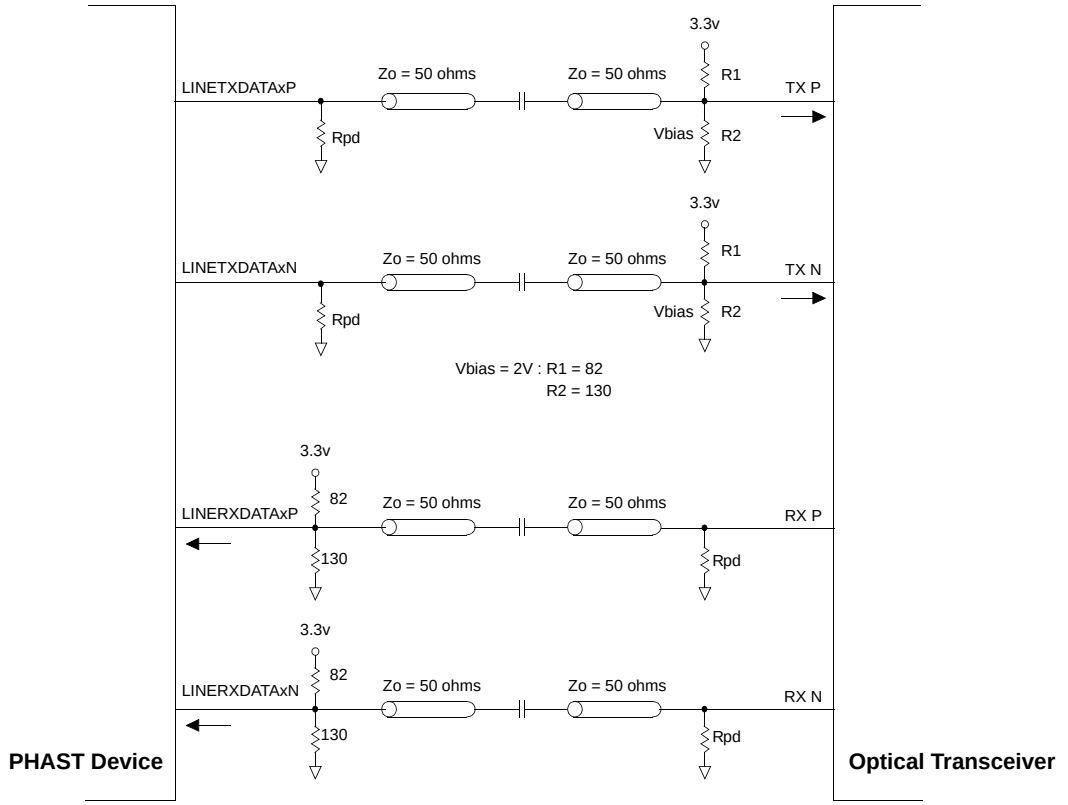
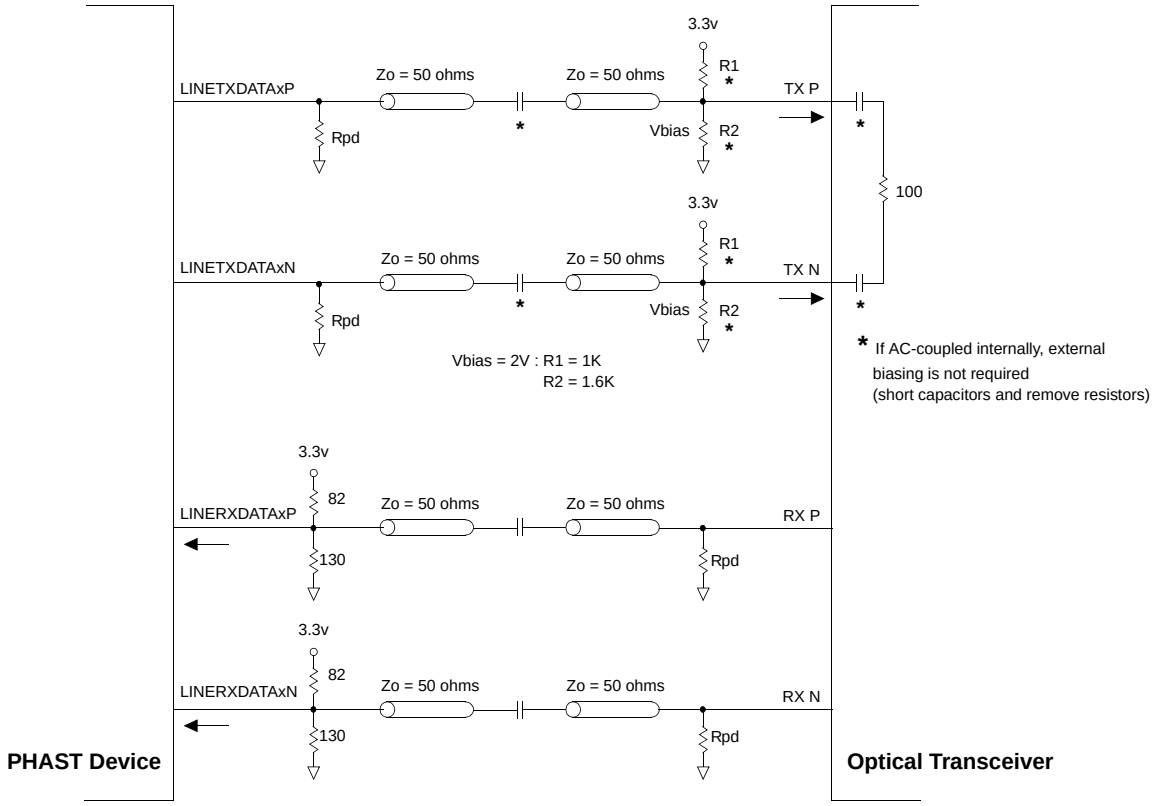


Figure 42. Typical LVPECL DC Termination



Note: Rpd = 180 - 250 ohms typical

Figure 43. Typical LVPECL AC Termination



Note: Rpd = 180 - 250 ohms typical

Figure 44. Transceiver with Internal Termination

5.6 LVDS I/O RECOMMENDATIONS:

LVDS - APS Port:

The LVDS I/O on the APS Port (APSRXDATAP/N, APSTXDATAP/N) is compliant to the LVDS standard: [IEEE Std 1596.3-1996].

The LVDS receiver (APSRXDATAP/N) has an integrated 100 Ω termination resistor between P and N. It is however recommended to provide a 100 Ω resistor on the board, between APSRXDATAP and APSRXDATAN, as close as possible to the PHAST-12P. This resistor will normally be treated as 'do not install'. See Figure 45.

Use DC coupling (no series capacitors).

LVDS - PCB, Connector and Cable guidelines:

The differential pairs (P and N) will be routed together, have a controlled impedance of 50 Ω and be the same length. Make them as short as possible and in as straight a path as possible. Vias should be avoided if practicable.

Use high quality connectors that are qualified for an LVDS signal at 622.08 Mbit/s (311.04 MHz).

The APS Port always operates at this rate. It cannot operate at a lower rate.

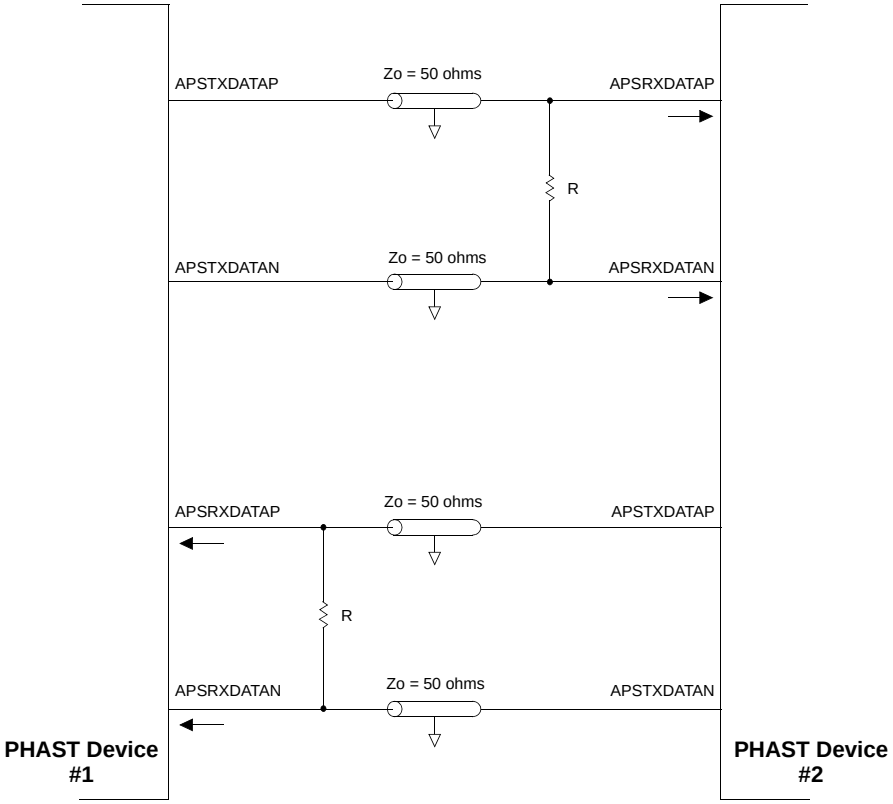
When a cable is used to interconnect two PHAST-12P devices using the APS Port, it is mandatory to use a 50 Ω cable. In a careful implementation, cable length can be up to 2 meter.

It is required to have a common ground between the two PHAST-12P devices that are connected using the APS Port.

LVDS - Unused pins:

Unused LVDS inputs can be left floating (no resistors required).

Unused LVDS outputs can be left floating (no resistors required).



Note: R is not installed for normal applications

Figure 45. LVDS PCB Layout

6.0 INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

Input/Output Parameters for LVPECL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{oH}	V_{DD} - 1.114		V_{DD} - 0.99	V	
V_{DD}-V_{oL}	V_{DD} - 1.769		V_{DD} - 1.576	V	
V_{oD}	0.586		0.750	V	
V_{oS}	V_{DD} - 1.44		V_{DD} - 1.283	V	
V_{iD}	0.2			V	
V_{iS}	1.525		2.4	V	

Note:

a. V_{DD} is VDDA33LVPCDRV.

b. V_{oD} = Tx output differential voltage

c. V_{oS} = Tx output offset voltage

d. V_{iD} = Rx input differential voltage

e. V_{iS} = Rx input offset voltage

Input/Output Parameters for LVDS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{oH}			1.475	V	
V_{oL}	0.925			V	
V_{oD}	0.25		0.4	V	
V_{oS}	1.125		1.275	V	
Ro	40		140	Ohm	
V_i	0		1.8	V	
V_{tH}	0.1			V	Differential Threshold, High
V_{tL}	-0.1			V	Differential Threshold, Low
RiN	80		120	Ohm	

Input Parameters for LVTTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

Input Parameters for LVTTLpu (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	-90		-25	µA	$V_{IN} = V_{SS}$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$
Input capacitance		5		pF	

Input Parameters for LVTTLpd (internal pull-down resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	28		85	µA	$V_{IN} = V_{DD33}$
Input leakage current	-10		10	µA	$V_{IN} = V_{SS}$
Input capacitance		5		pF	

Output Parameters for LVCMOS 24mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		30		pF	
V_{OH}	2.4			V	$V_{DD33} = 3.15$; $I_{OH} = -24$
V_{OL}			0.4	V	$V_{DD33} = 3.15$; $I_{OL} = 24$
I_{OL}		24		mA	
I_{OH}		-24		mA	
tRISE	1.17		2.25	ns	C_{LOAD} = 30 pF
tFALL	0.87		1.77	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

Output Parameters for LVCMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -8
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 8
I_{OL}	8			mA	
I_{OH}	-8			mA	
tRISE	1.78		3.38	ns	C_{LOAD} = 30 pF
tFALL	1.65		3.22	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

Output Parameters for LVCMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -4
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 4
I_{OL}	4			mA	
I_{OH}	-4			mA	
tRISE	2.97		5.54	ns	C_{LOAD} = 30 pF
tFALL	2.95		5.66	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input
Output capacitance		5		pF	

Output Parameters for LVCMOS 16mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -16
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 16
I_{OL}	16			mA	
I_{OH}	-16			mA	
tRISE	1.28		2.87	ns	C_{LOAD} = 30 pF
tFALL	1.04		2.65	ns	C_{LOAD} = 30 pF
Leakage tristate			±15	µA	0 to 3 V input

Input/Output Parameters For LVTTL/CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	V_{DD33} = 3.46
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33}= 3.14; I_{OH} = -8 mA
V_{OL}			0.4	V	V_{DD33}= 3.14; I_{OL} = 8 mA
I_{OL}	8.0			mA	
I_{OH}	-8.0			mA	

Input/Output Parameters for LVTTL Input and LV3CMOS Output 16mA (3.3V Volt Tolerant Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			±15	µA	0 to $_{3.3\ V\ input}$
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -16
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 16
I_{OL}	16			mA	
I_{OH}	-16			mA	
tRISE	1.76		2.85	ns	C_{LOAD} = 25 pF
tFALL	1.60		2.64	ns	C_{LOAD} = 25 pF

Input/Output Parameters for LVTTL Input and LV3CMOS Output 8mA (3.3V Volt Tolerant Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD33} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD33} \leq 3.45$
Input leakage current			±15	µA	0 to $_{3.3\ V\ input}$
Input capacitance		5		pF	
V_{OH}	2.4			V	V_{DD33} = 3.15; I_{OH} = -8
V_{OL}			0.4	V	V_{DD33} = 3.15; I_{OL} = 8
I_{OL}	8			mA	
I_{OH}	-8			mA	
tRISE	1.80		3.39	ns	C_{LOAD} = 25 pF
tFALL	1.78		3.36	ns	C_{LOAD} = 25 pF

7.0 TIMING CHARACTERISTICS

Detailed timing diagrams for the PHAST-12P device are illustrated in Figure 10 through Figure with values of the timing parameters tabulated below each waveform diagram. All outputs are measured with a maximum load capacitance of 50 pF unless otherwise stated. Timing parameters are measured at the voltage levels of $(V_{OH} + V_{OL})/2$ for output signals and $(V_{IH} + V_{IL})/2$ for input signals.

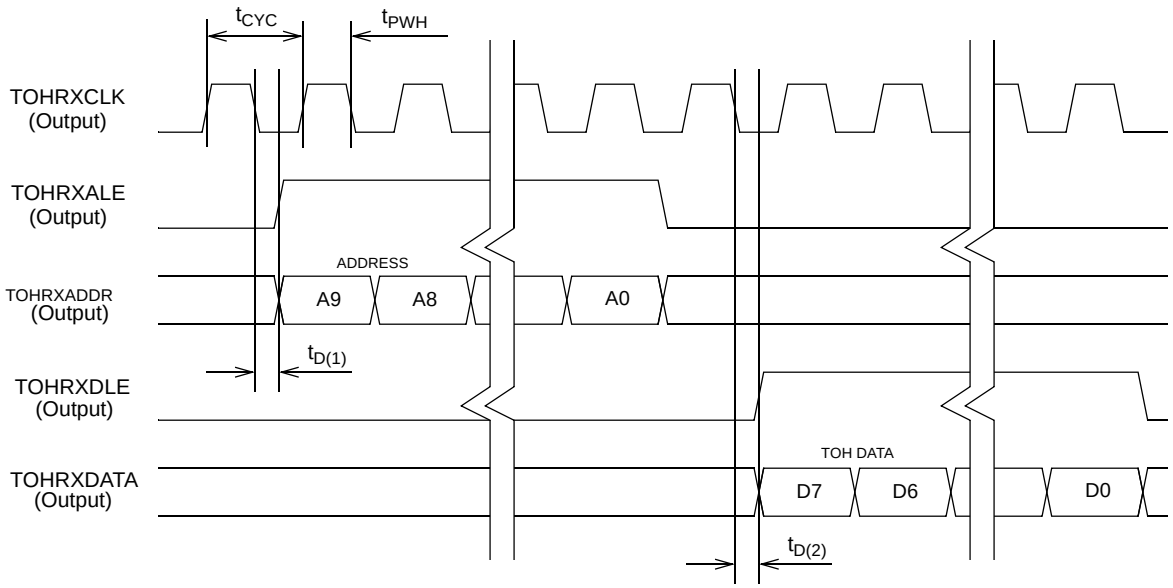


Figure 46. RX TOH Byte Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
TOHRXCLK clock period	t_{CYC}		12.86		ns
TOHRXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
TOHRXALE/TOHRXADDR out valid delay from TOHRXCLK↓	$t_{D(1)}$	1		4	ns
TOHRXDLE/TOHRXDATA out valid delay from TOHRXCLK↓	$t_{D(2)}$	1		4	ns

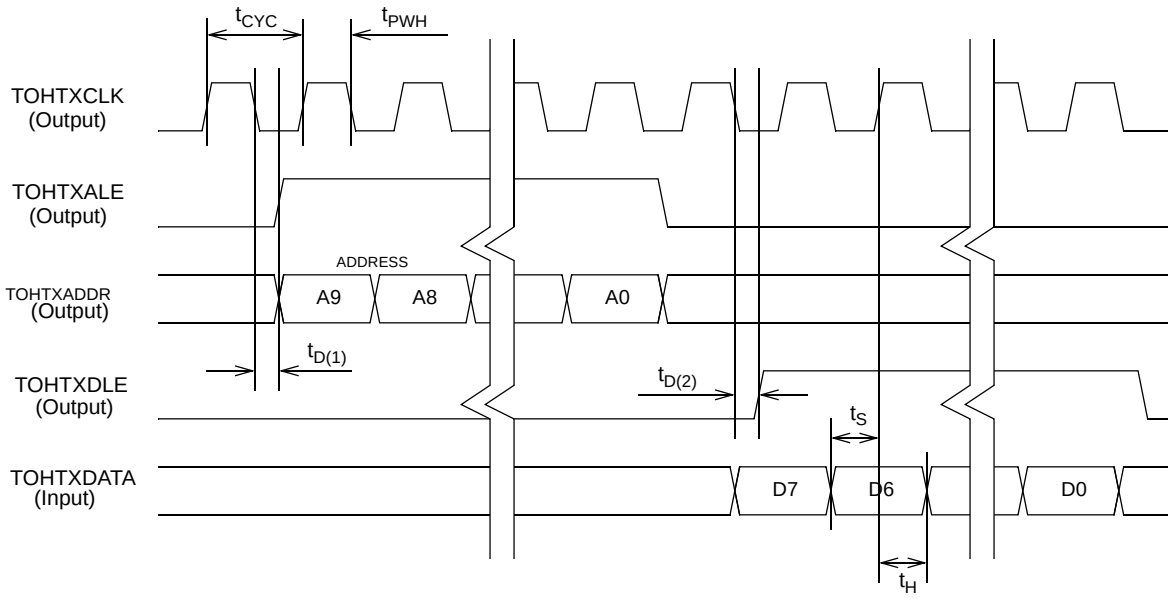


Figure 47. TX TOH Byte Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
TOHTXCLK clock period	t_{CYC}		12.86		ns
TOHTXCLK clock pulse width	t_{PWH}	40	50	60	%t_{CYC}
TOHTXALE/TOHTXADDR out valid delay from TOHTXCLK↓	$t_{D(1)}$	1		4	ns
TOHTXDLE out valid delay from TOHTXCLK↓	$t_{D(2)}$	1		4	ns
TOHTXDATA setup time before TOHTXCLK↑	t_S	6			ns
TOHTXDATA hold time after TOHTXCLK↑	t_H	0			ns

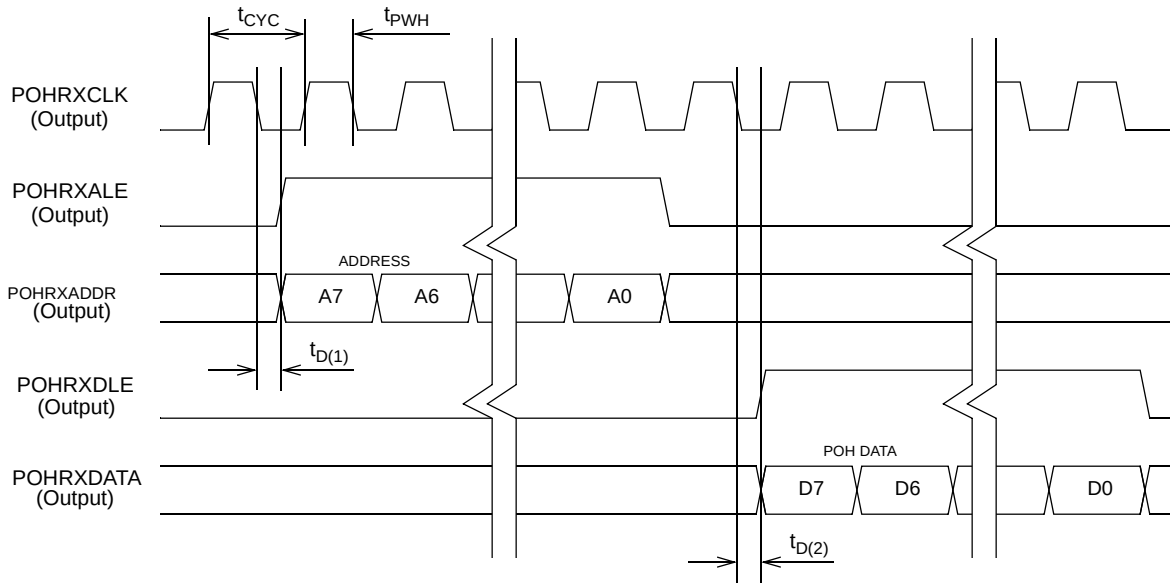


Figure 48. RX High Order POH Byte Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHRXCLK clock period	t_{CYC}		12.86		ns
POHRXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
POHRXALE/POHRXADDR out valid delay from POHRXCLK↓	$t_{D(1)}$	1		4	ns
POHRXDLE/POHRXDATA out valid delay from POHRXCLK↓	$t_{D(2)}$	1		4	ns

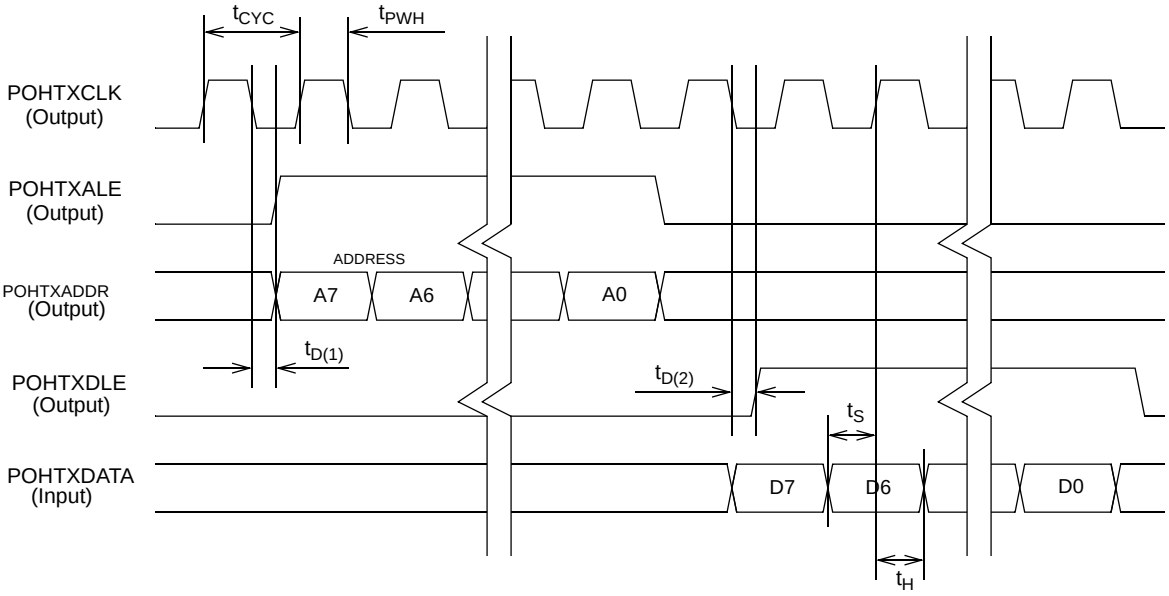


Figure 49. TX High Order POH Byte Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
POHTXCLK clock period	t_{CYC}		12.86		ns
POHTXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
POHTXALE/POHTXADDR out valid delay from POHTXCLK↓	$t_{D(1)}$	1		4	ns
POHTXDLE out valid delay from POHTXCLK↓	$t_{D(2)}$	1		4	ns
POHTXDATA setup time before POHTXCLK↑	t_S	6			ns
POHTXDATA hold time after POHTXCLK↑	t_H	0			ns

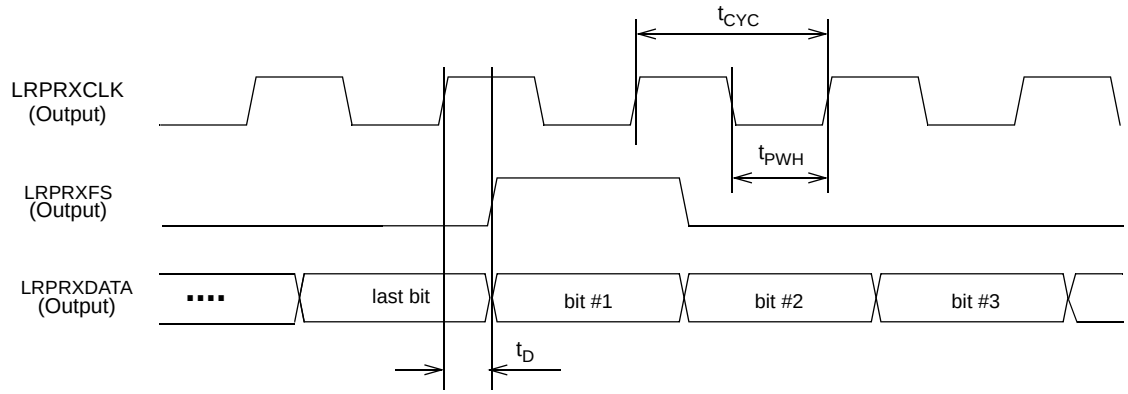


Figure 50. RX Line Ring Port Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
LRPRXCLK clock period	t_{CYC}		51.44		ns
LRPRXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
LRPRXFS/LRPRXDATA out valid delay from LRPRXCLK↑	t_D	1		6	ns

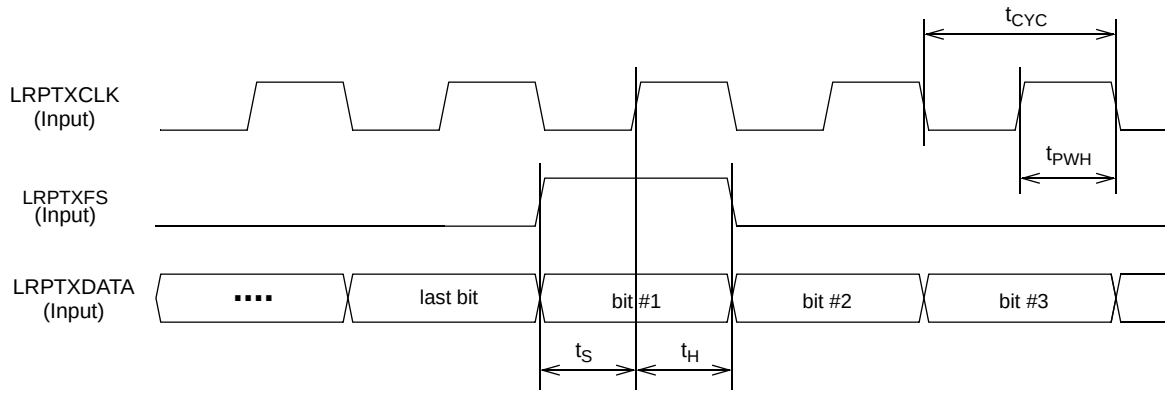


Figure 51. TX Line Ring Port Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
LRPTXCLK clock period	t_{CYC}		51.44		ns
LRPTXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
LRPTXFS/LRPTXDATA setup time before LRPTXCLK↑	t_S	30			ns
LRPTXFS/LRPTXDATA hold time after LRPTXCLK↑	t_H	0			ns

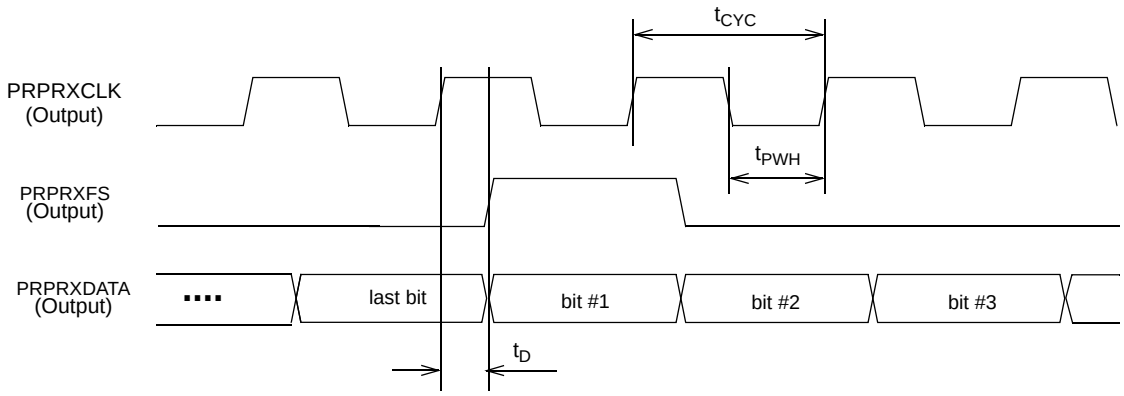


Figure 52. RX HO Path Alarm Indication Port Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
PRPRXCLK clock period	t_{CYC}		51.44		ns
PRPRXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
PRPRXFS/PRPRXDATA out valid delay from PRPRXCLK↑	t_D	1		6	ns

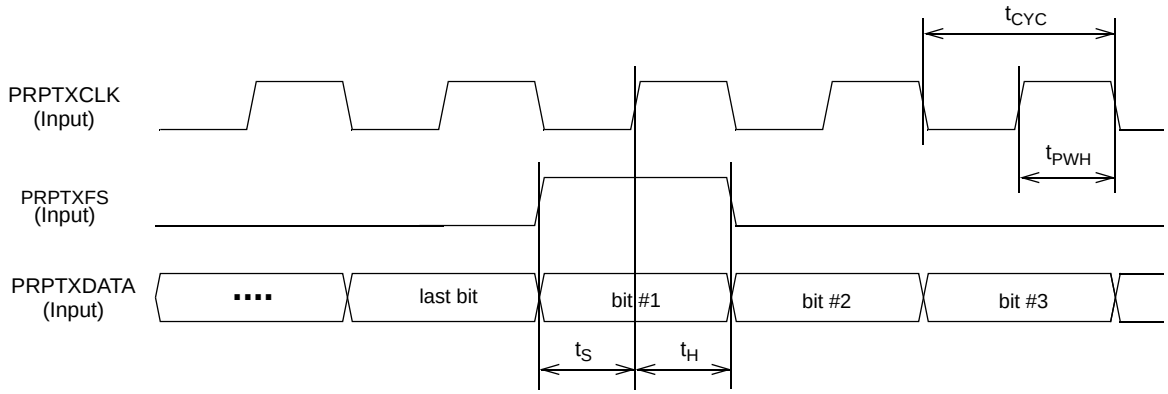


Figure 53. TX HO Path Alarm Indication Port Interface

50 pF Load

Parameter	Symbol	Min	Typ	Max	Unit
PRPTXCLK clock period	t_{CYC}		51.44		ns
PRPTXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
PRPTXFS/PRPTXDATA setup time before PRPTXCLK↑	t_S	35			ns
PRPTXFS/PRPTXDATA hold time after PRPTXCLK↑	t_H	0			ns

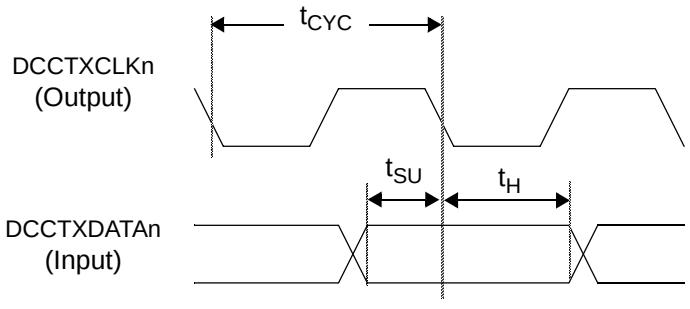


Figure 54. Transmit DCC Interface

Parameter	Symbol	Min	Typ	Max	Unit
DCCTXCLKn clock period (D1-D3)	t_{CYC1}		5.2		us
DCCTXCLKn clock period (D4-D12)	t_{CYC2}		1.7		us

Parameter	Symbol	Min	Typ	Max	Unit
DCCTXDATAn setup time to DCCTXCLKn↓	t_{SU}	14.9			ns
DCCTXDATAn hold time after DCCTXCLKn↓	t_H	-6.3			ns

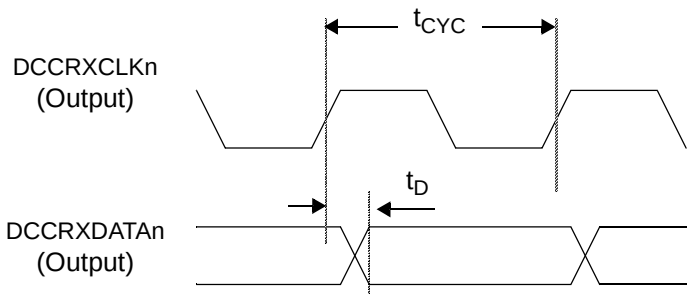


Figure 55. Receive DCC Interface

Parameter	Symbol	Min	Typ	Max	Unit
DCCRXCLKn clock period (D1-D3)	t_{CYC1}		5.2		us
DCCRXCLKn clock period (D4-D12)	t_{CYC2}		1.7		us
DCCRXDATAn delay after DCCRXCLKn↑	t_D	1.3		4.5	ns

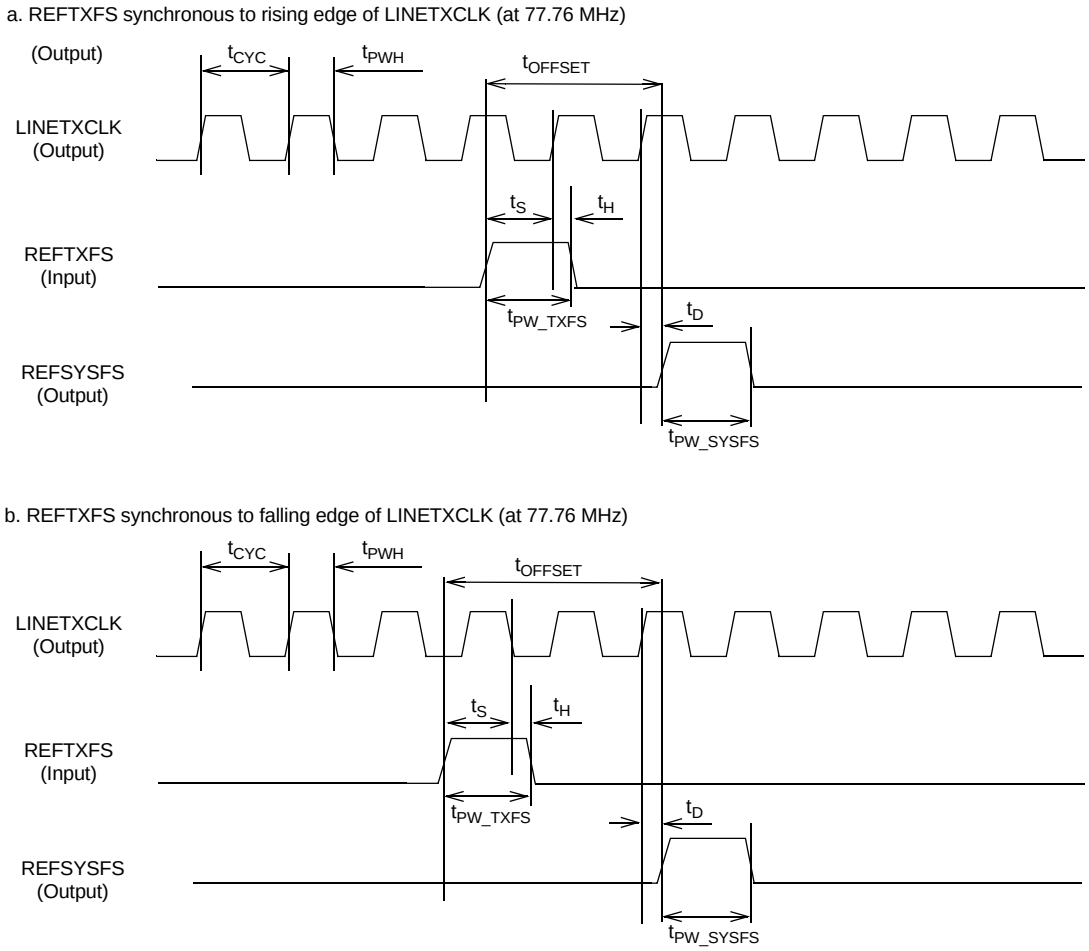


Figure 56. Relationship Between External Frame Reference Pulse (REFTXFS) and Generated Internal Frame Reference Pulse (REFSYSFS)

Parameter	Symbol	Min	Typ	Max	Unit
LINETXCLK	t_{CYC}		12.86		ns
LINETXCLK clock pulse width	t_{PWH}	40	50	60	$\%t_{CYC}$
REFTXFS pulse width	t_{PW_TXFS}	12.86			ns
REFSYSFS pulse width	t_{PW_SYSFS}		12.86	12.86	ns
REFTXFS synchronous to LINETXCLK↑ (at 77.76 MHz): offset between REFTXFS↑ and REFSYSFS↑	t_{OFFSET}		2		t_{CYC}
REFTXFS synchronous to LINETXCLK↓ (at 77.76 MHz): offset between REFTXFS↑ and REFSYSFS↑	t_{OFFSET}	1.5	2.5		t_{CYC}

Notes:

1. The relationship between the External Frame Reference pulse input (REFTXFS lead) and System Frame Reference Pulse is only useful when LINETXCLK is configured to 77.76 MHz. Because of this the period of LINETXCLK used in the timing diagrams above is 12.86 ns.
2. An additional offset of 0 to 9719 clock cycles (77.76 MHz clock) can be inserted between REFTXFS and REFSYSFS by configuring **ExtFramePulseOffset**, see "Locking on External Frame Reference Pulse" on page 65. The waveforms shown correspond to a delay of 0 clock cycles
3. The External Frame Reference Pulse input (REFTXFS lead) can be sampled at both positive or negative clock edge of LINETXCLK (when at 77.76 MHz). The sample edge is configured by setting **ExtFramePulseNegEdge**, see "Pointer Generator Common Configuration (T_RT_Common_Config)" on page 228. When REFTXFS is synchronous to the rising edge of LINETXCLK, the offset between REFTXFS and REFSYSFS is always equal to (2 + ExtFramePulseOffset) clock cycles (77.76 MHz clock), independent from the value of ExtFramePulseNegEdge. When REFTXFS is synchronous to the falling edge of LINETXCLK, the offset between REFTXFS and REFSYSFS is equal to (1.5 + ExtFramePulseOffset) clock cycles when ExtFramePulseNegEdge = 0, and (2.5 + ExtFramePulseOffset) clock cycles (77.76 MHz) when ExtFramePulseNegEdge = 1.

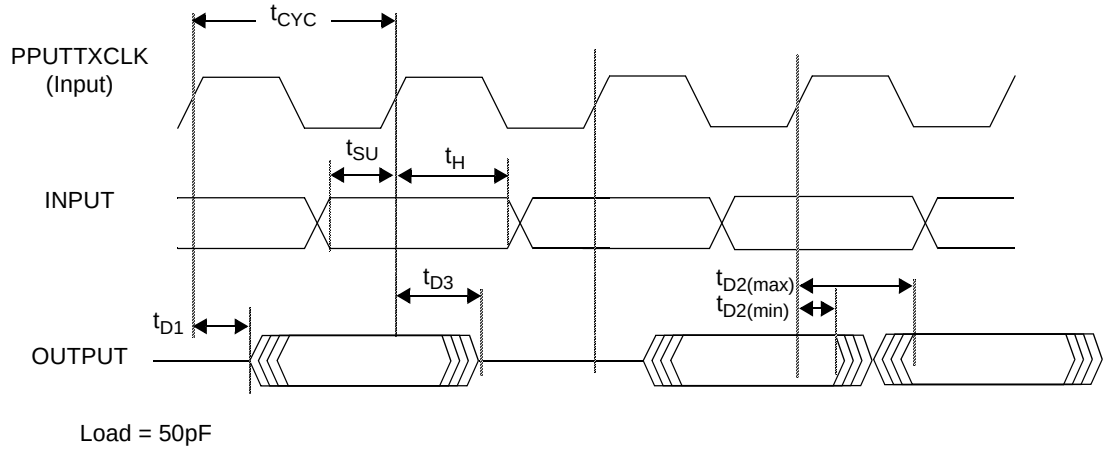


Figure 57. Transmit UTOPIA/POSPHY Level 2 Interface

Parameter	Symbol	Min	Typ	Max	Unit
PPUTTXCLK clock period	t_{CYC1}	20		40	ns
Input setup time to PPUTTXCLK↑	t_{SU}	4			ns
Input hold time after PPUTTXCLK↑	t_H	0			ns
Output driven from PPUTTXCLK↑	t_{D1}	4		11.5	ns
Output is valid from PPUTTXCLK↑	t_{D2}	3.5		12	ns
Output tristated from PPUTTXCLK↑	t_{D3}	2.5		10	ns

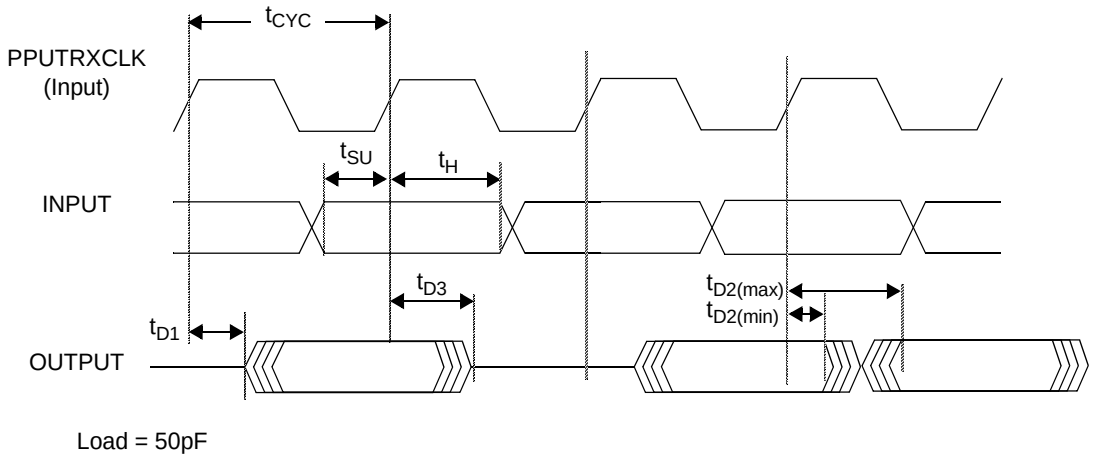
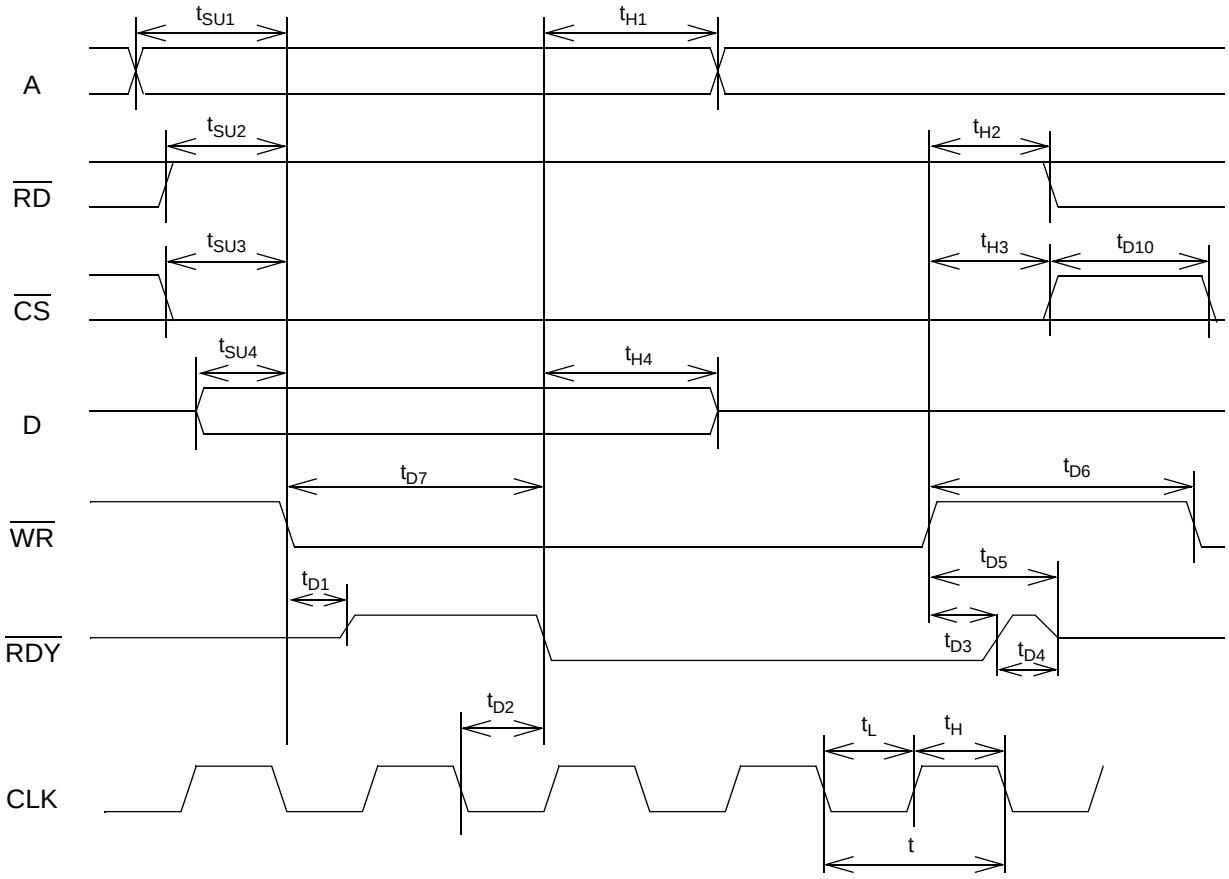


Figure 58. Receive UTOPIA/POSPHY Level 2 Interface

Parameter	Symbol	Min	Typ	Max	Unit
PPUTRXCLK clock period	t_{CYC1}	20		40	ns
Input setup time to PPUTRXCLK↑	t_{SU}	4			ns
Input hold time after PPUTRXCLK↑	t_H	0			ns
Output driven from PPUTTRCLK↑	t_{D1}	4		11.5	ns
Output is valid from PPUTRXCLK↑	t_{D2}	4		12	ns
Output tristated from PPUTR/XCLK↑	t_{D3}	2.5		10	ns



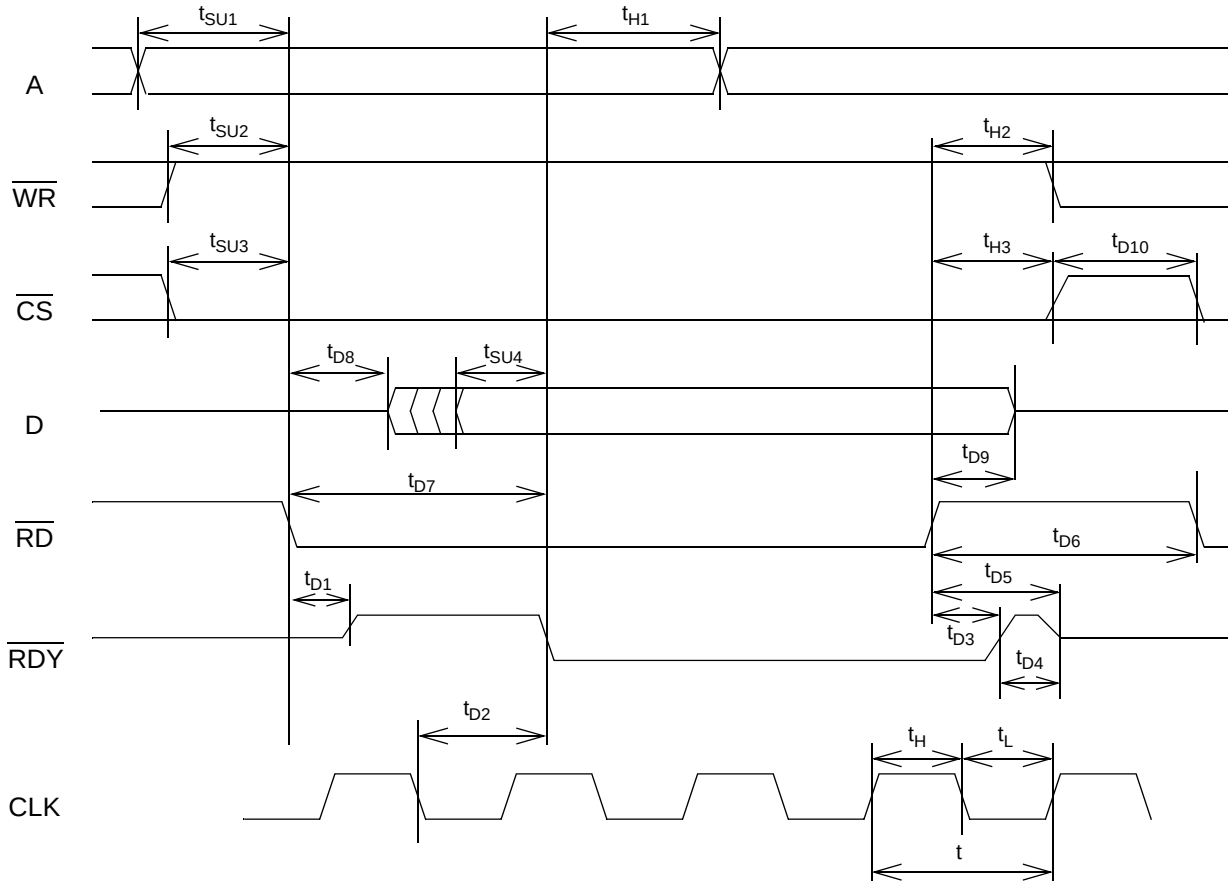
Note: MPACK ($\overline{RDY}$) is shown active low. This corresponds to MPACKLEVEL being tied low.

Figure 59. Microprocessor Interface: Generic Intel Mode Write Cycle[1]

1. See the Lead Description table on Generic Intel - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{WR}$
t_{SU2}[a]	0 ns	-	Setup time of $\overline{RD}$ to falling edge $\overline{WR}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{WR}$
t_{SU4}	-0.9t	-	Setup time of D to falling edge $\overline{WR}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{RDY}$
t_{H2}[c]	t	-	Hold time of $\overline{RD}$ to rising edge $\overline{WR}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{WR}$
t_{H4}	0 ns	-	Hold time of D to active edge $\overline{RDY}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{WR}$ to $\overline{RDY}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{RDY}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{WR}$ to inactive edge $\overline{RDY}$
t_{D4}	4 ns	-	Delay from $\overline{RDY}$ going inactive to $\overline{RDY}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{WR}$ to $\overline{RDY}$ going in tristate
t_{D6}	t	-	$\overline{WR}$ inactive pulse width
t_{D7}	363 ns	606 ns	Response latency
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. Only applies if a write access is preceded by a read access.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a write access is followed by a read access.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{WR}$ are defined. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals



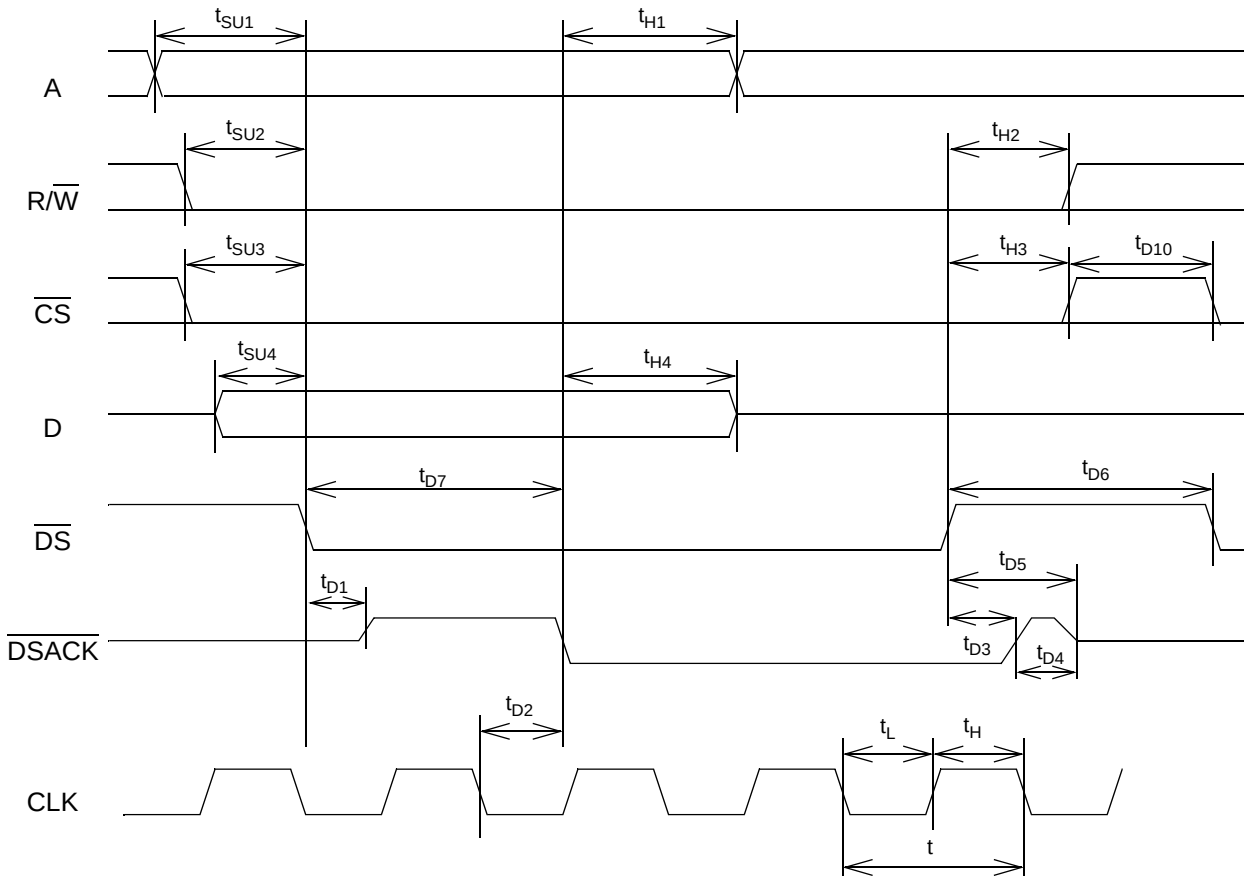
Note: MPACK ($\overline{RDY}$) is shown active low. This corresponds to MPACKLEVEL being tied low.

Figure 60. Microprocessor Interface: Generic Intel Mode Read Cycle[1]

1. See the Lead Description table on Generic Intel - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{RD}$
t_{SU2}[a]	0 ns	-	Setup time of $\overline{WR}$ to falling edge $\overline{RD}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{RD}$
t_{SU4}	0.7t	-	Setup time of D to active edge $\overline{RDY}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{RDY}$
t_{H2}[c]	t	-	Hold time of $\overline{WR}$ to rising edge $\overline{RD}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{RD}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{RD}$ to $\overline{RDY}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{RDY}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{RD}$ to inactive edge $\overline{RDY}$
t_{D4}	4 ns	-	Delay from $\overline{RDY}$ going inactive to $\overline{RDY}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{RD}$ to $\overline{RDY}$ going in tristate
t_{D6}	t	-	$\overline{RD}$ inactive pulse width
t_{D7}	363 ns	606 ns	Response latency
t_{D8}	0 ns	12 ns	Delay from falling edge $\overline{RD}$ to D driving
t_{D9}	0 ns	12 ns	Delay from rising edge $\overline{RD}$ to D going in tristate
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. $\overline{\text{Only}}$ applies if a read access is preceded by a write access.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a read access is followed by a write access.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{RD}$ are defined. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals



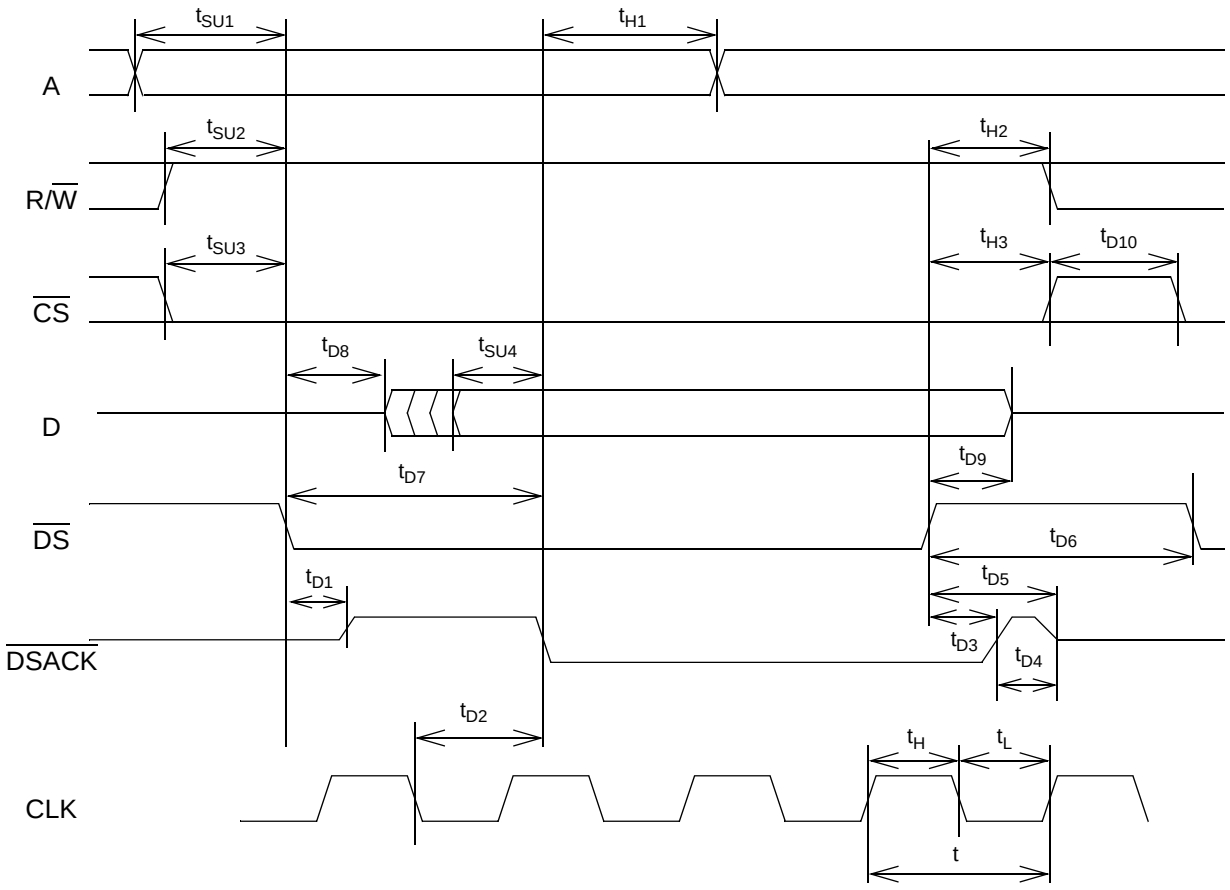
Note: MPACK ($\overline{\text{DSACK}}$) is shown active low. This corresponds to MPACKLEVEL being tied low.

Figure 61. Microprocessor Interface: Generic Motorola Mode Write Cycle[1]

1. See the Lead Description table on Generic Motorola - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{DS}$
t_{SU2}[a]	0 ns	-	Setup time of R/$\overline{W}$ to falling edge $\overline{DS}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{DS}$
t_{SU4}	-0.9t	-	Setup time of D to falling edge $\overline{DS}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{DSACK}$
t_{H2}[c]	0 ns	-	Hold time of R/$\overline{W}$ to rising edge $\overline{DS}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{DS}$
t_{H4}	0 ns	-	Hold time of D to active edge $\overline{DSACK}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{DS}$ to $\overline{DSACK}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{DSACK}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{DS}$ to inactive edge $\overline{DSACK}$
t_{D4}	4 ns	-	Delay from $\overline{DSACK}$ going inactive to $\overline{DSACK}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{DS}$ to $\overline{DSACK}$ going in tristate
t_{D6}	t	-	$\overline{DS}$ inactive pulse width
t_{D7}	363 ns	606 ns	Response latency
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. Only applies if a write access is preceded by a read access. R/$\overline{W}$ may stay low between 2 successive write accesses.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a write access is followed by a read access. R/$\overline{W}$ may stay low between 2 successive write accesses.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{DS}$ are defined, since no such relationship is defined in the MC68360 data sheet. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals



Note: MPACK (DSACK) is shown active low. This corresponds to MPACKLEVEL being tied low.

Figure 62. Microprocessor Interface: Generic Motorola Mode Read Cycle[1]

1. See the Lead Description table on Generic Motorola - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1}	-0.9t	-	Setup time of A to falling edge $\overline{DS}$
t_{SU2}[a]	0 ns	-	Setup time of R/$\overline{W}$ to falling edge $\overline{DS}$
t_{SU3}[b]	0 ns	-	Setup time of $\overline{CS}$ to falling edge $\overline{DS}$
t_{SU4}	0.7t	-	Setup time of D to active edge $\overline{DSACK}$
t_{H1}	0 ns	-	Hold time of A to active edge $\overline{DSACK}$
t_{H2}[c]	0 ns	-	Hold time of R/$\overline{W}$ to rising edge $\overline{DS}$
t_{H3}[b, d]	-	-	Hold time of $\overline{CS}$ to rising edge $\overline{DS}$
t_{D1}	0 ns	20 ns	Delay from falling edge $\overline{DS}$ to $\overline{DSACK}$ driving
t_{D2}	0 ns	8 ns	Delay from falling edge CLK to active edge $\overline{DSACK}$
t_{D3}	0 ns	7 ns	Delay from rising edge $\overline{DS}$ to inactive edge $\overline{DSACK}$
t_{D4}	4 ns	-	Delay from $\overline{DSACK}$ going inactive to $\overline{DSACK}$ going in tristate
t_{D5}	-	20 ns	Delay from rising edge $\overline{DS}$ to $\overline{DSACK}$ going in tristate
t_{D6}	t	-	$\overline{DS}$ inactive pulse width
t_{D7}	363 ns	606 ns	Response latency
t_{D8}	0 ns	12 ns	Delay from falling edge $\overline{DS}$ to D driving
t_{D9}	0 ns	12 ns	Delay from rising edge $\overline{DS}$ to D going in tristate
t_{D10}[e]	t	-	$\overline{CS}$ inactive pulse width

a. Only applies if a read access is preceded by a write access. R/$\overline{W}$ may stay high between 2 successive read accesses.
b. $\overline{CS}$ may stay low between 2 successive accesses to the same peripheral.
c. Only applies if a read access is followed by a write access. R/$\overline{W}$ may stay high between 2 successive read accesses.
d. No timing constraint between the rising edges of $\overline{CS}$ and $\overline{DS}$ are defined, since no such relationship is defined in the MC68360 data sheet. $\overline{CS}$ is only latched at the beginning of an access.
e. Between accesses to different peripherals

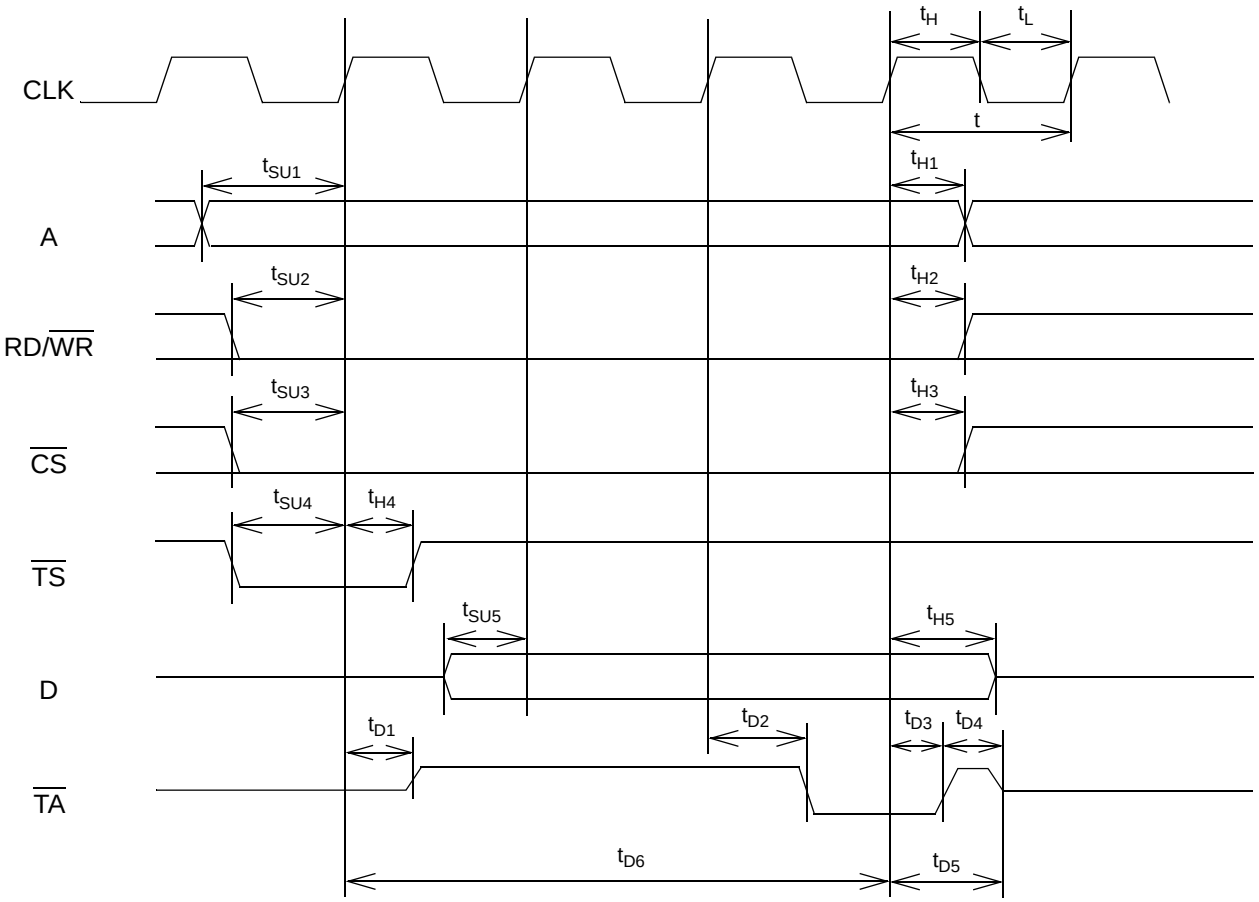


Figure 63. Microprocessor Interface: Motorola MPC860 Mode Write Cycle[1]

1. See the Lead Description table on Motorola MPC860 - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of RD/$\overline{WR}$ to rising edge CLK
t_{SU3} [a, c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{SU4}	6 ns	-	Setup time of falling edge $\overline{TS}$ to rising edge CLK
t_{SU5} [d]	0 ns	-	Setup time of D to rising edge CLK
t_{H1} [e]	0 ns	-	Hold time of A to rising edge CLK
t_{H2} [e, f]	0 ns	-	Hold time of RD/$\overline{WR}$ to rising edge CLK
t_{H3} [e, c]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{H4}	4 ns	-	Hold time of $\overline{TS}$ to rising edge CLK
t_{H5} [e]	0 ns	-	Hold time of D to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{TA}$ driving
t_{D2} [g]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{TA}$
t_{D3} [e]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{TA}$
t_{D4}	4 ns	-	Delay from $\overline{TA}$ going inactive to $\overline{TA}$ going in tristate
t_{D5} [e]	-	20 ns	Delay from rising edge CLK to $\overline{TA}$ going in tristate
t_{D6}	363 ns	606 ns	Maximum response latency

a. Timing is relative to the rising edge of CLK during which TS is asserted.
b. Only applies if a write access is preceded by a read access. RD/$\overline{WR}$ may stay low between 2 successive write accesses to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.
d. Timing is relative to next rising edge after the one during which $\overline{TS}$ is asserted.
e. Timing is relative to the rising edge of CLK during which $\overline{TA}$ is asserted.
f. Only applies if a write access is followed by a read access. RD/$\overline{WR}$ may stay low between 2 successive write accesses to the same peripheral.
g. Timing is relative to the rising edge before the one during which $\overline{TA}$ is asserted.

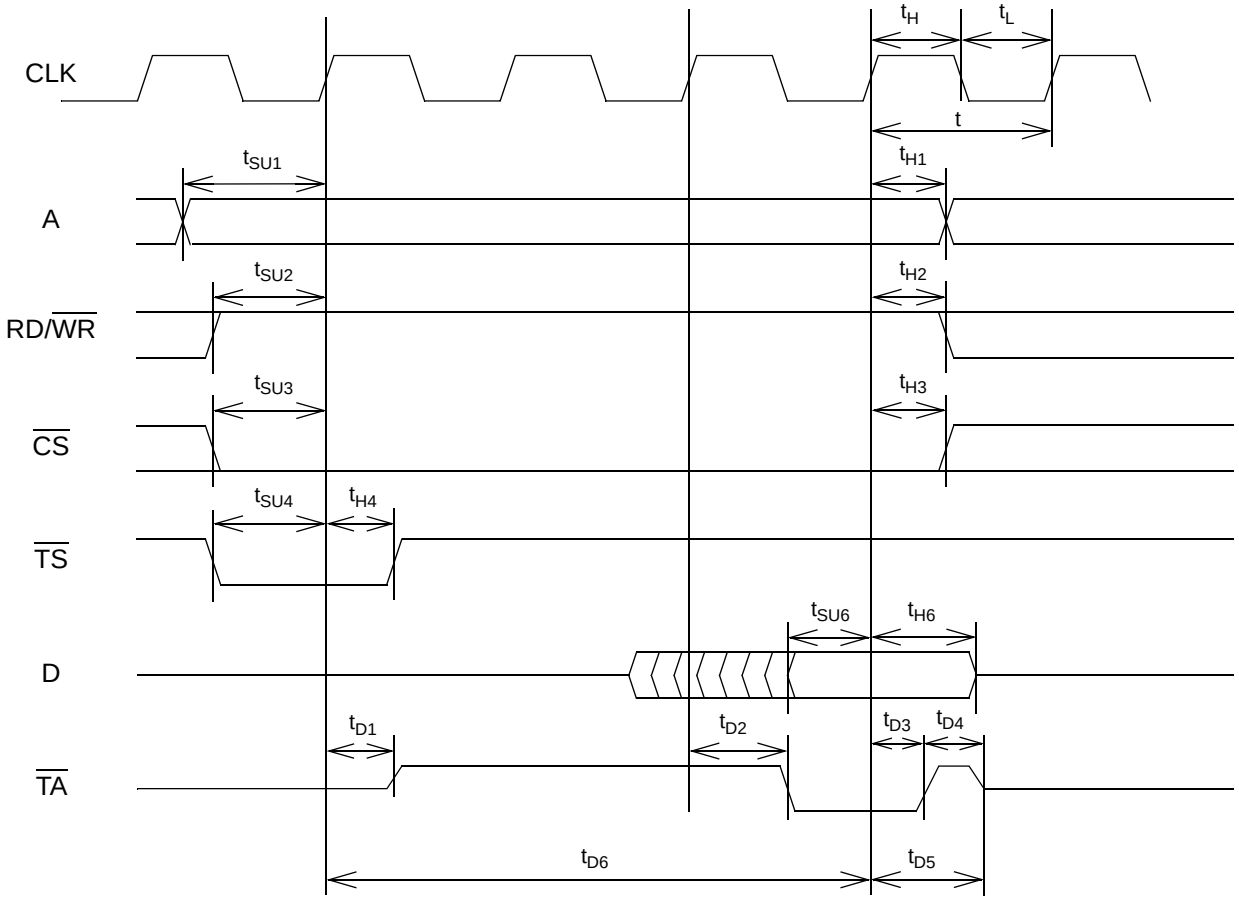


Figure 64. Microprocessor Interface: Motorola MPC860 Mode Read Cycle[1]

1. See the Lead Description table on Motorola MPC860 - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of RD/$\overline{WR}$ to rising edge CLK
t_{SU3} [a, c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{SU4}	6 ns	-	Setup time of falling edge $\overline{TS}$ to rising edge CLK
t_{H1} [d]	0 ns	-	Hold time of A to rising edge CLK
t_{H2} [d, e]	0 ns	-	Hold time of RD/$\overline{WR}$ to rising edge CLK
t_{H3} [c, d]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{H4}	4 ns	-	Hold time of $\overline{TS}$ to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{TA}$ driving
t_{D2} [f]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{TA}$
t_{D3} [d]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{TA}$
t_{D4}	4 ns	-	Delay from $\overline{TA}$ going inactive to $\overline{TA}$ going in tristate
t_{D5} [d]	-	20 ns	Delay from rising edge CLK to $\overline{TA}$ going in tristate
t_{D6}	363 ns	606 ns	Maximum response latency
t_{SU6} [d]	t	-	Setup time of D to rising edge CLK
t_{H6} [d]	1 ns	12 ns	Hold time of D going in tristate to rising edge CLK

a. Timing is relative to the rising edge of CLK during which $\overline{TS}$ is asserted.
b. Only applies if a read access is preceded by a write access. RD/WR may stay high between 2 successive read accesses to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral.
d. Timing is relative to the rising edge of CLK during which $\overline{TA}$ is asserted.
e. Only applies if a read access is followed by a write access. RD/$\overline{WR}$ may stay high between 2 successive read accesses to the same peripheral.
f. Timing is relative to the rising edge before the one during which $\overline{TA}$ is asserted.

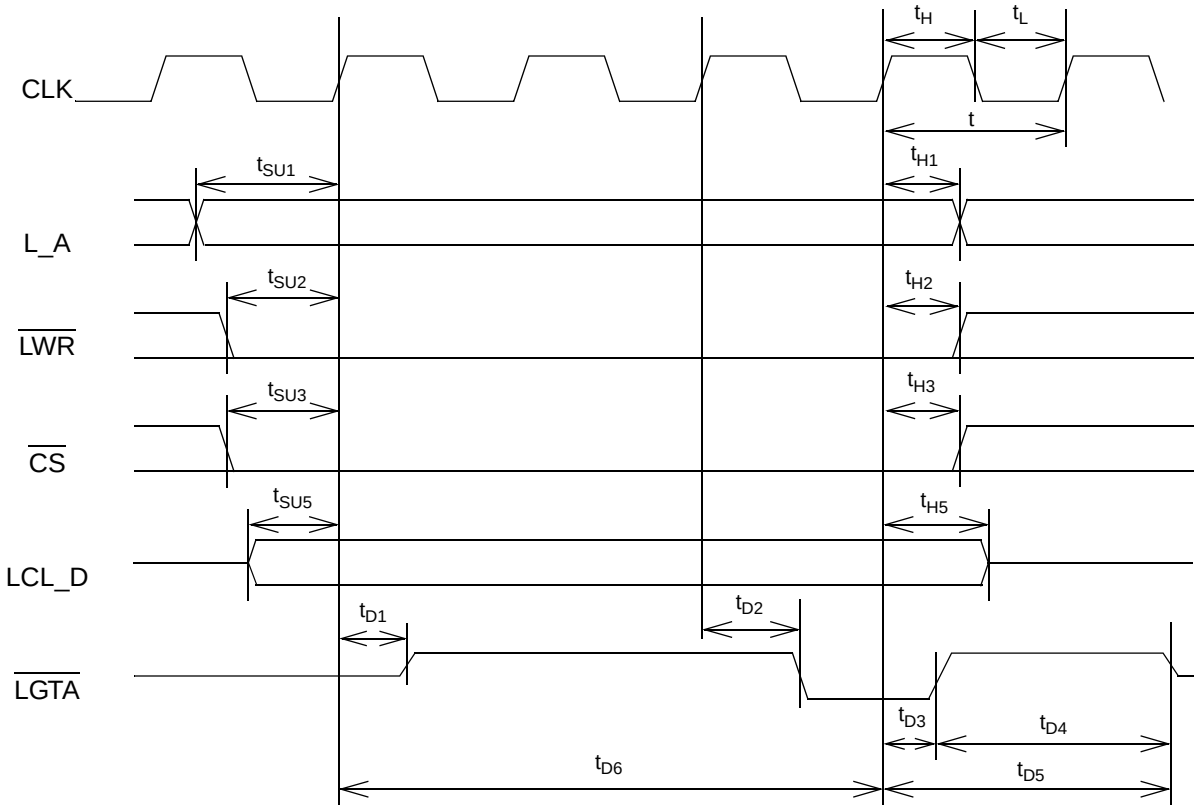


Figure 65. Microprocessor Interface: Motorola MPC8260 Local Bus Mode Write Cycle[1]

1. See the Lead Description table on Motorola MPC8260 Local Bus - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of L_A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of $\overline{LWR}$ to rising edge CLK
t_{SU3} [c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{SU5} [a]	0 ns	-	Setup time of LCL_D to rising edge CLK
t_{H1} [d]	0 ns	-	Hold time of L_A to rising edge CLK
t_{H2} [d, e]	0 ns	-	Hold time of $\overline{LWR}$ to rising edge CLK
t_{H3} [c, d]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{H5} [d]	0 ns	-	Hold time of LCL_D to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{LGTA}$ driving
t_{D2} [f]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{LGTA}$
t_{D3} [d]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{LGTA}$
t_{D4}	3t + 4 ns	-	Delay from $\overline{LGTA}$ going inactive to $\overline{LGTA}$ going in tristate
t_{D5} [d]	3t	3t + 20 ns	Delay from rising edge CLK to $\overline{LGTA}$ going in tristate
t_{D6}	363 ns	606 ns	Maximum response latency

a. Timing is relative to the first rising edge of the access during which $\overline{CS}$ is asserted.
b. Only applies if a write access is preceded by a read access. $\overline{LWR}$ may stay low if 2 successive write accesses are done to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral, as long as the other setup times are respected for the 2nd access. If $\overline{CS}$ remains low between accesses, the second access starts after the first is terminated.
d. Timing is relative to the rising edge during which $\overline{LGTA}$ is asserted.
e. Only applies if a write access is followed by a read access. $\overline{LWR}$ may stay low if 2 successive write accesses are done to the same peripheral.
f. Timing is relative to the rising edge before the one during which $\overline{LGTA}$ is asserted.

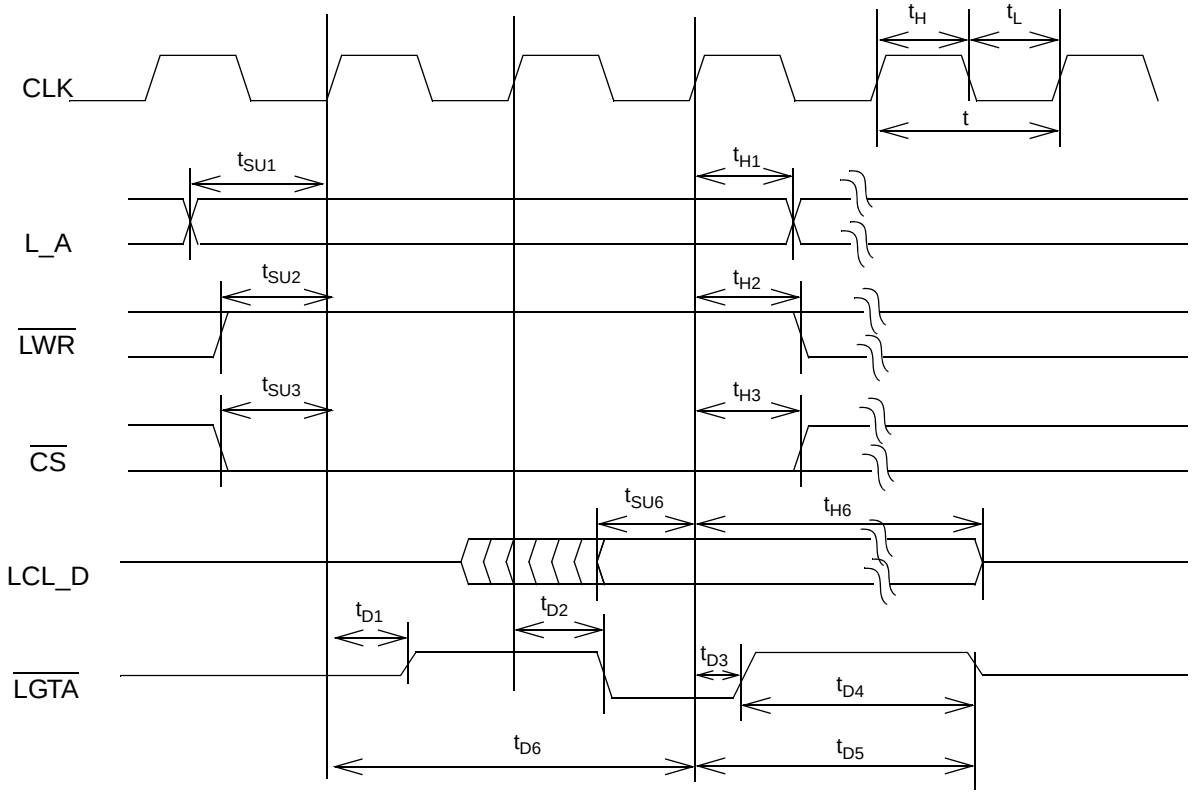


Figure 66. Microprocessor Interface: Motorola MPC8260 Local Bus Mode Read Cycle[1]

1. See the Lead Description table on Motorola MPC8260 Local Bus - Host Processor Interface for the mapping to I/O leads.

Symbol	Min	Max	Description
t	20 ns	-	CLK clock period
t_L	0.4t	-	CLK clock low phase pulse width
t_H	0.4t	-	CLK clock high phase pulse width
t_{SU1} [a]	0 ns	-	Setup time of L_A to rising edge CLK
t_{SU2} [a, b]	0 ns	-	Setup time of $\overline{LWR}$ to rising edge CLK
t_{SU3} [c]	6 ns	-	Setup time of $\overline{CS}$ to rising edge CLK
t_{H1} [d]	0 ns	-	Hold time of L_A to rising edge CLK
t_{H2} [d, e]	0 ns	-	Hold time of $\overline{LWR}$ to rising edge CLK
t_{H3} [c, d]	0 ns	-	Hold time of $\overline{CS}$ to rising edge CLK
t_{D1} [a]	0 ns	20 ns	Delay from rising edge CLK to $\overline{LGTA}$ driving
t_{D2} [f]	1 ns	7 ns	Delay from rising edge CLK to active edge $\overline{LGTA}$
t_{D3} [d]	1 ns	7 ns	Delay from rising edge CLK to inactive edge $\overline{LGTA}$
t_{D4}	3t + 4 ns	-	Delay from $\overline{LGTA}$ going inactive to $\overline{LGTA}$ going in tristate
t_{D5} [d]	3t	3t + 20 ns	Delay from rising edge CLK to $\overline{LGTA}$ going in tristate
t_{D6}	363 ns	606 ns	Maximum response latency
t_{SU6} [d]	t	-	Setup time D to rising edge CLK
t_{H6} [d]	4t + 1 ns	4t + 12 ns	Hold time of D going in tristate to rising edge CLK

a. Timing is relative to the first rising edge of the access during which $\overline{CS}$ is asserted.
b. Only applies if a read access is preceded by a write access. $\overline{LWR}$ may stay high if 2 successive read accesses are done to the same peripheral.
c. $\overline{CS}$ may stay low between successive accesses to the same peripheral, as long as the other setup times are respected for the 2nd access. If $\overline{CS}$ remains low between accesses, the second access starts after the first is terminated.
d. Timing is relative to the rising edge during which $\overline{LGTA}$ is asserted.
e. Only applies if a read access is followed by a write access. $\overline{LWR}$ may stay high if 2 successive read accesses are done to the same peripheral.
f. Timing is relative to the rising edge before the one during which $\overline{LGTA}$ is asserted.

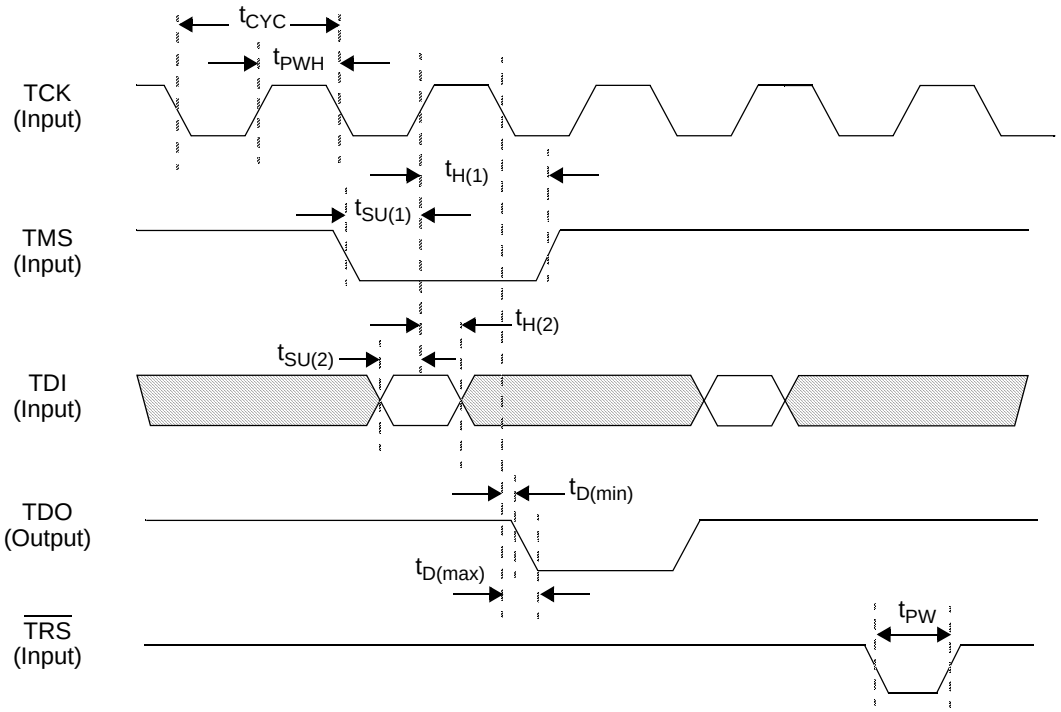


Figure 67. Boundary Scan Timing

Parameter	Symbol	Min	Max	Unit
TCK clock period	t_{CYC}	100		ns
TCK clock duty cycle $t_{PWH/tCYC}$		40	60	%
TMS setup time to TCK↑	$t_{SU(1)}$	3.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	15		ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	15		ns
TDO delay from TCK↓	t_D	4.0	20	ns
$\overline{TRS}$ pulse width	t_{PW}	250		ns

8.0 MEMORY MAPS

This section contains the address map of the internal memory locations of the PHAST-12P. The Access columns of the tables specify the access types as Read-only (ro), Read-Write (rw), Clear-On-Read (cor) or Clear-On-Write-1 (cow_1).

All addresses and offsets are byte addresses.
Bit transmission order is Bite 1 - Bit 8. This corresponds to Bits 7 - 0 in the memory map.
For alarm bits, 1 indicates alarm present. 0 indicates alarm not present. Latched status bits should be cleared after power-up and initial configuration so that any transitory values that might have occurred during device setup can be cleared.

8.1 OVERVIEW

Table 5: Memory Map Overview

Offset	Description
0x0000	Global Control (See page 196.)
0x0080	Line Ring Port/Alarm Interface (See page 198.)
0x00A0	Reset Generator (See page 198.)
0x00B0	Interrupt (See page 199.)
0x00C0	Transmit APS Port (See page 201.)
0x0100	Ingress UTOPIA/POS-PHY Level 2 Interface (See page 202.)
0x0200	POH Generator (See page 204.)
0x0400	TOH Monitor - Rx Line 1 (See page 208.)
0x0500	TOH Monitor - Rx Line 2 (See page 208.)
0x0600	TOH Monitor - Rx Line 3 (See page 208.)
0x0700	TOH Monitor - Rx Line 4 (See page 208.)
0x0800	TOH Generator (See page 213.)
0x1000	TOH and DCC Port (See page 215.)
0x1800	High Order Pointer Tracker and Retimer - Rx Line Interface (See page 217.)
0x1C00	High Order Pointer Tracker and Retimer - Rx APS Interface (See page 217.)
0x2000	POS/ATM Demapper (See page 220.)
0x3000	POS/ATM Mapper (See page 224.)
0x3800	Pointer Generator (See page 228.)
0x3A00	Clock Recovery/Clock Synthesis/SerDes (See page 229.)
0x3B00	Receive APS Port (See page 235.)
0x3C00	Cross Connect (See page 237.)
0x3E00	Egress UTOPIA/POS-PHY Level 2 Interface (See page 238.)
0x3E80	High Order Path Ring Port/Alarm Interface (See page 240.)
0x3F00	JTAG Master (See page 241.)

Table 5: Memory Map Overview

Offset	Description
0x4000	POH Monitor - Rx Line Interface (See page 242.)
0x4800	POH Monitor - Rx APS Interface (See page 242.)
0x5000	POH Monitor - Terminal Side (See page 242.)

8.2 GLOBAL CONTROL

Table 6: Global Control (T_GLOBAL_CONTROL)

Offset	Bits	Name	Init	Access	Description
0x0000		DeviceIdentification		ro	T_DeviceIdentification (See page 197.) Device identification.
0x0010	0	STM4_Mode	0x0	rw	STM-4/OC-12 Mode when 0x1: Line 1 is a 622.08 Mbit/s signal, lines 2 to 4 are not used. STM-1/OC-3 Mode when 0x0: lines 1 to 4 are 155.52 Mbit/s signals.
0x0012	0	Reserved	0x1	rw	**Reserved. This field must be set to 0x0.**
0x0014	0	UTOPIA2	0x1	rw	The terminal interface operates in POS-PHY Level 2 Mode when 0x0. The terminal interface operates in UTOPIA Level 2 mode when 0x1.
0x0016	8 - 0	TimeOutCount	0x1FF	rw	Range 0 to 511 Acknowledge Time Out Count. Specifies the Time Out after which an Acknowledge is generated if a request hasn't been acknowledged. Timebase is the microprocessor clock period (MPCLK).
0x0018	0	AckOnTimeOut	0x1	rw	Acknowledge on Time Out. An Acknowledge will be generated upon failed accesses after a period specified by TimeOutCount when 0x1. No Acknowledge will be generated upon failed accesses when 0x0.
0x001A	15 - 0	LastAddress	0x0	ro	Last Address. Indicates the address of the last timed-out request. Note: The address returned is a word address.
0x001C	0	Reserved	0x0	ro	Reserved.
0x001E	15 - 0	LocDivider	0x4	rw	Range 0 to 65535 Loss Of Clock Divider. The clock to be monitored is divided by this number + 1 for LOC detection.
0x0020	15 - 0	LocEntryThreshold	0x20	rw	Range 1 to 65535 Loss Of Clock Entry Threshold. Specifies the time without divided clock transition before declaring LOC. Timebase is the microprocessor clock period (MPCLK).
0x0024	15 - 0	LocExitThreshold	0x2	rw	Range 1 to 65535 Loss Of Clock Exit Threshold. LOC is deasserted when this many divided clock transitions were detected. Detection occurs in the microprocessor clock domain (MPCLK).
0x0028	0	External1secRef_Select	0x0	rw	External One Second Reference Select. The one second reference on the REFONESECCLK is used when 0x1. The one second reference is generated internally when 0x0.
0x002C	0	DeviceInitialized	0x0	rw	The device processes incoming data when this value is set to 0x1. The software must set this value to 0x1 as soon as it has finished the configuration of the device.
0x0030	3 - 0	GP_Input	0x0	ro	General purpose input (GPIN4...GPIN1).

Table 6: Global Control (T_GLOBAL_CONTROL) (cont.)

Offset	Bits	Name	Init	Access	Description
0x0034	3 - 0	GP_Output	0x0	rw	General purpose output (GPOUT4...GPOUT1).
0x0038	5 - 0	RamResetDone	0x0	ro	For every bit in the list, 0x1 means the RAMs of the corresponding clock domain are initialized, 0x0 the RAMs are not initialized. • bit 0: System Clock domain • bit 1: Rx Line 1 Clock domain • bit 2: Rx Line 2 Clock domain • bit 3: Rx Line 3 Clock domain • bit 4: Rx Line 4 Clock domain • bit 5: Rx APS Clock domain
0x003A	10 - 0	GlobalControlSummary_Unlatched	0x0	ro	Global Control Interrupt Summary. • bit 0: Loss of System Clock • bit 1: Loss of Clock for Rx Line PLL1 • bit 2: Loss of Clock for Rx Line PLL2 • bit 3: Loss of Clock for Rx Line PLL3 • bit 4: Loss of Clock for Rx Line PLL4 • bit 5: Loss of Clock for Rx APS PLL • bit 6: Loss of Rx UTOPIA Clock • bit 7: Loss of Tx UTOPIA Clock • bit 8: Reserved • bit 9: Acknowledge Time Out • bit 10: One Second Reference
0x003C	10 - 0	GlobalControlSummary_LatchForInt	0x0	cow_1	Global Control Interrupt Summary. See GlobalControlSummary_Unlatched for details.
0x003E	10 - 0	GlobalControlSummary_Mask	0x7FF	rw	Global Control Interrupt Summary Mask. See GlobalControlSummary_Unlatched register for details.
0x0040		ScratchPad	All 0x0	rw	Array (32) of two_bytes Offset between two elements = 0x2. Array index indicates the scratch pad address. Scratch pad: general purpose read/write memory which can be used as scratch pad by the device driver.

Table 7: Device Identification (T_DeviceIdentification)

Offset	Bits	Name	Init	Description
0x0000	10 - 0	ManufacturerIdentity	0x6B	Manufacturer Identity, assigned by the Solid State Products Engineering Council (JEDEC) to the TranSwitch Corporation (0x06B = “0001101011”).
0x0002	15 - 0	PartNumber	0x190C	Part Number (06412).
0x0004	3 - 0	Version	--	Version or revision level. The version register will be incremented with each new revision of the part.
0x0006	Growth_Mask			
	3 - 0	MaskLevel	0x0	Indicates the Mask Level.
	7 - 4	GrowthField	0x0	Indicates the Growth Field.
0x0008	12 - 0	Reserved	0x0	Reserved.

8.3 LINE RING PORT/ALARM INTERFACE

Table 8: Ring Port/Alarm Interface (T_TOH_RING_PORT)

Offset	Bits	Name	Init	Access	Description
0x0000		ExternalSourceSelect	All 0x0	rw	Array (4) of boolean Offset between two elements = 0x2. Array index indicates the line (= line number - 1). Selection of external ring port interface. The internal ring port interface is used when 0x0, the external port is used when 0x1.
0x0008	0	CRC_Error_Insert	0x0	rw	Insert CRC errors. All CRC bits are inverted when 0x1 (for test purposes only).
0x000A		CorrDefects_Unlatched		ro	T_TOH_RING_PORT_Defects (See page 198.) Correlated defects.
0x000C		CorrDefects_LatchForInt		cow_1	T_TOH_RING_PORT_Defects (See page 198.) Correlated defects latched for interrupt.
0x000E		CorrDefects_Mask		rw	T_TOH_RING_PORT_Defects (See page 198.) Correlated defects masks.

Table 9: Ring Port/Alarm Interface Defects (T_TOH_RING_PORT_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	CRC_Error	0x1	CRC error on external Ring Port interface.
	1	LOC	0x1	Loss of clock on external Ring Port interface.

8.4 RESET GENERATOR

Table 10: Reset Generator (T_RGEN)

Offset	Bits	Name	Init	Access	Description
0x0000	7 - 0	RESETH	0x0	rw	Microprocessor Controlled Reset. Writing the value 0x91 to this register generates a reset in all clock domains, except the microprocessor clock domain (MPCLK). Reset is active as long as this register contains the value 0x91.
0x0002	7 - 0	Reserved	0x0	rw	Reserved
0x0004	7 - 0	Reserved	0x0	rw	Reserved.
0x0006	7 - 0	Reserved	0x0	rw	Reserved
0x0008	7 - 0	RxLine1_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 1. Writing the value 0x91 to this register generates a reset in the Receive Line 1 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.

Table 10: Reset Generator (T_RGEN) (cont.)

Offset	Bits	Name	Init	Access	Description
0x000A	7 - 0	RxLine2_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 2. Writing the value 0x91 to this register generates a reset in the Receive Line 2 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.
0x000C	7 - 0	RxLine3_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 3. Writing the value 0x91 to this register generates a reset in the Receive Line 3 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.
0x000E	7 - 0	RxLine4_Reset	0x0	rw	Microprocessor Controller Reset for Rx Line 4. Writing the value 0x91 to this register generates a reset in the Receive Line 4 clock domain. Reset is active as long as this register contains the value 0x91. Note: Only assert reset when RESETH = 0x91. Can be deasserted at any time.

8.5 INTERRUPT

Table 11: Interrupt (T_INTERRUPT)

Offset	Bits	Name	Init	Access	Description
0x0000	11 - 0	APS_Interrupts_Mask	0xFFF	rw	APS Interrupts Mask. See APS_Interrupts register for details.
0x0004		IntCtrl_Config		rw	T_InterruptCtrl_Config (See page 200.) Interrupt and performance configuration.
0x0006	0	HINT	0x0	ro	Global device interrupt (HINT = Hardware INTerrupt).
0x0008	0	HINTEN	0x0	rw	The global device interrupt is enabled when 0x1, no interrupt will be generated when 0x0 (HINTEN = Hardware INTerrupt ENable).

Table 11: Interrupt (T_INTERRUPT) (cont.)

Offset	Bits	Name	Init	Access	Description
0x000A	15 - 0	GeneralInterrupts	0x0	ro	General Interrupts Register: • bit 0: Global Control Interrupt • bit 1: Pointer Generator • bit 2: Reserved • bit 3: Transmit UTOPIA/POS-PHY • bit 4: POS/ATM Mapper • bit 5: POS/ATM Demapper • bit 6: POH Ring Port • bit 7: Terminal POH Monitor • bit 8: Line Pointer Tracker/Retimer • bit 9: TOH Ring Port • bit 10: Receive TOH/DCC Port • bit 11: TOH Monitor Line 1 • bit 12: TOH Monitor Line 2 • bit 13: TOH Monitor Line 3 • bit 14: TOH Monitor Line 4 • bit 15: Mixed Signal
0x000C	11 - 0	APS_Interrupts	0x0	ro	APS Interrupts Register: • bit 0: APS Pointer Tracker/Retimer • bit 1: Receive APS • bit 2: APS POH Monitor • bit 3: Line POH Monitor • bit 4: Receive APS Line 1 • bit 5: Receive APS Line 2 • bit 6: Receive APS Line 3 • bit 7: Receive APS Line 4 • bit 8: TOH Monitor APS Line 1 • bit 9: TOH Monitor APS Line 2 • bit 10: TOH Monitor APS Line 3 • bit 11: TOH Monitor APS Line 4
0x000E	15 - 0	GeneralInterrupts_Mask	0xFFFF	rw	General Interrupts Mask. See GeneralInterrupts register for details.

Table 12: Interrupt Configuration (T_InterruptCtrl_Config)

Offset	Bits	Name	Init	Description
0x0000	7 - 0	ResetCounters	0x0	All performance counters are reset when the value 0x91 is written to this register. Reset is active as long this register contains the value 0x91.
	9 - 8	LatchForIntCtrl	0x3	0x0 = INT_LEVEL 0x1 = INT_RISING_EDGE 0x2 = INT_FALLING_EDGE 0x3 = INT_BOTH_EDGES Field to control on which edges the unlatched defects are latched for interrupts.
	10	Reserved	0x0	Reserved.

8.6 TRANSMIT APS PORT

Table 13: Transmit APS Port (T_TX_APS)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_TX_APS_Common_Config (See page 201.) General configuration.
0x0020		MSP		rw	Array (4) of T_TX_APS_Config (See page 201.) Offset between two elements = 0x8. Array index indicates the line (= line number - 1). Multiplex Section Protection configuration.

Table 14: Transmit APS Port Configuration (T_TX_APS_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	Functionality			
	0	AIS_Force	0x0	Insertion of line AIS is forced when 0x1.
	1	Scrambler_Disable	0x0	Scrambling is disabled when 0x1.
0x0002	Setting			
	7 - 0	B1_Mask	0x0	Mask used on the B1 byte, set to default value for normal operation.
	15 - 8	J0_Insert	0x0	J0 byte. Used as a form of simple connection identification.
0x0004		B2_Mask	All 0x0	Array (12) of byte Offset between two elements = 0x2. Mask used on the B2 byte, set to the default value for normal operation.

Table 15: Transmit APS Port Line Configuration (T_TX_APS_Config)

Offset	Bits	Name	Init	Description
0x0000	Enable			
	0	K1K2_ForwardEnable	0x0	Rx K1 K2 APS signal are forwarded from MSOH monitor when 0x1, Rx K1 K2 APS signal are inserted from register when 0x0. (RX_K1K2_Data).
	1	SignalFail_ForwardEnable	0x0	Signal fail indication is forwarded from MSOH monitor when 0x1, signal fail indication is inserted from register (StatusRequest) when 0x0. Positioned at the LSB of the status-byte.
	2	SignalDegrade_ForwardEnable	0x0	Signal degrade indication is forwarded from MSOH monitor when 0x1, signal degrade indication is inserted from register (StatusRequest) when 0x0. Positioned at the 2nd LSB of the status-byte.
0x0002	15 - 0	RX_K1K2_Data	0x0	Register that contains the values for Rx K1 and Rx K2. Rx K1 is located in MSB, Rx K2 is located in LSB.
0x0004	15 - 0	TX_K1K2_Data	0x0	Register that contains the values for Tx K1 and Tx K2. Tx K1 is located in MSB, Tx K2 is located in LSB.
0x0006	15 - 0	StatusRequest	0x0	Register that contains the values for Status and Request. Status is located in MSB, Request is located in LSB.

8.7 INGRESS UTOPIA/POS-PHY LEVEL 2 INTERFACE

Table 16: Ingress UTOPIA/POS-PHY (T_DI_UTOPIA_POSPHY)

Offset	Bits	Name	Init	Access	Description
0x0000		CorrDefects_Mask		rw	Array (12) of T_DIUP_CorrDefects (See page 203.) Offset between two elements = 0x2. Array index indicates the PHY. Defects mask.
0x0040		CorrDefects_Unlatched		ro	Array (12) of T_DIUP_CorrDefects (See page 203.) Offset between two elements = 0x2. Array index indicates the PHY. Defects.
0x0080		CorrDefects_LatchForInt		cow_1	Array (12) of T_DIUP_CorrDefects (See page 203.) Offset between two elements = 0x2. Array index indicates the PHY. Defects latched for interrupt.
0x00C0		DirectStatus_Config		rw	Array (4) of T_DirectStatusTimeslot (See page 203.) Offset between two elements = 0x2. Array index indicates the CLAV for UTOPIA, the TPA for POS-PHY. Direct status configuration.
0x00D0		Common_Config		rw	T_DI_UTOPIA_POSPHY_Common_Config (See page 203.) General configuration.
0x00D8	11 - 0	CorrDefects_Summary	0x0	ro	Defects summary, one bit per PHY. Least significant bit corresponds to the first PHY.
0x00DC	11 - 0	CorrDefects_SummaryMask	0xFFF	rw	Defects summary mask, one bit per PHY. Least significant bit corresponds to the first PHY.
0x00E0		PHY_Port_Config		rw	Array (12) of T_UTOPIA_POSPHY_PHY_Port_Config (See page 204.) Offset between two elements = 0x2. Array index indicates the PHY. PHY Configuration.

Table 17: Ingress UTOPIA/POS-PHY Defects (T_DIUP_CorrDefects)

Offset	Bits	Name	Init	Description
0x0000	0	LateSOC_Error	0x1	Late SOC error. Applies to UTOPIA mode only.
	1	EarlySOC_Error	0x1	Early SOC error. Applies to UTOPIA mode only.
	2	ParityError	0x1	Parity error. Applies to both UTOPIA and POS-PHY mode.
	3	SOP_EOP_Error	0x1	SOP without a preceding EOP or the inverse. Applies to POS-PHY mode only.
	4	Overflow_Error	0x1	Overflow Error: • UTOPIA Mode: Trying to write new cell without CLAV. • POS-PHY Mode: Internal FIFO full condition. Trying to write a new cell without CLAV

Table 18: Direct Status Configuration (T_DirectStatusTimeslot)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	Timeslot	0x0	Range 0 to 11 Timeslot used for this CLAV/TPA. Applies to both UTOPIA and POS-PHY mode.

Table 19: Ingress UTOPIA/POS-PHY Common Configuration (T_DI_UTOPIA_POSPHY_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	Protocol			
	0	EnableInterface	0x0	Enables the interface when 0x1. Applies to both UTOPIA and POS-PHY mode.
	1	MPHY	0x1	Multiple PHY mode when 0x1, Single PHY mode when 0x0. Applies to both UTOPIA and POS-PHY mode.
	2	Reserved	0x1	Reserved
	4 - 3	StatusIndication	0x1	0x0 = DIRECT_STATUS 0x1 = MUX_STATUS_POLLING_FULL_ADDR 0x2 = MUX_STATUS_POLLING_GROUP_ADDR Applies to both UTOPIA and POS-PHY mode, note that for POS-PHY mode the option multiplexed status polling with group address is not valid.
	5	ParityEven	0x0	Even parity is used when 0x1, odd parity when 0x0. Applies to both UTOPIA and POS-PHY mode.
	6	ParityOverDataOnly	0x1	The parity is calculated over databus only when 0x1, over databus and control signals when 0x0. Applies to both UTOPIA and POS-PHY mode.
	14 - 7	Threshold	0x0	Range 0 to 124 Threshold used for low transition of STPA. Applies to POS-PHY mode only.

Table 19: Ingress UTOPIA/POS-PHY Common Configuration (T_DI_UTOPIA_POSPHY_Common_Config) (cont.)

Offset	Bits	Name	Init	Description
0x0002	Threshold			
	7 - 0	SpaceAV_Threshold_Low	0x1B	Range 0 to 124 Maximum number of free words which may be available in the FIFO before the near full indication (PTPA low) is set on the POS-PHY interface. Applies to POS-PHY mode only.
	15 - 8	SpaceAV_Threshold_High	0x1B	Range 4 to 124 Minimum number of free words which needs to be available in the FIFO before the space available indication (PTPA/CLAV high) is set on the POS-PHY interface. Applies to POS-PHY mode only, for UTOPIA mode this should always be set to 27 (0x1B).

Table 20: UTOPIA/POS-PHY PHY/Port Configuration (T_UTOPIA_POSPHY_PHY_Port_Config)

Offset	Bits	Name	Init	Description
0x0000	4 - 0	Address	0x1F	Address of this PHY. Applies to both UTOPIA and POS-PHY mode.
	5	Enable	0x0	Enables this PHY when 0x1. Applies to both UTOPIA and POS-PHY mode.

8.8 POH GENERATOR

Table 21: POH Generator (T_POH_GENERATOR)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_VCXPG_Common_Config (See page 204.) General configuration.
0x0100		VC_Config		rw	T_VCXPG_VC_Config (See page 205.) High order path configuration. The high order path to be configured is selected by indirect access. See the Config_Channel register in the Common_Config record to select the desired high order path.

Table 22: POH Generator Common Configuration (T_VCXPG_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	Config_Channel	0x0	Range 0 to 11 High order path for which configuration can be done in VC_Config.
0x0002		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration.

Table 23: AUG-1 Mode Configuration (T_AUG1_Mode_Config)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	TimeslotIsConcatenated	0x0	Concatenation setting, one bit per AUG-1. Each bit has following meaning (Least significant bit represents the first AUG-1. Don't care for line side in STM-1 mode): The corresponding AUG-1 is either an independent AUG-1 or the first AUG-1 of a larger concatenated structure when '0' (e.g., AU4-4c). The corresponding AUG-1 is part of a larger concatenated structure (but not the first one) when '1'. Note: The least significant bit must be '0' (the first AUG-1 is always master). This bit will be forced to '0', no matter what has been written to it.
	7 - 4	Has_AU3	0x0	Selection between AU-3 and AU-4 mapping for independent AUG-1's, one bit per AUG-1. Each bit has following meaning (Least significant bit represents the first AUG-1. For the line side: least significant bit represents the first AUG-1 in STM-4 mode or the first line in STM-1 mode): The corresponding AUG-1 contains an AU-4 when '0', the corresponding AUG-1 contains three AU-3's when '1'. Note the configuration is a don't care for AUG-1's which are part of a larger concatenated structure. It is advisable to fill in the default value.
	11 - 8	Reserved	0x0	Reserved.

Table 24: POH Generator Path Configuration (T_VCXPG_VC_Config)

Offset	Bits	Name	Init	Description
0x0000		RAM		T_VCXPG_RAMBytes (See page 206.) Configuration of the POH RAM bytes.
0x0090		Mode		T_VCXPG_Mode_record (See page 206.) Mode Configuration.
0x0092		Control		T_VCXPG_Control_record (See page 207.) Source selection for the POH bytes.

Table 25: Transmit POH Byte RAM (T_VCXPG_RAMBytes)

Offset	Bits	Name	Init	Description
0x0000		J1	All 0x0	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. TTI-message for insertion in the J1 location. • bytes 0-15 for 16 byte TTI message • bytes 0-63 for 64 byte TTI message
0x0080	7 - 0	B3_ErrorMask	0x0	Mask used on the B3 byte, set to default value for normal operation.
0x0082	7 - 0	C2	0x0	Signal label to be inserted.
0x0084	7 - 0	G1	0x0	Value used when G1 is inserted out of RAM.
0x0086	7 - 0	F2	0x0	Value used when F2 is inserted out of RAM.
0x0088	7 - 0	H4	0x0	Value used when H4 is inserted out of RAM.
0x008A	7 - 0	F3	0x0	Value used when F3 is inserted out of RAM.
0x008C	7 - 0	K3	0x0	Value used when K3 is inserted out of RAM.
0x008E	7 - 0	N1	0x0	Value used when N1 is inserted out of RAM.

Table 26: POH Generator Path Mode (T_VCXPG_Mode_record)

Offset	Bits	Name	Init	Description
0x0000	0	Force_AIS	0x0	AIS insertion is forced in the corresponding high order path when 0x1.
	1	Force_Uneq	0x0	Unequipped is forced in the corresponding high order path when 0x1.
	2	Force_SupUneq	0x0	Supervisory Unequipped is forced in the corresponding high order path when 0x1.
	3	UniDirectional	0x0	Uni-directional option is activated (G1 byte will be filled with 0x00, regardless the byte provided from the selected source) when 0x1.
	4	OneBitRDI	0x0	RDI is encoded in one bit when 0x1, in three bits (Enhanced RDI) when 0x0.
	5	Reserved	0x0	Reserved.

Table 27: POH Byte Source Control (T_VCXPG_Control_record)

Offset	Bits	Name	Init	Description
0x0000	1 - 0	REI_Control	0x0	0x0 = VCXPG_RAM_RI 0x1 = VCXPG_POH_INTF_RI 0x2 = VCXPG_PR_RI Selects the source of the G1 REI field. • VCXPG_RAM_RI = Use RAM as source • VCXPG_POH_INTF_RI = Use POH Port Interface as source • VCXPG_PR_RI = Use Ring port Interface as source
	3 - 2	RDI_Control	0x0	0x0 = VCXPG_RAM_RI 0x1 = VCXPG_POH_INTF_RI 0x2 = VCXPG_PR_RI Selects the source of the G1 RDI value. • VCXPG_RAM_RI = Use RAM as source • VCXPG_POH_INTF_RI = Use POH Port Interface as source • VCXPG_PR_RI = Use Ring port Interface as source
	4	SPARE_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the G1 SPARE bit. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	5	F2_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the F2 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	7 - 6	H4_Control	0x0	0x0 = VCXPG_RAM_H4 0x1 = VCXPG_POH_INTF_H4 0x2 = Reserved 0x3 = Reserved Selects the source of the H4 Byte. • VCXPG_RAM_H4 = Use RAM as source • VCXPG_POH_INTF_H4 = Use POH Port Interface as source
	8	F3_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the F3 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	9	K3_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the K3 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source
	10	N1_Control	0x0	0x0 = VCXPG_RAM 0x1 = VCXPG_POH_INTF Selects the source of the N1 Byte. • VCXPG_RAM = Use RAM as source • VCXPG_POH_INTF = Use POH Port Interface as source

8.9 TOH MONITOR

Table 28: TOH Monitor (T_TOH_MONITOR)

Offset	Bits	Name	Init	Access	Description
0x0000		TTI_ExpectedMessage	All 0x0	rw	Array (16) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Expected TTI message: • 16 byte TTI message: specify all sixteen bytes. • 1 byte specific TTI message: write all bytes with the same value. This register is only used when NonSpecificMessage is 0x0 (see J0 TTI Configuration).
0x0040		TTI_ReportedMessage	All 0x0	ro	Array (16) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Reported TTI message.
0x0080		PerfCounters_Shadow		ro	T_TOH_MONITOR_Performance_Counters (See page 208.) RSOH/MSOH Performance counters.
0x00A0		Line_Status		ro/cow_1	T_TOH_MONITOR_Line_Status (See page 209.) Line Status. Note: Latched bits are clear-on-write-1, all others are read-only.
0x00B0		CorrDefects_LatchForInt		cow_1	T_TOH_MONITOR_Defects (See page 209.) Correlated defects latched for interrupt.
0x00B4		APS_Defects_Mask		rw	T_TOH_MONITOR_APS_Defects (See page 209.) Defects for APS handling mask.
0x00B8		APS_Defects_LatchForInt		cow_1	T_TOH_MONITOR_APS_Defects (See page 209.) Defects for APS handling latched for (APS) interrupt.
0x00BC		CorrDefects_Unlatched		ro	T_TOH_MONITOR_Defects (See page 209.) Correlated defects.
0x00BE		CorrDefects_Mask		rw	T_TOH_MONITOR_Defects (See page 209.) Correlated defects mask.
0x00C0		Common_Config		rw	T_TOH_MONITOR_Common_Config (See page 210.) General configuration.

Table 29: TOH Monitor Performance Counters (T_TOH_MONITOR_Performance_Counters)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	B1_BIP_Errors	0x0	B1 BIP error counter. Configurable as bit or block count.
0x0002	15 - 0	B2_BIP_BitErrors_LSB	0x0	B2 BIP bit error counter, least significant bits.
0x0004	3 - 0	B2_BIP_BitErrors_MSB	0x0	B2 BIP bit error counter, most significant bits.
0x0006	12 - 0	B2_BIP_BlockErrors	0x0	B2 BIP block error counter.
0x0008	15 - 0	REI_BIP_Errors	0x0	REI BIP Counter. Configurable as bit or block count.
0x000A	DefectSeconds			
	0	NearEndDefectSec	0x0	TSF one second latch.
	1	FarEndDefectSec	0x0	RDI defect one second latch.

Table 30: TOH Monitor Status (T_TOH_MONITOR_Line_Status)

Offset	Bits	Name	Init	Description
0x0000	TTI_StableIndications			
	0	TTI_Stable1	0x0	TTI 1 byte message stable indication.
	1	TTI_Stable16	0x0	TTI 16 byte message stable indication.
	2	TTI_Stable16_Latched	0x0	Latched TTI 16 byte message stable indication. This field is clear-on-write-1.
0x0002	15 - 0	Debounced_K1K2	0x0	Debounced value of K1/K2 bytes (most significant byte is K1, least significant byte is K2).
0x0004	7 - 0	Debounced_S1	0x0	Debounced value of S1 nibbles.

Table 31: TOH Monitor Events/Defects (T_TOH_MONITOR_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	SignalDetect	0x1	SignalDetect from optical transceiver. SignalDetect is active high. (this is LINERXSIGDET when SignalDetect_ActiveLow is 0x0 and not LINERXSIGDET when SignalDetect_ActiveLow is 0x1).
	1	OOF	0x1	Out Of Frame.
	2	LOF	0x1	Loss Of Frame.
	3	LOS	0x1	Loss Of Signal. It is recommended to use the LINERXSIGDETx lead for LOS detection since some fiber optic modules output noise during LOS.
	4	RSOHM_CI_SSF	0x1	Incoming SSF on RSOH Monitor.
	5	B1_Error	0x1	B1 BIP Error.
	6	TIM	0x1	Trail Identifier Mismatch.
	7	MSOHM_CI_SSF	0x1	Incoming SSF on MSOH Monitor.
	8	DEG	0x1	Degraded signal.
	9	EXC	0x1	Excessive error.
	10	RDI	0x1	Remote Defect Indication.
	11	AIS	0x1	Line AIS detected on K2.
	12	SF	0x1	Signal Fail.
	13	K1K2_Event	0x1	New (debounced) K1K2 value accepted.
	14	S1_Event	0x1	New (debounced) S1 value accepted.

Table 32: TOH Monitor APS Events/Defects (T_TOH_MONITOR_APS_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	DEG	0x1	Signal Degrade.
	1	SF	0x1	Signal Fail.
	2	K1K2_Event	0x1	New K1K2 value accepted.

Table 33: TOH Monitor Configuration (T_TOH_MONITOR_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	General_Config			
	0	B1_BIP_PerformanceCounter_BitCount	0x0	B1 BER performance counter reports bit errors when 0x1, block errors when 0x0.
	1	REI_BIP_PerformanceCounter_BitCount	0x0	REI BIP performance counter reports bit errors when 0x1, block counter when 0x0.
	2	SignalDetect_ActiveLow	0x0	SignalDetect input from transceiver (LINERXSIGDET) is active low when 0x1, active high when 0x0.
	3	LOS_Detection_Disable	0x0	LOS detection is disabled when 0x1.
	4	Descrambler_Disable	0x0	Descrambling is disabled when 0x1. Descrambling must be enabled in normal operation.
	5	Debounce_K2_LSB_Separately	0x1	Debouncing of K1/K2 bytes: The three least significant bits of K2 are debounced separately when 0x1. All sixteen bits are debounced when 0x0.
	6	SignalDetect_LOF_Inhibit_Disable	0x1	Inhibition of LOF by SignalDetect is disabled when 0x1.
	7	LOS_LOF_Inhibit_Disable	0x0	Inhibition of LOF by LOS is disabled when 0x1.
	8	SSF_AIS_Inhibit_Disable	0x0	Inhibition of K2 Line AIS by incoming SSF is disabled when 0x1.
0x0002		TTI_Config		T_TOH_MONITOR_TTI_Config (See page 211.) TTI Configuration.
0x0006		B2_Config		T_TOH_MONITOR_BIP_Detector_Config (See page 211.) Configuration for B2 DEG/EXC detection.
0x0022	AIS_RDI_Config			
	0	AIS_RDI_Insert_Disable	0x0	Insertion of RDI on K2 Line AIS is disabled when 0x1.
	1	SSF_RDI_Insert_Disable	0x0	Insertion of RDI on SSF (incoming SSF in MSOH Monitor) is disabled when 0x1.
	2	EXC_RDI_Insert_Disable	0x0	Insertion of RDI on EXC is disabled when 0x1.
	3	SignalDetect_AIS_Insert_Disable	0x1	Insertion of Line AIS on SignalDetect is disabled when 0x1.
	4	LOS_AIS_Insert_Disable	0x0	Insertion of Line AIS on LOS defect detected in the A1/A2 Framer is disabled when 0x1.
	5	LOF_AIS_Insert_Disable	0x0	Insertion of Line AIS on LOF defect is disabled when 0x1.
	6	TIM_AIS_Insert_Disable	0x0	Insertion of Line AIS on TIM defect is disabled when 0x1.
	7	AIS_AIS_Insert_Disable	0x0	Insertion of Line AIS on K2 line AIS detection is disabled when 0x1.
	8	SSF_AIS_Insert_Disable	0x0	Insertion of Line AIS on SSF (incoming SSF in MSOH Monitor) is disabled when 0x1.
	9	EXC_AIS_Insert_Disable	0x0	Insertion of Line AIS on B2 EXC defect is disabled when 0x1.
	10	Framer_AIS_Force	0x0	Forces Line AIS insertion after Framing when 0x1.
	11	RSOH_AIS_Force	0x0	Forces Line AIS insertion after Regenerator Section Overhead Monitoring when 0x1.
	12	MSOH_AIS_Force	0x0	Forces Line AIS insertion after Multiplex Section Overhead Monitoring when 0x1.

Table 34: J0 TTI Configuration (T_TOH_MONITOR_TTI_Config)

Offset	Bits	Name	Init	Description
0x0000	Config			
	0	TIM_Enable	0x0	TIM detection is enabled when 0x1.
	1	NonSpecificMessage	0x0	Ignore expected TTI message and assume non-specific repeating byte message when 0x1. When 0x0 the TTI message has to match the specified expected message (16 byte TTI message or repeating specific byte message).
0x0002	Counters			
	3 - 0	MultiFramesToSet_TIM	0x5	Range 2 to 15 Number of multiframes to set TIM alarm.
	7 - 4	MultiFramesToReset_TIM	0x3	Range 2 to 15 Number of multiframes to reset TIM alarm.

Table 35: Section BER Detection Configuration (T_TOH_MONITOR_BIP_Detector_Config)

Offset	Bits	Name	Init	Description
0x0000	0	PoissonErrorCheck	0x0	Assume Poisson error distribution when 0x1, bursty distribution when 0x0.
0x0002		PoissonDetector_Config		T_BIP_PoissonDetector_Config (See page 211.) Configuration for DEG/EXC detection, assuming Poisson distribution of errors.
0x0014		BurstyDetector_Config		T_Line_BIP_BurstyDetector_Config (See page 212.) Configuration for DEG detection, assuming bursty distribution of errors.

Table 36: Poisson Distribution BER Detection (T_BIP_PoissonDetector_Config)

Offset	Bits	Name	Init	Description
0x0000	PoissonCommon_Config			
	0	DEG_Use125usCounter	0x0	Use 125 us interval length for DEG detection when 0x1, otherwise 500 us interval length.
	1	EXC_Use125usCounter	0x0	Use 125 us interval length for EXC detection when 0x1, otherwise 500 us interval length.
	2	BurstProtection	0x0	Enables Burst Protection when 0x1.
0x0002	15 - 0	DEG_DetectionErrorThreshold	0xFFFF	Range 1 to 65535 Minimum number of bit errors within a window for DEG detection.
0x0004	15 - 0	DEG_DetectionWindowSize	0xFFFF	Range 1 to 65535 Window size for DEG detection in 125/500 us intervals.
0x0006	15 - 0	DEG_RecoveryErrorThreshold	0xFFFF	Range 1 to 65535 Allowed number of bit errors within a window for DEG recovery (error threshold for which the DEG state will not be exited).
0x0008	15 - 0	DEG_RecoveryWindowSize	0x1	Range 1 to 65535 Window size for DEG recovery in 125/500 us intervals.

Table 36: Poisson Distribution BER Detection (T_BIP_PoissonDetector_Config) (cont.)

Offset	Bits	Name	Init	Description
0x000A	15 - 0	EXC_DetectionErrorThreshold	0xFFFF	Range 1 to 65535 Minimum number of bit errors within a window for EXC detection.
0x000C	15 - 0	EXC_DetectionWindowSize	0xFFFF	Range 1 to 65535 Window size for EXC detection in 125/500 us intervals.
0x000E	15 - 0	EXC_RecoveryErrorThreshold	0xFFFF	Range 1 to 65535 Maximum allowed number of bit errors within a window for EXC recovery (error threshold for which the EXC state will not be exited).
0x0010	15 - 0	EXC_RecoveryWindowSize	0x1	Range 1 to 65535 Window size for EXC recovery in 125/500 us intervals.

Table 37: Section Bursty Distribution BER Detection (T_Line_BIP_BurstyDetector_Config)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	DEG_DetectionErrorThreshold_LSB	0xFFFF	Integer range 0 to 768000 (two addresses) Least significant bits of Detection Error Threshold. An (one second) interval is bad if the number of detected errored bits in that interval is greater than or equal to this threshold.
0x0002	Detection_Config			
	3 - 0	DEG_DetectionWindowSize	0xA	Range 2 to 10 Number of consecutive bad intervals before DEG is declared.
	7 - 4	DEG_DetectionErrorThreshold_MSB	0xF	Integer range 0 to 768000 (two addresses) Most significant bits of Detection Error Threshold. An (one second) interval is bad if the number of detected errored bits in that interval is greater than or equal to this threshold.
0x0004	15 - 0	DEG_RecoveryErrorThreshold_LSB	0xFFFF	Range 0 to 768000 (two addresses) Least significant bits of Recovery Error Threshold. An (one second) interval is a good interval when the number of errored bits in this interval does not exceed this threshold.
0x0006	Recovery_Config			
	3 - 0	DEG_RecoveryWindowSize	0x2	Range 2 to 10 Number of consecutive good intervals before DEG is cleared.
	7 - 4	DEG_RecoveryErrorThreshold_MSB	0xF	Range 0 to 768000 (two addresses) Most significant bits of Recovery Error Threshold. An (one second) interval is a good interval when the number of errored bits in this interval does not exceed this threshold.

8.10 TOH GENERATOR

Table 38: TOH Generator (T_TOH_GENERATOR)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_TOHG_Common_Config (See page 214.) General configuration.
0x0100		Line_Config		rw	Array (4) of T_TOHG_Line_Config (See page 214.) Offset between two elements = 0x8. Array index indicates the line (= line number - 1). Configuration.
0x0200		TTI_Contents	All 0x0	rw	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. This array contains the TTI sequence for the four lines: • bytes 0-15: TTI message for line 1 • bytes 16-31: TTI message for line 2 • bytes 32-47: TTI message for line 3 • bytes 48-63: TTI message for line 4 Note: Bytes 16 to 63 are not used in STM-4 mode.
0x0400		TOH_Contents	See desc.	rw	Array (324) of nine_bits Offset between two elements = 0x2. Array index indicates the TOH byte number. This array contains the TOH for a single STM-4 or 4 times STM-1. Each TOH byte is represented by a nine bit word. The most significant bit determines the source of the corresponding byte (0x0 = internal memory, 0x1 = TOH Port Interface). This way of determining the source of a byte is the default behavior. For certain bytes (DCC-bytes, M1, K1, K2), other sources than internal memory or TOH-Port can be selected by extra settings which override this default behavior. The least significant byte contains the byte value when this bytes has to be inserted from memory. The order in which bytes are mapped in memory is the same order as these bytes appear in the TOH. For STM-1 mode the columns are byte interleaved: column #1 corresponds to line 1, column 2 to line 2, etc. The byte number can easily be calculated as follows: byte number = (a-1)x36 + (b-1)x4 + c-1 where • a = row number (1 to 3, 5 to 9), • b = multi-column number (1 to 9), • c, for STM-4 mode = depth of the interleave within the multi-column (1-4), • c, for STM-1 mode = line number (1-4). See also [ITU-T G.707/Y.1322] for the TOH bytes locations. Note 1: Space is also reserved for the administrative Unit Pointer bytes (a = 4) but these bytes are not used. Note 2: K1/K2 can not be sourced from this internal memory. Separate sixteen bit registers are provided for these bytes to guarantee that K1 and K2 are kept together. Note 3: B1 and B2 byte locations serve as an error mask which will be EXORed with the calculated BIP. These locations must be 0x00 for normal operation. Note 4: A1 bytes (bytes 0-11) are initialized to 0xF6, A2 bytes (bytes 12-23) are initialized to 0x28. All other entries are initialized to 0x00.

Table 39: Transmit TOH Port Configuration (T_TOHG_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	TOH_Port_Enable	0x0	Enables TX side TOH port when 0x1.

Table 40: TOH Configuration (T_TOHG_Line_Config)

Offset	Bits	Name	Init	Description
0x0000	Sources			
	0	RSOH_DCC_Select	0x0	Select mode for DCC port. The DCC port requests RS DCC bytes (D1-D3) when 0x1 and MS DCC bytes (D4-D12) when 0x0. Only valid when DCC port is enabled.
	1	DCC_Port_Enable	0x0	The DCC port is enabled when 0x1 and RSOH_DCC_Port_Select setting determines which set of DCC bytes will be filled in from the DCC port (RS DCC or MS DCC). For the other set, default behavior applies (see TOH_Contents). Default behavior applies both for RSOH and MSOH DCC bytes when 0x0.
	2	REI_Ring_Port_Enable	0x1	REI, in M1. M1 contents is taken from Ring Port when 0x1, default behavior applies when 0x0.
	4 - 3	K1K2_Source	0x0	Source for K1 and K2 bytes: • 0x0 = Register • 0x1 = TOH Port • 0x2 = Rx APS • 0x3 = Reserved
	6 - 5	RDI_Source	0x2	Source for RDI, in K2 (b6-b8). • 0x0 = Register • 0x1 = TOH Port • 0x2 = Ring Port • 0x3 = None
0x0002	15 - 0	K1K2_Value	0x0	Values for K1 and K2 bytes, used when Source is Register. K1 is least significant byte, K2 is most significant byte.
0x0004	2 - 0	RDI_Value	0x0	RDI value used to overwrite b6-b8 of K2 when RDI Source = Register.
0x0006	0	Scrambling_Disable	0x0	Scrambling is disabled when 0x1. Scrambling must be enabled in normal operation.

8.11 TOH AND DCC PORT

Table 41: Receive TOH and DCC Port (T_RX_TOH_DCC_PORT)

Offset	Bits	Name	Init	Access	Description
0x0000		TOH_Events_Mask	All 0x1	rw	Array (36) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH byte events. Masks for the corresponding events. Refer to TOH_Events_LatchForInt descriptions for the layout of the bits.
0x0200		Common_Config		rw	T_RXTDP_Common_Config (See page 217.) General configuration.
0x0240		Line_Config		rw	Array (4) of T_RXTDP_Line_Config (See page 217.) Offset between two elements = 0x2. Array index indicates the line (= line number - 1). DCC port configuration.
0x0280		TOH_Events_Summary	All 0x0	ro	Array (4) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH_Events_LatchedForInt bits. Each bit corresponds to the summary of one entry in TOH_Events_LatchForInt. Each entry of this array corresponds to the summaries of all TOH byte events for the bytes with the same interleave depth (STM-4 mode), or with the same line number (STM-1 mode). The array index and the bit position can be calculated as follows: Array index = c-1 The correlation between bit position and TOH_Events_LatchForInt entry is as follows: A bit p corresponds to the summary of TOH Events entry (px4) + c. where • a = row number (1 to 9), • b = multi-column number (1 to 9), • c, for STM-4 mode = depth of the interleave within the multi-column (1-4), • c, for STM-1 mode = line number (1-4). • p = bit position (0 to 8, least significant bit is 0) See also [ITU-T G.707/Y.1322] for the TOH bytes locations.

Table 41: Receive TOH and DCC Port (T_RX_TOH_DCC_PORT) (cont.)

Offset	Bits	Name	Init	Access	Description
0x02C0		TOH_Events_Summary_Mask	All 0x1	rw	Array (4) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH_Events_LatchedForInt bits. Summary mask of TOH Events. Refer to TOH_Events_Summary descriptions for the layout of the bits.
0x0300		TOH_Events_LatchForInt	All 0x0	cow_1	Array (36) of nine_bits Offset between two elements = 0x2. Array index indicates the summary of nine TOH byte events. Latched events on TOH bytes. Events occur if the TOH byte content has a different value as the one in the previous frame. The array index and the bit position within the corresponding entry can be calculated as follows: Array index = (a-1)x4 + c-1 Bit position = b-1 where • a = row number (1 to 9), • b = multi-column number (1 to 9), • c, for STM-4 mode = depth of the interleave within the multi-column (1-4), • c, for STM-1 mode = line number (1-4). See also [ITU-T G.707/Y.1322] for the TOH bytes locations.
0x0400		TOH_Contents	All 0x0	ro	Array (324) of byte Offset between two elements = 0x2. Array index indicates the TOH byte number. Received TOH bytes (raw, unprocessed values, except B1/B2). The order in which bytes are mapped in memory is the same order as these bytes appear in the TOH. For STM-1 mode the columns are byte interleaved: column #1 corresponds to line 1, column 2 to line 2, etc. The byte number can easily be calculated as follows: byte number = (a-1)x36 + (b-1)x4 + c-1 where • a = row number (1 to 9), • b = multi-column number (1 to 9), • c, for STM-4 mode = depth of the interleave within the multi-column (1-4), • c, for STM-1 mode = line number (1-4). See also [ITU-T G.707/Y.1322] for the TOH bytes locations. Note: B1 and B2 locations contain the EXOR of the calculated BIP with the received BIP.

Table 42: Receive TOH Port Configuration (T_RXTDP_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	TOH_Port_Enable	0x0	TOH Port is enabled when 0x1.

Table 43: Receive DCC Port Configuration (T_RXTDP_Line_Config)

Offset	Bits	Name	Init	Description
0x0000	0	RSOH_DCC_Select	0x0	Select mode for DCC port. The DCC port sends RS DCC bytes (D1-D3) when 0x1 and MS DCC bytes (D4-D12) when 0x0. Only valid when the DCC port is enabled.
	1	DCC_Port_Enable	0x0	The DCC port is enabled when 0x1 and the RSOH_DCC_Port_Select setting determines which set of DCC bytes will be sent out on the DCC port (RS DCC or MS DCC).

8.12 HIGH ORDER POINTER TRACKER AND RETIMER

Table 44: Pointer Tracker and Retimer (T_HO_PTR_RETIMER)

Offset	Bits	Name	Init	Access	Description
0x0000	0	DetectedConcat_Event_Mask	0x1	rw	Detected Concatenation event mask.
0x0040	0	DetectedConcat_Event_LatchForInt	0x0	cow_1	Detected Concatenation event latched for interrupt.
0x0080		CorrDefects_SummaryMask		rw	T_HOPTRRT_Defects_Summary (See page 218.) Summary mask.
0x00C0		CorrDefects_Summary		ro	T_HOPTRRT_Defects_Summary (See page 218.) Summary.
0x0100		Reserved	0x0	ro	Reserved.
0x0140		Reserved	0x0	ro	Reserved.
0x0180		Common_Config		rw	T_HOPTRRT_Common_Config (See page 218.) General configuration.
0x01C0		AUG1_Mode_Config		rw	T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration.
0x01E0	11 - 0	DetectedConcat	0x0	ro	Detected concatenation in the Pointer Tracker. A '1' means a concatenation indication (Y1*) has been detected on the pointer bytes of the corresponding timeslot (least significant bit corresponds to the first timeslot).
0x0200		VCx			Array (12) of T_HOPTRRT_VCx (See page 218.) Offset between two elements = 0x20. Array index indicates the high order path. Configuration and status.

Table 45: Pointer Tracker and Retimer Defect/Event Summary (T_HOPTRRT_Defects_Summary)

Offset	Bits	Name	Init	Description
0x0000	11 - 0	Summary	0xFFF	Defects summary, one bit per high order path. Least significant bit corresponds to the first high order path.
	12	DetectedConcat_Event	0x1	Event telling detected concatenation has changed.

Table 46: Pointer Tracker and Retimer Common Configuration (T_HOPTRRT_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	AIS_Config			
	0	AU_AIS_AIS_Insert_Disable	0x0	Insertion of AU AIS on AU AIS detection by the Pointer Tracker is disabled when 0x1.
	1	LOP_AIS_Insert_Disable	0x0	Insertion of AU AIS on Loss Of Pointer is disabled when 0x1 by the Pointer Tracker.
	2	TSF_AIS_Insert_Disable	0x0	Insertion of AU AIS on TSF is disabled when 0x1.
	3	FifoError_AIS_Insert_Disable	0x0	Insertion of AU AIS on a FIFO Error is disabled when 0x1.
0x0002	0	Reserved	0x0	Reserved.

Table 47: Pointer Tracker and Retimer Per Path (T_HOPTRRT_VCx)

Offset	Bits	Name	Init	Access	Description
0x0000		VC3_TUG3_Config		rw	T_HOPTRRT_VC3_TUG3_Config (See page 219.) Per VC-3/TUG-3 configuration.
0x0006		VCx_Status		ro	T_HOPTR_VCx_Status (See page 219.) Pointer Tracker Status.
0x0008		PerfCounters_Shadow		ro	T_HOPTRRT_PerfCounters (See page 219.) Performance counters.
0x000C		CorrDefects_Mask		rw	T_HOPTRRT_Defects (See page 219.) Correlated defects mask.
0x000E		CorrDefects_Unlatched		ro	T_HOPTRRT_Defects (See page 219.) Correlated defects.
0x0010		CorrDefects_LatchForInt		cow_1	T_HOPTRRT_Defects (See page 219.) Correlated defects latched for interrupt.
0x0012		Reserved	0x0	cow_1	Reserved.
0x0014		Reserved	0x0	ro	Reserved.
0x0016		Reserved	0x0	ro	Reserved.

Table 48: Pointer Tracker and Retimer Path Configuration (T_HOPTRRT_VC3_TUG3_Config)

Offset	Bits	Name	Init	Description
0x0000	General_Config			
	0	AIS_Force	0x0	Insertion of AU AIS (after the Retimer) is forced when 0x1.
	2 - 1	SS_bits	0x2	SS bits to be used in the Pointer Generator.
0x0002	15 - 0	SlowLeakRegister	0x10	Slow Leak Register (see Section 2.17).
0x0004	15 - 0	FastLeakRegister	0x10	Fast Leak Register (see Section 2.17).

Table 49: Pointer Tracker Path Status (T_HOPTR_VCx_Status)

Offset	Bits	Name	Init	Description
0x0000	1 - 0	Reported_SS_Bits	0x0	Received SS bits reported by the Pointer Tracker.

Table 50: Pointer Justification Counters (T_HOPTRRT_PerfCounters)

Offset	Bits	Name	Init	Description
0x0000	IncomingJustifications			
	7 - 0	Incoming_PJ	0x0	Range 0 to 0xFE Positive Justifications as counted by the Pointer Tracker.
	15 - 8	Incoming_NJ	0x0	Range 0 to 0xFE Negative Justifications as counted by the Pointer Tracker.
0x0002	OutgoingJustifications			
	7 - 0	Outgoing_PJ	0x0	Range 0 to 0xFE Positive Justifications as generated by the Pointer Generator.
	15 - 8	Outgoing_NJ	0x0	Range 0 to 0xFE Negative Justifications as generated by the Pointer Generator.

Table 51: Pointer Tracker and Retimer Defects (T_HOPTRRT_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	AIS	0x1	AIS, detected by the Pointer Tracker.
	1	LOP	0x1	Loss of Pointer.
	2	Fifo_Error	0x1	Retimer FIFO Error.

8.13 POS/ATM DEMAPPER

Table 52: POS/ATM Demapper (T_POS_ATM_DEMAPPER)

Offset	Bits	Name	Init	Access	Description
0x0000		DefectsAndCounters			Array (12) of T_DMP_DefectsAndCounters (See page 220.) Offset between two elements = 0x20. Array index indicates the PHY. Fields related to defects and performance counters.
0x0400	7 - 0	EgressFIFO_Reset	0x0	rw	Microprocessor Controlled Reset for the Egress FIFO. Writing the value 0x91 to this register generates a Soft Reset for the Egress FIFO. Reset is active as long as this register contains the value 0x91.
0x0440		AUG1_Mode_Config		rw	T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration.
0x0480	11 - 0	CorrDefects_Summary	0x0	ro	Defects summary, one bit per PHY. Least significant bit corresponds to the first PHY.
0x04C0	11 - 0	CorrDefects_SummaryMask	0xFFF	rw	Defects summary mask, one bit per PHY. Least significant bit corresponds to the first PHY.
0x0500		Common_Config		rw	T_DMP_Common_Config (See page 222.) General configuration.
0x0600		Phy_Config		rw	Array (12) of T_DMP_Phy_Config (See page 222.) Offset between two elements = 0x20. Array index indicates the PHY. PHY Configuration.

Table 53: POS/ATM Demapper Per PHY (T_DMP_DefectsAndCounters)

Offset	Bits	Name	Init	Access	Description
0x0000		CorrDefects_Unlatched		ro	T_DMP_Defects (See page 221.) Defects.
0x0002		CorrDefects_LatchForInt		cow_1	T_DMP_Defects (See page 221.) Defects latched for interrupt.
0x0004		CorrDefects_Mask		rw	T_DMP_Defects (See page 221.) Defects mask.
0x0006		PerfCounters_Shadow		ro/cor	T_DMP_PerfCounters (See page 221.) Performance counters. Note: In case the one second performance monitoring mechanism is enabled, the access type is read-only, otherwise it is clear-on-read.

Table 54: POS/ATM Demapper Defects (T_DMP_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	OCD	0x1	Out of Cell Delineation. Applies to ATM mode only.
	1	LCD	0x1	Loss of Cell Delineation. Applies to ATM mode only.
	2	Overflow	0x1	Rx FIFO overflow condition. Applies to both ATM and PPP mode.

Table 55: POS/ATM Demapper Performance Counters (T_DMP_PerfCounters)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	FrameToFifoCounter_LSBytes	0x0	Number of cells / packets forwarded to Rx FIFO (2 LSBytes of the 24 bit counter). Applies to both ATM and PPP mode.
0x0002	7 - 0	FrameToFifoCounter_MSByte	0x0	Number of cells / packets forwarded to Rx FIFO (MSByte of the 24 bit counter). Applies to both ATM and PPP mode.
0x0004	15 - 0	CellFilteredCounter_LSBytes	0x0	Number of cells discarded due to cell filtering (2 LSBytes of the 24 bit counter). Discards due to HEC errors are not counted. Applies to ATM mode only.
0x0006	7 - 0	CellFilteredCounter_MSByte	0x0	Number of cells discarded due to cell filtering (MSByte of the 24 bit counter). Discards due to HEC errors are not counted. Applies to ATM mode only.
0x0008	15 - 0	CorrHECErrorCounter	0x0	Number of cells with corrected HEC error. Applies to ATM mode only.
0x000A	15 - 0	UncorrHECErrorCounter	0x0	Number of cells with uncorrected HEC error. Applies to ATM mode only.
0x000C	15 - 0	OverflowCounter	0x0	Number of cells / packets discarded due to Rx FIFO overflow. Applies to both ATM and PPP mode.
0x000E	7 - 0	FrameDiscardedCounter	0x0	Number of frames with an abort sequence (0x7D7E) or mismatched Address / Control fields. Applies to PPP (no transparent) mode only.
0x0010	7 - 0	MaxFrameLengthCounter	0x0	Number of frames longer than the maximum frame length. Applies to PPP (no transparent) mode only.
0x0012	7 - 0	MinFrameLengthCounter	0x0	Number of frames shorter than the minimum frame length. Applies to PPP (no transparent) mode only.

Table 56: POS/ATM Demapper Common Configuration (T_DMP_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	OneSecondPM_Enable	0x0	One second performance monitoring mechanism is enabled when 0x1, otherwise clear-on-read performance monitoring mechanism is enabled. Applies to both ATM and PPP modes.
0x0002	2 - 0	LCD_Time	0x4	Loss of Cell Delineation (LCD) integration time in ms. Applies to ATM mode only.
0x0004	7 - 0	Threshold	0x1B	Range 5 to 128 The minimum number of free words which has to be available in the FIFO before the POS/ATM Demapper starts writing data to that FIFO. This value must always be larger than 4. Applies to PPP mode only, for ATM mode this must always be set to 27 (0x1B).
0x0006	7 - 0	MinimumFrameLength	0x0	Range 0 to 255 Minimum Frame Length. Applies to PPP (no transparent) mode only.
0x0008	15 - 0	MaximumFrameLength	0xFFFF	Range 0 to 65535 Maximum Frame Length. Applies to PPP (no transparent) mode only.
0x000A	1 - 0	FragmentSize	0x0	0x0 = SIZE_64 0x1 = SIZE_128 0x2 = SIZE_256 0x3 = SIZE_1024 Size of each fixed-length POS-PHY packet (in bytes). Applies to PPP (transparent) mode only.

Table 57: POS/ATM Demapper PHY Configuration (T_DMP_Phy_Config)

Offset	Bits	Name	Init	Description
0x0000	General			
	0	Phy_Enable	0x0	Enables demapping for this PHY when 0x1. Applies to both ATM and PPP mode.
	1	Descrambling_Disable	0x0	Disables descrambling when 0x1. Applies to both ATM and PPP mode. Note for ATM it is mandatory to enable descrambling in normal operation.
0x0002	Thresholds			
	3 - 0	Alpha	0x7	Range 1 to 15 Threshold for leaving SYNC-state. Its value must be set to a value different from 0. Applies to ATM mode only.
	7 - 4	Delta	0x6	Range 1 to 15 Threshold for entering SYNC-state. Its value must be set to a value different from 0. Applies to ATM mode only.

Table 57: POS/ATM Demapper PHY Configuration (T_DMP_Phy_Config) (cont.)

Offset	Bits	Name	Init	Description
0x0004	HEC			
	7 - 0	Coset	0x55	HEC offset (coset) pattern. Applies to ATM mode only.
	8	HEC_Corr_Enable	0x1	Enables single bit HEC error correction when 0x1. Applies to ATM mode only.
	9	HEC_Detect_Enable	0x1	Enables transition from Detection to Correction state while in SYNC when 0x1. When disabled, single-bit HEC errors in consecutive cells are all corrected. Applies to ATM mode only.
0x0006	Filtering			
	0	MatchCellFilt_Enable	0x0	Enables cell filtering (discard) for matched cells when 0x1. Applies to ATM mode only.
	1	IdleCellFilt_Enable	0x1	Enables cell filtering (discard) for idle cells (ITU-T I.432) when 0x1. Applies to ATM mode only.
	2	UnasCellFilt_Enable	0x1	Enables cell filtering (discard) for unassigned cells (ITU-T I.361) when 0x1. Applies to ATM mode only.
	3	UnCorCellFilt_Enable	0x1	Enables cell filtering (discard) for cells with uncorrected HEC when 0x1. Applies to ATM mode only.
0x0008	11 - 0	HeaderPattern_GFC_VPI	0x0	The GFC and the VPI field of a UNI cell or the VPI field of a NNI cell for the match header pattern. Applies to ATM mode only.
0x000A	15 - 0	HeaderPattern_VCI	0x0	The VCI field for the match header pattern. Applies to ATM mode only.
0x000C	Pattern_LastWord			
	7 - 0	Reserved	0x0	Reserved.
	8	HeaderPattern_CLP	0x0	The CLP field for the match header pattern. Applies to ATM mode only.
	11 - 9	HeaderPattern_PTI	0x0	The PTI field for the match header pattern. Applies to ATM mode only.
0x000E	11 - 0	HeaderMask_GFC_VPI	0x0	The GFC and the VPI field of a UNI cell or the VPI field of a NNI cell for the match header mask. Applies to ATM mode only.
0x0010	15 - 0	HeaderMask_VCI	0x0	The VCI field for the match header mask. Applies to ATM mode only.
0x0012	Mask_LastWord			
	7 - 0	Reserved	0x0	Reserved.
	8	HeaderMask_CLP	0x0	The CLP field for the match header mask. Applies to ATM mode only.
	11 - 9	HeaderMask_PTI	0x0	The PTI field for the match header mask. Applies to ATM mode only.

Table 57: POS/ATM Demapper PHY Configuration (T_DMP_Phy_Config) (cont.)

Offset	Bits	Name	Init	Description
0x0014	PPP			
	0	TransparentMode	0x0	Enables transparent mode when 0x1. In transparent mode the HDLC functionality is bypassed, i.e., all bytes are passed through transparently (no framing, no byte destuffing, no abort detection, no FCS processing). Applies to PPP mode only.
	1	CheckHeader_Enable	0x1	Enables Address and Control fields check when 0x1. When enabled, packets of which the address field is not equal to 0xFF and/or the Control field is not equal to 0x03 are filtered (discarded). Applies to PPP (no transparent) mode only.
	2	StripHeader_Enable	0x1	Enables Address and Control fields stripping when 0x1. Applies to PPP (no transparent) mode only.
	3	CheckFCS_Enable	0x1	Enables FCS check when 0x1. When disabled, all consequent actions (status, counters, interrupt generation and signaling on POS-PHY interface) are also disabled. Applies to PPP (no transparent) mode only.
	4	StripFCS_Enable	0x1	Enables FCS stripping when 0x1. Applies to PPP (no transparent) mode only.
	5	FCS32_Enable	0x1	32 bit FCS size when 0x1, 16 bit FCS size otherwise. Applies to PPP (no transparent) mode only.

8.14 POS/ATM MAPPER

Table 58: POS/ATM Mapper (T_POS_ATM_MAPPER)

Offset	Bits	Name	Init	Access	Description
0x0000		PerfCounters_Shadow		ro/cor	Array (12) of T_MAP_PerfCounters (See page 225.) Offset between two elements = 0x10. Array index indicates the PHY. Performance counters. Note: In case the one second performance monitoring mechanism is enabled, the access type is read-only, otherwise it is clear-on-read.
0x0200	11 - 0	CorrDefects_Mask	0xFFF	rw	Defects mask. See CorrDefects_Unlatched. Applies to PPP mode only.
0x0240		Common_Config		rw	T_MAP_Common_Config (See page 226.) General configuration.
0x0280	7 - 0	IngressFIFO_Reset	0x0	rw	Microprocessor Controlled Reset for the Ingress FIFO. Writing the value 0x91 to this register generates a Soft Reset for the Ingress FIFO. Reset is active as long as this register contains the value 0x91.
0x02A0		AUG1_Mode_Config		rw	T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration.

Table 58: POS/ATM Mapper (T_POS_ATM_MAPPER) (cont.)

Offset	Bits	Name	Init	Access	Description
0x02C0	11 - 0	CorrDefects_Unlatched	0x0	ro	Defects, one bit per PHY. If one of the bits becomes equal to 0x1, an underflow occurs in the Tx FIFO corresponding to that bit while a packet is being transmitted. Least significant bit corresponds to the first PHY. The least significant bit of this field corresponds to PPP stream number 0. Applies to PPP mode only.
0x02E0	11 - 0	CorrDefects_LatchForInt	0x0	cow_1	Defects latched for interrupt. See CorrDefects_Unlatched. Applies to PPP mode only.
0x0300		Phy_Config		rw	Array (12) of T_MAP_Phy_Config (See page 226.) Offset between two elements = 0x10. Array index indicates the PHY. PHY Configuration.

Table 59: POS/ATM Mapper Performance Counters (T_MAP_PerfCounters)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	FrameFromFifoCounter_LSBytes	0x0	Number of good cells / packets received from Tx FIFO (2 LSBytes of the 24 bit counter). Applies to both ATM and PPP mode.
0x0002	7 - 0	FrameFromFifoCounter_MSByte	0x0	Number of good cells / packets received from Tx FIFO (MSByte of the 24 bit counter). Applies to both ATM and PPP mode.
0x0004	15 - 0	IdleCellInsertCounter_LSBytes	0x0	Number of cells inserted (2 LSBytes of the 24 bit counter). Applies to ATM mode only.
0x0006	7 - 0	IdleCellInsertCounter_MSByte	0x0	Number of cells inserted (MSByte of the 24 bit counter). Applies to ATM mode only.
0x0008	7 - 0	HEC_ErrorCounter	0x0	Number of corrupted cells received from Tx FIFO. Applies to ATM mode only.
0x000A	7 - 0	UnderflowCounter	0x0	Number of frames affected by a TX FIFO underflow (= number of frames for which a TX FIFO underflow occurs while the frame is being transmitted). Applies to PPP mode only.
0x000C	7 - 0	ErroredPacketCounter	0x0	Number of packets for which the error signal on the POS-PHY Level 2 interface was asserted during the last word transfer of that packet. Applies to PPP mode only.

Table 60: POS/ATM Mapper Common Configuration (T_MAP_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	OneSecondPM_Enable	0x0	One second performance monitoring mechanism is enabled when 0x1, otherwise clear-on-read performance monitoring mechanism is enabled. Applies to both ATM and PPP mode.
0x0002	7 - 0	Threshold	0x1B	Range 1 to 128 The minimum number of words which has to be available in the FIFO before the POS/ATM Mapper starts to read data from that FIFO. This value must always be larger than 0. Applies to PPP mode only, for ATM mode this must always be set to 27 (0x1B).

Table 61: POS/ATM Mapper PHY Configuration (T_MAP_Phy_Config)

Offset	Bits	Name	Init	Description
0x0000	General			
	0	Phy_Enable	0x0	Enables mapping for this PHY when 0x1. Applies to both ATM and PPP mode.
	1	Scrambling_Disable	0x0	Disables scrambling when 0x1. Applies to both ATM and PPP mode. Note for ATM it is mandatory to enable scrambling in normal operation.
0x0002	HEC			
	7 - 0	Coset	0x55	HEC offset (coset) pattern. Applies to ATM mode only.
	8	HEC_ATMlayer_Enable	0x0	Enables insertion of calculated HEC for ATM layer cells when 0x1. Applies to ATM mode only.
	9	HEC_IdleUnas_Enable	0x0	Enables insertion of calculated HEC for inserted cells when 0x1. Use the HEC byte in the 5 bytes header value setting when 0x0. Applies to ATM mode only.
0x0004	HEC_Manip			
	7 - 0	HEC_CorruptionMask_XOR	0x0	HEC corruption mask: The HEC is EXORed with this mask. Set to default value for normal operation. Applies to ATM mode only.
	9 - 8	HEC_Manipulation	0x0	0x0 = NO_MANIP 0x1 = XOR_HEC 0x2 = AND_HEC 0x3 = OR_HEC HEC / UDF1 manipulation. Set to the default value for normal operation. Applies to ATM mode only.
0x0006	11 - 0	HeaderPattern_GFC_VPI	0x0	The GFC and the VPI field of a UNI cell or the VPI field of a NNI cell for cell insertion. Applies to ATM mode only.

Table 61: POS/ATM Mapper PHY Configuration (T_MAP_Phy_Config) (cont.)

Offset	Bits	Name	Init	Description
0x0008	15 - 0	HeaderPattern_VCI	0x0	The VCI field for cell insertion. Applies to ATM mode only.
0x000A	Pattern_LastWord			
	7 - 0	HeaderPattern_HEC	0x52	The HEC field for cell insertion. Applies to ATM mode only.
	8	HeaderPattern_CLP	0x1	The CLP field for cell insertion. Applies to ATM mode only.
	11 - 9	HeaderPattern_PTI	0x0	The PTI field for cell insertion. Applies to ATM mode only.
0x000C	IdleCell			
	7 - 0	PayloadValue	0x6A	Payload value for cell insertion. Applies to ATM mode only.
	9 - 8	PayloadMode	0x0	0x0 = FIXED_VALUE 0x1 = INC_EACH_BYTE 0x2 = INC_EACH_BYTE_ACROSS_CELL 0x3 = INC_EACH_CELL Payload mode for cell insertion. The following modes are supported: • FIXED_VALUE: fixed to configured payload value • INC_EACH_BYTE: incremented each byte and start each cell with the configured payload value • INC_EACH_BYTE_ACROSS_CELL: incremented each byte and cross cell boundaries • INC_EACH_CELL: incremented each cell Applies to ATM mode only.
0x000E	PPP			
	0	TransparentMode	0x0	Enables transparent mode when 0x1. In transparent mode the HDLC functionality is bypassed, i.e., all bytes are passed through transparently (no flag insertion, no byte stuffing, no FCS insertion). Applies to PPP mode only.
	1	InsertHeader_Enable	0x1	Enables Address (0xFF) and Control (0x03) fields insertion when 0x1. Applies to PPP (no transparent) mode only.
	2	FCS_Calculation_Enable	0x1	Enables FCS calculation when 0x1. Applies to PPP (no transparent) mode only.
	3	FCS32_Enable	0x1	32 bit FCS size when 0x1, 16 bit FCS size otherwise. Applies to PPP (no transparent) mode only.
	4	MultipleFlag_Enable	0x0	Enables insertion of minimum two flag characters (0x7E) between two frames when 0x1, insertion of minimum one flag character otherwise. Applies to PPP (no transparent) mode only.
	12 - 5	TransparentByte	0x0	If transparent mode is enabled: Byte to be inserted as payload 1) during Tx FIFO underflow if mapping is enabled or 2) if mapping is disabled. Applies to PPP (transparent) mode only.

8.15 POINTER GENERATOR

Table 62: Pointer Generator (T_RETIMER)

Offset	Bits	Name	Init	Access	Description
0x0000		AUG1_Mode_Config		rw	T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration.
0x0010		CorrDefects_Mask		rw	T_RT_Defects (See page 228.) Correlated defects mask.
0x0020		CorrDefects_Unlatched		ro	T_RT_Defects (See page 228.) Correlated defects.
0x0030		CorrDefects_LatchForInt		cow_1	T_RT_Defects (See page 228.) Correlated defects latched for interrupt.
0x0040		Common_Config		rw	T_RT_Common_Config (See page 228.) General configuration.
0x0080		VCx			Array (12) of T_RT_VCx (See page 229.) Offset between two elements = 0x8. Array index indicates the high order path. Configuration and status.

Table 63: Pointer Generator Defects (T_RT_Defects)

Offset	Bits	Name	Init	Description
0x0000	11 - 0	Reserved	0xFFF	Reserved.
	12	LOF	0x1	Loss Of Frame defect on external reference frame sync (REFTXFS).

Table 64: Pointer Generator Common Configuration (T_RT_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	PointerZero	0x0	Fixed pointer value for pointer generation. Pointer is 0 when 0x1, 522 when 0x0.
0x0002	0	Reserved	0x0	Reserved.
0x0004	0	ExtFramePulseExpected	0x0	Lock on external reference frame sync (REFTXFS) when 0x1.
0x0006	0	ExtFramePulseNegEdge	0x0	Sample external reference frame sync (REFTXFS) on negative clockedge when 0x1.
0x0008	13 - 0	ExtFramePulseOffset	0x0	Range 0 to 9719 Offset between external reference frame sync (REFTXFS) and system reference frame sync.
0x000A	13 - 0	Reserved	0x25E4	Reserved.
0x000C	13 - 0	Reserved	0x25E1	Reserved.

Table 65: Pointer Generator Per Path (T_RT_VCx)

Offset	Bits	Name	Init	Access	Description
0x0000		VC3_TUG3_Config		rw	T_RT_VC3_TUG3_Config (See page 229.) High order path configuration.
0x0006		Reserved		ro	Reserved.

Table 66: Pointer Generator Path Configuration (T_RT_VC3_TUG3_Config)

Offset	Bits	Name	Init	Description
0x0000	1 - 0	SS_bits	0x2	SS bits to be used in the Pointer Generator.
0x0002	15 - 0	Reserved	0x10	Reserved.
0x0004	15 - 0	Reserved	0x10	Reserved.

8.16 CLOCK RECOVERY/CLOCK SYNTHESIS/SERDES

Table 67: Clock Recovery/Clock Synthesis/SerDes (T_ANALOG)

Offset	Bits	Name	Init	Access	Description
0x0000		TestControl		rw	T_TestControl (See page 230.) Configuration of the PRBS generator/analyzer at the cross connect.
0x0020		Common_Config		rw	T_ANALOG_Common_Config (See page 231.) Loopback selection routes input or output data to different output/inputs for test purposes.
0x0030		PadPowerDown		rw	T_PadPowerDown (See page 232.) Powerdown for each LVPECL and LVDS pad.
0x0040	11 - 0	Status_Unlatched	0x0	ro	Unlatched Status. • bit 0: reserved • bit 1: reserved • bit 2: reserved • bit 3: reserved • bit 4: reserved • bit 5: Lock indication Transmit PLL • bit 6: Lock indication Receive PLL • bit 7: SignalDetect Line 1 • bit 8: SignalDetect Line 2 • bit 9: SignalDetect Line 3 • bit 10: SignalDetect Line 4 • bit 11: Lock indication PRBS analyzer
0x0044	11 - 0	Status_LatchForInt	0x0	cow_1	Status Latched for Interrupt, see Unlatched Status
0x0048	11 - 0	Status_Mask	0xFFF	rw	Status Mask, see Unlatched Status

Table 67: Clock Recovery/Clock Synthesis/SerDes (T_ANALOG) (cont.)

Offset	Bits	Name	Init	Access	Description
0x004C	2 - 0	DivideClocks	0x0	rw	Divide clocks by 4. For every bit in the list, 0x1 divides the corresponding clock by 4. • bit 0: Line 1 receive clock • bit 1: APS receive clock • bit 2: Transmit clock Note: The undivided APS receive clock and Transmit Clock are always 77.76 MHz. Line 1 receive clock frequency depends on the operational mode (77.76 MHz in STM-4 mode, 19.44 MHz in STM-1 mode.
0x0050		CDR_CS_Setup		rw	T_CDR_CS_Setup (See page 233.) Setup and initialization of the Clock Recovery, Serializer and Deserializer (CDR/CS).
0x0060		PLL_Control		rw	T_PLL_Control (See page 233.) Control of the PLL's in Clock Recovery, Serializer and Deserializer (CDR/CS).

Table 68: Test Configuration (T_TestControl)

Offset	Bits	Name	Init	Description
0x0000	0	Reserved	0x0	Reserved.
0x0002	0	Reserved	0x0	Reserved.
0x0004	3 - 0	Reserved	0x0	Reserved.
0x0006	0	Reserved	0x0	Reserved.
0x0008	3 - 0	Reserved	0x0	Reserved.
0x000A	0	Reserved	0x0	Reserved.
0x000C		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration for the PRBS generator/analyzer at the cross connect.
0x000E		XConnectPRBSControl		T_XConnectPRBSControl (See page 231.) Configuration of the PRBS generator/analyzer in the cross connect.

Table 69: PRBS Configuration (T_XConnectPRBSControl)

Offset	Bits	Name	Init	Description
0x0000	0	EnablePRBSGenerator	0x0	The PRBS generator at the cross connect is enabled when 0x1, disabled when 0x0.
	4 - 1	PRBSGeneratorChannel	0x0	Range 0 to 11 Path on which PRBS is inserted.
	5	InvertPRBSGeneratorOutput	0x1	The output of the PRBS generator is inverted when 0x1.
	6	EnablePRBSAnalyzer	0x0	The PRBS analyzer at the cross connect is enabled when 0x1, disabled when 0x0.
	10 - 7	PRBSAnalyzerChannel	0x0	Range 0 to 11 Path on which PRBS is received.
	11	InvertPRBSAnalyzerOutput	0x1	The received bits are inverted before they are analyzed by the PRBS analyzer when 0x1.

Table 70: CDR/CS Configuration (T_ANALOG_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	SerDes_LoadConfig	0x0	Writing 0x1 to this register will start the transmission of the control signals to the SerDes. When the transmission is finished this register is reset to its default value. Writing 0x0 to the register is ignored. The following settings are transmitted: • CDR_CS_Setup.TxPowerDown • CDR_CS_Setup.RxPowerDown1 • CDR_CS_Setup.RxPowerDown2 • CDR_CS_Setup.ToplevelPowerDown • CDR_CS_Setup.OC3NotOC12 • PLL_Control.TxPLL_Cap_Enable • PLL_Control.RxPLL_Cap_Enable • PLL_Control.TxPLL_PowerDown • PLL_Control.RxPLL_PowerDown • PLL_Control.CDRTune[4:0] • PLL_Control.PLLTune • All settings configured via the indirect access register (CDR_CS_Setup.Indirect_AccessData and Common_Config.IndirectAccessMode)

Table 70: CDR/CS Configuration (T_ANALOG_Common_Config) (cont.)

Offset	Bits	Name	Init	Description
0x0002	4 - 0	SysLoop	0x0	System Loopback Select, it routes the serialized transmit output to the deserializer receive input. Each bit controls a line. The corresponding LIU is in normal operation when 0x0 and is looped back when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0004	4 - 0	FacLoop	0x0	Facility Loopback Select, it routes the receive serial input back to the transmit serial output. Each bit controls a line. The corresponding LIU is in normal operation when 0x0 and is looped back when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0006	5 - 0	IndirectAccessMode	0x0	Selects the mode for the IndirectAccessData register. • 0x0: Mode0 • 0x8: Mode1 • All others: Reserved

Table 71: High Speed Interface Power Down (T_PadPowerDown)

Offset	Bits	Name	Init	Description
0x0000	4 - 0	RxPAD	0x1F	Power Down for the Receive Line and APS pads. Each bit controls a receive pad. The corresponding pad is powered down when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0002	4 - 0	TxPAD	0x1F	Power Down for the Transmit Line and APS pads. Each bit controls a transmit pad. The corresponding pad is powered down when 0x1. • bit 0: Line 1 • bit 1: Line 2 • bit 2: Line 3 • bit 3: Line 4 • bit 4: APS
0x0004	0	TxRefClock2	0x1	Power Down for the Transmit Reference Clock Pad, REFTXCLK2. The pad is powered down when 0x1.

Table 72: Setup of Clock Recovery/Clock Synthesis/SerDes (T_CDR_CS_Setup)

Offset	Bits	Name	Init	Description
0x0000	9-0	TxPowerDown	0x3FF	Power down for the SerDes transmit section. Must be set to 0x0 at power-up.
0x0002	0	LineRate	0x0	Indicates the line rate for the selected line when line timing is used. Line rate is 155.52 Mbit/s when 0x0, 622.08 Mbit/s when 0x1. Note: This setting is only applicable for the line selected by LineTimingChannel when TimingMode is 0x1.
0x0004	13-0	RxPowerDown1	0x3FFF	Power down for the SerDes receive section. Must be set to 0x0 at power-up.
0x0006	14-0	RxPowerDown2	0x7FFF	Power down for the SerDes receive section. Must be set to 0x0 at power-up.
0x0008	0	ToplevelPowerDown	0x1	Power down for the toplevel SerDes bias module. Must be set to 0x0 at power-up.
0x000A	4 - 0	OC3NotOC12	0x1F	Line Rate Configuration • 0x0E: STM-4 Mode • 0x0F: STM-1 Mode • All others: Reserved
0x000C	15 - 0	PRBSBitErrorCounter	0x0	Bit Error counter of the PRBS analyzer at the cross connect. This (read-only) counter is clear-on-read.
0x000E	15 - 0	IndirectAccessData	0x0	Indirect Access Data register. When a write is done to this register, the field specified by the IndirectAccessMode will be configured. Following values need to be set when initializing the CDR/CS: • 0x0017 to IndirectAccessMode Mode0 • 0x5000 to IndirectAccessMode Mode1

Table 73: PLL Control (T_PLL_Control)

Offset	Bits	Name	Init	Description
0x0000	0	TimingMode	0x0	External/Line timing mode selection for the transmit PLL. External timing mode is selected when 0x0, TxRefSelect selects the external source. Line-Timing mode is selected when 0x1, LineTimingChannel selects the line timing channel.
0x0002	2 - 0	LineTimingChannel	0x0	Range 0 to 4 Line timing mode channel selection. This field is only used when TimingMode is '1'. The value indicates the line. • 0x0: Line 1 • 0x1: Line 2 • 0x2: Line 3 • 0x3: Line 4 • 0x4: APS
0x0004	0	TxRefSelect	0x0	Transmit reference clock external source selection for the PLL in the transmit section. This field is only valid when TimingMode is '0'. • 0x0: REFTXCLK1 is used as reference clock • 0x1: REFTXClK2 is used as reference clock

Table 73: PLL Control (T_PLL_Control) (cont.)

Offset	Bits	Name	Init	Description
0x0006	0	RxRefSelect	0x0	Receive reference clock external source selection for the PLL in the receive section. • 0x0: REFRXCLK is used as reference clock • 0x1: REFTXCLK1/REFTXCLK2 is used as reference clock, the selection between the transmit reference clocks is made using the TxRefSelect field
0x0008	0	TxPLL_Cap_Enable	0x0	Enables the external capacitor in the Transmit PLL when 0x1.
0x000A	0	RxPLL_Cap_Enable	0x0	Reserved. Must be set to 0.
0x000C	1 - 0	TxRefFreq	0x0	Transmit PLL reference clock frequency. Indicates the frequency of the reference clock for the PLL. • 0x0: 19.44 MHz, REFTXCLK1 or REFTXCLK2 • 0x1: 77.76 MHz, REFTXCLK1 or REFTXCLK2 • 0x2: 155.52 MHz, REFTXCLK2 • 0x3: 622.04 MHz, REFTXCLK2. In this mode the Transmit PLL must be bypassed. Mind the Transmit PLL is actually still working then, although it's output is never used.
0x000E	1 - 0	RxRefFreq	0x0	Receive PLL reference clock frequency. Indicates the frequency of the reference clock for the PLL. • 0x0: 19.44 MHz, REFRXCLK or REFTXCLK1 or REFTXCLK2 • 0x1: 77.76 MHz, REFRXCLK or REFTXCLK1 or REFTXCLK2 • 0x2: 155.52 MHz, REFTXCLK2 • 0x3: Reserved
0x0010	4-0	TxPLL_PowerDown	0x1F	Power Down for the Transmit PLL modules. Must be set to 0x0 at power-up.
0x0012	4-0	RxPLL_PowerDown	0x1F	Power Down for the RxPLL modules. Must be set to 0x0 at power-up.
0x0014		CDRTune		Array (5) of T_CDRTune (See page 234.) Offset between two elements = 0x2. Array index indicates the interface. • Array index 0: Line 1 • Array index 1: Line 2 • Array index 2: Line 3 • Array index 3: Line 4 • Array index 4: APS
0x001E		PLLTune		T_PLLTune (See page 235.)

Table 74: CDR Tuning Configuration (T_CDRTune)

Offset	Bits	Name	Init	Description
0x0000	2 - 0	PhaseInterpolator	0x4	Reserved. Set to 0x4 for Line/Loop Timing and STM-4/OC-12 application Set to 0x1 for all other application
	12 - 3	DigitalLoopFilter	0x4A	Reserved. Set to 0x4a for STM-4/OC-12 application Set to 0x5c for STM-1/OC-3 application

Table 75: PLL Tuning Configuration (T_PLLTune)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	TxPLL_ChargePump	0x4	Reserved. Set to 0x1 for External Timing Set to 0x4 for Line/Loop Timing and STM-4/OC-12 application Set to 0x8 for Line/Loop Timing and STM-1/OC-3 application
	6 - 4	TxPLL_VCO	0x4	Reserved. Set to 0x1
	10 - 7	RxPLL_ChargePump	0x4	Reserved. Set to 0x4
	13 - 11	RxPLL_VCO	0x4	Reserved. Set to 0x1

8.17 RECEIVE APS PORT

Table 76: Receive APS Port (T_RX_APS)

Offset	Bits	Name	Init	Access	Description
0x0000	7 - 0	Reported_TTI_Message	0x0	ro	Received J0 byte.
0x0010		Common_Config		rw	T_RX_APS_Common_Config (See page 236.) General configuration.
0x0018	7 - 0	Expected_TTI_Message	0x0	rw	Expected J0 byte.
0x0020		CorrDefects_Unlatched		ro	T_RX_APS_Defects (See page 236.) Correlated defects.
0x0028		CorrDefects_LatchForInt		cow_1	T_RX_APS_Defects (See page 236.) Correlated defects latched for interrupt.
0x0030		CorrDefects_Mask		rw	T_RX_APS_Defects (See page 236.) Correlated defects mask.
0x0038	15 - 0	B1_PM_Counter	0x0	ro	B1 performance counter.
0x0040		APS_Info			Array (4) of T_RX_APS_APSInfo (See page 236.) Offset between two elements = 0x10. Array index indicates the line (= line number - 1). Received APS information.

Table 77: Receive APS Port Common Configuration (T_RX_APS_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	LOF_AIS_Insert_Disable	0x0	Insertion of AIS on Loss of Frame defect is disabled when 0x1.
	1	Framer_AIS_Force	0x0	AIS insertion is forced after framing when 0x1.
	2	Descrambler_Disable	0x0	Descrambling is disabled when 0x1.
	3	TIM_AIS_Insert_Disable	0x0	Insertion of AIS on Trail Trace Identifier Mismatch defect is disabled when 0x1.
	4	SSF_AIS_Insert_Disable	0x0	Insertion of AIS on incoming Server Signal Fail is disabled when 0x1.
	5	APS_AIS_Force	0x0	AIS insertion is forced after APS monitoring when 0x1.

Table 78: Receive APS Port Defects (T_RX_APS_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	OOF	0x1	Out of Frame.
	1	LOF	0x1	Loss of Frame.
	2	B1_Error	0x1	B1 BIP error.
	3	TIM	0x1	J0 Trail Trace Identifier mismatch.
	4	SSF	0x1	Incoming SSF (Server Signal Fail).

Table 79: Receive APS Port Per Line (T_RX_APS_APSInfo)

Offset	Bits	Name	Init	Access	Description
0x0000		APS_Bytes		ro	T_RX_APS_APSBytes_Status (See page 236.) Received APS information.
0x0006		APSEvents_Unlatched		ro	T_RX_APS_APSBytes_Event (See page 237.) Events on APS bytes.
0x0008		APSEvents_LatchForInt		cow_1	T_RX_APS_APSBytes_Event (See page 237.) Events on APS bytes latched for interrupt.
0x000A		APSEvents_Mask		rw	T_RX_APS_APSBytes_Event (See page 237.) Events on APS bytes mask.

Table 80: Receive APS Port Status (T_RX_APS_APSBytes_Status)

Offset	Bits	Name	Init	Description
0x0000	15 - 0	RX_K1K2	0x0	Received K1/K2 bytes (most significant byte is K1, least significant byte is K2).
0x0002	15 - 0	TX_K1K2	0x0	K1/K2 bytes to transmit (most significant byte is K1, least significant byte is K2).

Table 80: Receive APS Port Status (T_RX_APS_APSBytes_Status) (cont.)

Offset	Bits	Name	Init	Description
0x0004	15 - 0	Status_Request	0x0	Received SF and SD indications and indications for switch/bridge requests (most significant byte is status (bit 0 is SF and bit 1 is SD), least significant byte is switch/bridge request).

Table 81: Receive APS Port Events (T_RX_APS_APSBytes_Event)

Offset	Bits	Name	Init	Description
0x0000	0	RX_K1K2_Changed	0x1	Receive K1/K2 changed.
	1	TX_K1K2_Changed	0x1	Transmit K1/K2 changed.
	2	Status_Request_Changed	0x1	Status/Request information changed.

8.18 CROSS CONNECT

Table 82: Cross Connect (T_VC_XCONNECT)

Offset	Bits	Name	Init	Access	Description
0x0000		Termination_Config		rw	T_XC_Bus_Config (See page 237.) Configuration for the Terminal interface bus.
0x0040		Line_Config		rw	T_XC_Bus_Config (See page 237.) Configuration for the Line interface bus.
0x0060		APS_Config		rw	T_XC_Bus_Config (See page 237.) Configuration for the APS Port bus.

Table 83: Cross Connect Bus Configuration (T_XC_Bus_Config)

Offset	Bits	Name	Init	Description
0x0000		AUG1		T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration.
0x0002		Timeslot		Array (12) of T_XConnect_Config (See page 238.) Offset between two elements = 0x2. Array index indicates the high order path. Cross connect configuration.

Table 84: Cross Connect Time Slot Configuration (T_XConnect_Config)

Offset	Bits	Name	Init	Description
0x0000	8 - 0	SourceTimeslot	0x0	Range 0 to 11 Source time slot for this output slot.
	10 - 9	SourceBus	0x0	Range 0 to 2 Source bus for this output slot. • 0x0 = Line Interface • 0x1 = APS Interface • 0x2 = Terminal Interface
	13 - 11	Reserved	0x0	Reserved.
	14	Force_AIS	0x0	The AIS pattern is inserted in this timeslot when 0x1.
	15	Force_Uneq	0x0	The Uneq pattern is inserted in this timeslot when 0x1.

8.19 EGRESS UTOPIA/POS-PHY LEVEL 2 INTERFACE

Table 85: UTOPIA/POS-PHY (T_DO_UTOPIA_POSPHY)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_DO_UTOPIA_POSPHY_Common_Config (See page 239.) General configuration.
0x0010		DirectStatus_Config		rw	Array (4) of T_DirectStatusTimeslot (See page 203.) Offset between two elements = 0x2. Array index indicates the CLAV. Direct status configuration.
0x0020		PHY_Port_Config		rw	Array (12) of T_UTOPIA_POSPHY_PHY_Port_Config (See page 204.) Offset between two elements = 0x2. Array index indicates the PHY. PHY Configuration.

Table 86: UTOPIA/POS-PHY Common Configuration (T_DO_UTOPIA_POSPHY_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	EnableInterface	0x0	Enables the interface when 0x1. Applies to both UTOPIA and POS-PHY mode.
	1	MPHY	0x1	Multiple PHY when 0x1, Single PHY when 0x0. Applies to both UTOPIA and POS-PHY mode.
	2	Reserved	0x1	Reserved
	4 - 3	StatusIndication	0x1	0x0 = DIRECT_STATUS 0x1 = MUX_STATUS_POLLING_FULL_ADDR 0x2 = MUX_STATUS_POLLING_GROUP_ADDR Applies to both UTOPIA and POS-PHY mode, note that for POS-PHY mode the option multiplexed status polling with group address is not valid.
	5	ParityEven	0x0	Even parity when 0x1, odd parity when 0x0. Applies to both UTOPIA and POS-PHY mode.
	6	ParityOverDataOnly	0x1	Parity over databus only when 0x1, over databus and control signals when 0x0. Applies to both UTOPIA and POS-PHY mode.
	14 - 7	DataAV_Threshold	0x1B	Range 1 to 128 Minimum number of words which needs to be available in the FIFO before the data available indication (PRPA/DRPA) is set on the POS-PHY interface. This value must always be larger than 0. Applies to POS-PHY mode only, for UTOPIA mode this must always be set to 27 (0x1B).

8.20 HIGH ORDER PATH RING PORT/ALARM INTERFACE

Table 87: Path Ring Port/Alarm Interface (T_HO_POH_RING_PORT)

Offset	Bits	Name	Init	Access	Description
0x0000		Common_Config		rw	T_HOPR_Common_Config (See page 240.) General configuration.
0x0008		CorrDefects_Unlatched		ro	T_HOPR_Defects (See page 240.) Correlated defects.
0x0010		CorrDefects_LatchForInt		cow_1	T_HOPR_Defects (See page 240.) Correlated defects latched for interrupt.
0x0018		Defects_Mask		rw	T_HOPR_Defects (See page 240.) Correlated defects mask.
0x0020		VC_Config		rw	Array (12) of T_HOPR_VC_Config (See page 240.) Offset between two elements = 0x2. Array index indicates the high order path. High order path configuration.

Table 88: Path Ring Port/Alarm Interface Common Configuration (T_HOPR_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	0	InsertCRCError	0x0	Insert CRC errors. All CRC bits are inverted when 0x1 (for test purposes only).

Table 89: Path Ring Port/Alarm Interface Defects (T_HOPR_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	CRC_Error	0x1	CRC error on external Ring Port interface.
	1	LOC	0x1	Loss of clock on external Ring Port interface.

Table 90: Path Ring Port/Alarm Interface Path Configuration (T_HOPR_VC_Config)

Offset	Bits	Name	Init	Description
0x0000	0	SelectExternalSource	0x0	Select external ring port when 0x1. Internal ring port is used when 0x0.
	1	ResetVC	0x0	Resets an entire VC information when 0x1.
	2	ExtendRDI	0x0	Extends RDI for 20 frames when 0x1.

8.21 JTAG MASTER

Table 91: JTAG Master (T_JTAG_MASTER)

Offset	Bits	Name	Init	Access	Description
0x0000	0	Bit_wise_control	0x0	rw	This bit selects if direct microprocessor control bits will be used, instead of the FIFO's.
0x0004	1 - 0	TDI_TMS_bit	0x0	rw	The microprocessor driven TDI and TMS bit values (bit 0 = TMS, bit 1 = TDI).
0x0008	0	TCK_bit	0x0	rw	The microprocessor driven TCK clock bit value.
0x000C	0	TDO_bit	0x0	ro	The microprocessor read TDO bit value.
0x0010	7 - 0	TCK_DIVIDER	0x0	rw	A clock divider number to create an appropriate 10 MHz TCK clock using the current system clock.
0x0012	5 - 0	Counter	0x0	rw	6-bit shift count register.
0x0014	7 - 0	TDI_Fifo_B0	0x0	rw	FIFO containing TDI data to send to TAP (byte 0).
0x0016	7 - 0	TDI_Fifo_B1	0x0	rw	FIFO containing TDI data to send to TAP (byte 1).
0x0018	7 - 0	TDI_Fifo_B2	0x0	rw	FIFO containing TDI data to send to TAP (byte 2).
0x001A	7 - 0	TDI_Fifo_B3	0x0	rw	FIFO containing TDI data to send to TAP (byte 3).
0x001C	7 - 0	TDI_Fifo_B4	0x0	rw	FIFO containing TDI data to send to TAP (byte 4).
0x001E	7 - 0	TMS_Fifo_B0	0x0	rw	FIFO containing TMS data to send to TAP (byte 0).
0x0020	7 - 0	TMS_Fifo_B1	0x0	rw	FIFO containing TMS data to send to TAP (byte 1).
0x0022	7 - 0	TMS_Fifo_B2	0x0	rw	FIFO containing TMS data to send to TAP (byte 2).
0x0024	7 - 0	TMS_Fifo_B3	0x0	rw	FIFO containing TMS data to send to TAP (byte 3).
0x0026	7 - 0	TMS_Fifo_B4	0x0	rw	FIFO containing TMS data to send to TAP (byte 4).
0x0028	7 - 0	TDO_Fifo_B0	0x0	ro	FIFO containing TDO data received from the TAP (byte 0).
0x002A	7 - 0	TDO_Fifo_B1	0x0	ro	FIFO containing TDO data received from the TAP (byte 1).
0x002C	7 - 0	TDO_Fifo_B2	0x0	ro	FIFO containing TDO data received from the TAP (byte 2).
0x002E	7 - 0	TDO_Fifo_B3	0x0	ro	FIFO containing TDO data received from the TAP (byte 3).
0x0030	7 - 0	TDO_Fifo_B4	0x0	ro	FIFO containing TDO data received from the TAP (byte 4).
0x0032	0	Start	0x0	rw	Start bit. Is set to trigger a transfer between microprocessor & TAP. This bit clears the Done and Error bits.
0x0034	1 - 0	Done	0x0	ro	When the transfer is completed, these bits are set: • bit 0 = 'Done' • bit 1 = 'Error'
0x0036	0	JM_TRSTN	0x0	rw	The value of TRSTN driven by the microprocessor interface.
0x0038	0	TDI_LoopBack	0x0	rw	This bit loops back the TDI FIFO output, back into the TDO FIFO Input (Used for test).
0x003A	0	TMS_LoopBack	0x0	rw	This bit loops back the TMS FIFO output, back into the TDO FIFO Input (Used for test).
0x003C	0	TRSTN_Sample	0x0	ro	This bit samples what the microprocessor interface is driving into the TAP.
0x003E	0	uProcessor_CNTRL	0x1	rw	This bit switches the TAP control over to the microprocessor.

8.22 POH MONITOR

Table 92: POH Monitor (T_VC_POH_MONITOR)

Offset	Bits	Name	Init	Access	Description
0x0000		VC_Config		rw	T_VCXPM_Config (See page 242.) High order path configuration. The high order path to be configured is selected by indirect access. See the Config_Channel register in the Common_Config record to select the desired high order path.
0x0200		Common_Config		rw	T_VCXPM_Common_Config (See page 244.) General configuration.
0x0300		Common_Status		ro/cow_1	T_VCXPM_Common_Status (See page 246.) General status. Note: Latched bits are clear-on-write-1, all others are read-only.
0x0400		VC_Status		ro/cow_1	Array (12) of T_VCXPM_Status (See page 246.) Offset between two elements = 0x40. Array index indicates the high order path. High order path status. Note: Latched bits are clear-on-write-1, all others are read-only.

Table 93: POH Monitor Path Configuration (T_VCXPM_Config)

Offset	Bits	Name	Init	Description
0x0000	ModeTTIConfig			
	0	Bypass	0x0	No processing is done on this high order path when 0x1. Use this bypass for unused paths.
	1	AIS_Force	0x0	AIS insertion is forced when 0x1.
	2	Unidirectional	0x0	Enables the uni-directional option when 0x1. When the uni-directional option is active, the FarEndBlockErrorCounter will report 0 and the RDI defect is cleared.
	3	TTI_ExTiMessage	0x0	Ignore expected TTI message and assume non-specific repeating byte message when 0x0. When 0x1 the TTI message has to match the specified expected message (16 or 64 byte TTI message).
	4	TTI_ExTi64	0x0	64 byte trace message when 0x1, 16 byte trace message when 0x0. This setting is only valid when TTI_ExTiMessage is 0x1.
	5	TTI_TimEnable	0x0	TIM detection is enabled when 0x1.
	6	TIM_AIS_Insert_Disable	0x0	AIS insertion on Trail Trace Identifier Mismatch defect is disabled when 0x1.
0x0002		ExpectedBytes	All 0x0	T_VCXPM_ExpectedBytes (See page 243.) Expected bytes.
0x0084		B3_Config		T_BIP_Detector_Config (See page 243.) Configuration for B3 BIP detector (DEG/EXC).
0x00A0	BytesConfig			
	3 - 0	G1_AcceptNoOfIntervals	0x5	Integer 3, 5 (ETSI) or 10 (Telcordia) Number of consecutive frames to debounce G1.
	4	G1_CountBitErrors	0x0	REI bit errors are reported when 0x1, block errors when 0x0.
	6 - 5	Reserved	0x0	Reserved.
	10 - 7	Reserved	0x5	Reserved.
0x00A2		CorrDefects_Mask		T_VCXPM_Defects (See page 244.) Correlated defects mask.

Table 94: POH Monitor Expected J1/C2 (T_VCXPM_ExpectedBytes)

Offset	Bits	Name	Init	Description
0x0000		Expected_TTI_Message	All 0x0	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Expected TTI message. • bytes 0-15 for 16 byte TTI message • bytes 0-63 for 64 byte TTI message This register is only used when TTI_ExTiMessage is 0x1 (see VC_Config).
0x0080	7 - 0	Expected_C2	0x0	Expected C2 Byte.

Table 95: BER Detection Configuration (T_BIP_Detector_Config)

Offset	Bits	Name	Init	Description
0x0000	0	PoissonErrorCheck	0x0	Assume Poisson error distribution when 0x1, bursty distribution when 0x0.
0x0002		PoissonDetector_Config		T_BIP_PoissonDetector_Config (See page 211.) Configuration for DEG/EXC detection, assuming Poisson distribution of errors.
0x0014		BurstyDetector_Config		T_BIP_BurstyDetector_Config (See page 243.) Configuration for DEG detection, assuming bursty distribution of errors.

Table 96: Path Bursty Distribution BER Detection (T_BIP_BurstyDetector_Config)

Offset	Bits	Name	Init	Description
0x0000	12 - 0	DEG_DetectionErrorThreshold	0x1F40	Range 0 to 8000 An (one second) interval is bad if the number of detected errored blocks in that interval is greater than or equal to this threshold.
0x0002	3 - 0	DEG_DetectionWindowSize	0xA	Range 2 to 10 Number of consecutive bad intervals before DEG is declared.
0x0004	12 - 0	DEG_RecoveryErrorThreshold	0x1F40	Range 0 to 8000 An (one second) interval is a good interval when the number of errored blocks in this interval does not exceed this threshold.
0x0006	3 - 0	DEG_RecoveryWindowSize	0x2	Range 2 to 10 Number of consecutive good intervals before DEG is cleared.

Table 97: POH Monitor Defects (T_VCXPM_Defects)

Offset	Bits	Name	Init	Description
0x0000	0	SSF	0x1	Incoming SSF (Server Signal Fail).
	1	TIM	0x1	J1 Trail Trace Identifier Mismatch.
	2	TTIZERO	0x1	J1 Trail Trace Identifier Zero.
	3	DEG	0x1	Degraded signal.
	4	EXC	0x1	Excessive error.
	5	UNEQ	0x1	Unequipped.
	6	AIS	0x1	VC-AIS detected on C2.
	7	RDI	0x1	Remote Defect Indication.
	8	RDI_S	0x1	Enhanced Remote Defect Indication (E-RDI) Server.
	9	RDI_C	0x1	Enhanced Remote Defect Indication (E-RDI) Connectivity.
	10	RDI_P	0x1	Enhanced Remote Defect Indication (E-RDI) Payload.
	11	PLM	0x1	Payload Mismatch.
	12	Reserved	0x1	Reserved.
	13	K3_APS	0x1	Event on K3 APS byte.
	14	C2_Changed	0x1	Event on C2 byte.

Table 98: POH Monitor Common Configuration (T_VCXPM_Common_Config)

Offset	Bits	Name	Init	Description
0x0000	3 - 0	Config_Channel	0x0	Range 0 to 11 High order path for which configuration can be done in VC_Config.
0x0002		AUG1_Mode_Config		T_AUG1_Mode_Config (See page 205.) AUG-1 mode configuration.
0x0004	TTIConfig			
	0	TTI_Report_Enable	0x0	Enables J1 TTI message reporting when 0x1. TTI_Report_Channel indicates the high order path for which reporting is enabled.
	4 - 1	TTI_Report_Channel	0x0	Range 0 to 11 High order path for which J1 reporting is done.
	5	SSF_TIM_Inhibit_Disable	0x0	Inhibition of TIM defect by incoming SSF is disabled when 0x1.
	6	UNEQ_TIM_Inhibit_Disable	0x0	Inhibition of TIM defect by UNEQ defect is disabled when 0x1.
	7	TTIZERO_TIM_Inhibit_Disable	0x0	Inhibition of TIM defect by TTIZERO defect is disabled when 0x1.
	8	SSF_TTIZERO_Inhibit_Disable	0x0	Inhibition of TTIZERO defect by SSF defect is disabled when 0x1.
0x0006	TTISettings			
	3 - 0	TTI_FramesToSetTim	0x5	Range 2 to 15 Number of consecutive mismatched multiframes to set TIM.
	7 - 4	TTI_FramesToResetTim	0x3	Range 2 to 15 Number of consecutive match multiframes to clear TIM.

Table 98: POH Monitor Common Configuration (T_VCXPM_Common_Config) (cont.)

Offset	Bits	Name	Init	Description
0x0008	AISRDIInsertion			
	0	SSF_AIS_Insert_Disable	0x0	Insertion of AIS on incoming Server Signal Fail is disabled when 0x1.
	1	AIS_AIS_Insert_Disable	0x0	Insertion of AIS on AIS defect is disabled when 0x1.
	2	EXC_AIS_Insert_Disable	0x0	Insertion of AIS on EXC defect is disabled when 0x1.
	3	UNEQ_AIS_Insert_Disable	0x0	Insertion of AIS on unequipped defect is disabled when 0x1.
	4	PLM_AIS_Insert_Disable	0x0	Insertion of AIS on Payload mismatch defect is disabled when 0x1.
	5	Reserved	0x0	Reserved.
	6	SSF_RDI_Insert_Disable	0x0	Insertion of RDI on incoming Server Signal Fail is disabled when 0x1.
	7	UNEQ_RDI_Insert_Disable	0x0	Insertion of RDI on unequipped defect is disabled when 0x1.
	8	TIM_RDI_Insert_Disable	0x0	Insertion of RDI on Trail Trace Identifier Mismatch defect is disabled when 0x1.
	9	PLM_RDI_Insert_Disable	0x0	Insertion of RDI on Payload mismatch defect is disabled when 0x1.
	10	LCD_RDI_Insert_Disable	0x0	Insertion of RDI on Loss of cell delineation defect is disabled when 0x1.
0x000A	AlarmInhibition			
	0	SSF_UNEQ_Inhibit_Disable	0x0	Inhibition of UNEQ defect by incoming SSF is disabled when 0x1.
	1	TTIZERO_UNEQ_Contribution_Disable	0x0	Contribution of TTIZERO to UNEQ defect is disabled when 0x1.
	2	TIM_UNEQ_Contribution_Disable	0x0	Contribution of TIM to UNEQ defect is disabled when 0x1.
	3	SSF_EXC_Inhibit_Disable	0x0	Inhibition of EXC defect by incoming SSF is disabled when 0x1.
	4	TIM_EXC_Inhibit_Disable	0x0	Inhibition of EXC defect by TIM defect is disabled when 0x1.
	5	SSF_DEG_Inhibit_Disable	0x0	Inhibition of DEG defect by incoming SSF is disabled when 0x1.
	6	TIM_DEG_Inhibit_Disable	0x0	Inhibition of DEG defect by TIM defect is disabled when 0x1.
	7	SSF_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by incoming SSF is disabled when 0x1.
	8	UNEQ_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by UNEQ defect is disabled when 0x1.
	9	TTIZERO_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by TTIZERO defect is disabled when 0x1.
	10	TIM_RDI_Inhibit_Disable	0x0	Inhibition of RDI defect by TIM defect is disabled when 0x1.
	11	AIS_SSF_Contribution_Disable	0x0	Contribution of AIS defect to SSF defect is disabled when 0x1.
	12	TSF_PLM_Inhibit_Disable	0x0	Inhibition of PLM defect by TSF indication is disabled when 0x1.
	13	Reserved	0x0	Reserved.
	14	Reserved	0x0	Reserved.
0x000C	11 - 0	Summary_Mask	0xFFF	Summary mask, one bit per high order path. Least significant bit corresponds to the first high order path.

Table 99: POH Monitor Status (T_VCXPM_Common_Status)

Offset	Bits	Name	Init	Description
0x0000		Reported_TTI64_Message	All 0x0	Array (64) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Accepted Stable 64 byte TTI message.
0x0080		Reported_TTI16_Message	All 0x0	Array (16) of byte Offset between two elements = 0x2. Array index indicates the TTI byte number. Accepted Stable 16 byte TTI message.
0x00A0		ReportStatus		T_VCXPM_Report (See page 246.) Reporting status.
0x00A2	11 - 0	Summary_LatchForInt	0x0	Defects summary, one bit per high order path. Least significant bit corresponds to the first high order path.
0x00A4	11 - 0	Reserved	0x0	Reserved.
0x00A6	11 - 0	Reserved	0x0	Reserved.

Table 100: J1 TTI Stable (T_VCXPM_Report)

Offset	Bits	Name	Init	Description
0x0000	0	Stable_1	0x0	TTI 1 byte message stable indication.
	1	Stable_16	0x0	TTI 16 byte message stable indication.
	2	Stable_64	0x0	TTI 64 byte message stable indication.
	3	Stable_16_Latched	0x0	Latched TTI 16 byte message stable indication. This field is clear-on-write-1.
	4	Stable_64_Latched	0x0	Latched TTI 64 byte message stable indication. This field is clear-on-write-1.

Table 101: POH Monitor Per Path (T_VCXPM_Status)

Offset	Bits	Name	Init	Description
0x0000		POH_Status		T_VCXPM_POH_Status (See page 247.) POH Status: Status of received and accepted POH bytes.
0x0016		PerfMon		T_VCXPM_PM (See page 247.) Performance counters.
0x001E		CorrDefects_Unlatched		T_VCXPM_Defects (See page 244.) Correlated defects.
0x0020		CorrDefects_LatchForInt		T_VCXPM_Defects (See page 244.) Correlated defects latched for interrupt.
0x0022		Reserved	0x0	Reserved.
0x0024		Reserved	0x0	Reserved.
0x0026		Reserved	0x0	Reserved.

Table 102: POH Monitor Path Status (T_VCXPM_POH_Status)

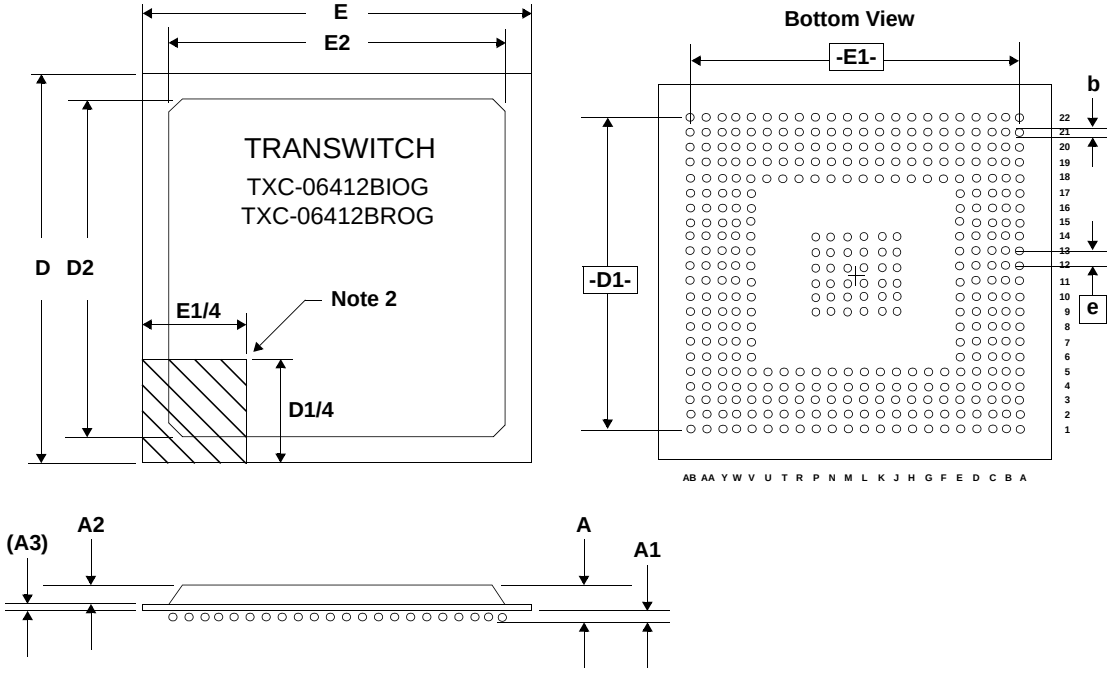
Offset	Bits	Name	Init	Description
0x0000	7 - 0	Received_J1	0x0	J1 byte of the previously received frame.
0x0002	7 - 0	Received_B3_error	0x0	Errored bit positions in B3 byte of the previously received frame.
0x0004	7 - 0	Received_C2	0x0	C2 byte of the previously received frame.
0x0006	7 - 0	Received_G1	0x0	G1 byte of the previously received frame.
0x0008	7 - 0	Received_F2	0x0	F2 byte of the previously received frame.
0x000A	7 - 0	Received_H4	0x0	H4 byte of the previously received frame.
0x000C	7 - 0	Received_F3	0x0	F3 byte of the previously received frame.
0x000E	7 - 0	Received_K3	0x0	K3 byte of the previously received frame.
0x0010	7 - 0	Received_N1	0x0	N1 byte of the previously received frame.
0x0012	7 - 0	Accepted_TSL	0x0	Accepted C2 byte.
0x0014	7 - 0	Accepted_K3	0x0	Accepted K3 byte.

Table 103: POH Monitor Performance Counters (T_VCXPM_PM)

Offset	Bits	Name	Init	Description
0x0000	12 - 0	NearEndDefect_BlockCounter	0x0	Near end block error counter (B3).
0x0002	15 - 0	NearEndDefect_BitCounter	0x0	Near end bit error counter (B3).
0x0004	15 - 0	FarEndDefect_Counter	0x0	Far end error counter (G1). Configurable as bit or block count.
0x0006	DefectSec			
	0	NearEndDefectSec	0x0	TSF one second latch.
	1	FarEndDefectSec	0x0	RDI defect one second latch.

PACKAGE INFORMATION

The PHAST-12P device is packaged in a 376-lead, 23 mm x 23 mm, plastic ball grid array package suitable for surface mounting, as illustrated in Figure 68.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 22 x 22, JEDEC code MO-151.

Dimension (Note 1)	Min	Max
A	2.02	2.44
A1	0.40	0.60
A2	1.12	1.22
A3 (Ref.)	0.56	
b	0.50	0.70
D	23.00	
D1 (Nom)	21.00	
D2	19.45	20.20
E	23.00	
E1 (Nom)	21.00	
E2	19.45	20.20
e (Ref.)	1.00	

Figure 68. PHAST-12P TXC-06412B 376-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-06412BIOG	376-Lead Plastic Ball Grid Array Package
Part Number: TXC-06412BROG	376-Lead Plastic Ball Grid Array Package, Green (RoHS and Lead-free) compliant

RELATED PRODUCTS

PHAST-3P Device (STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface). This device performs STM-1/STS-3c termination into a UTOPIA Level 2 for ATM cell data, or a UTOPIA Level 2P interface for PPP data. Single-PHY or Multi-PHY operation is supported. A serial and byte parallel line interface is provided. Section, line, and path overhead byte processing is performed. Clock synthesis/recovery at 155.52 Mbit/s, alarm and error processing, as well as TX and RX retiming is provided.

PHAST-12N Device (STM-4/OC-12 SDH/SONET Overhead Terminator with Telecom Bus Interface). A highly integrated SDH/SONET overhead terminator device designed for TDM payload mappings. A single PHAST-12N can terminate four individual STM-1/OC-3 lines or a single STM-4/OC-12 line. Each SDH/SONET terminator has a line interface block that performs clock synthesis and clock recovery for four 155 Mbit/s signals or a single 622 Mbit/s serial signal.

Envoy-8FE Device (Octal Fast Ethernet Controller). An 8-port Fast Ethernet to POS-PHY Level 2/OIF SPI-3 bridging device. Each SMII port is connected to Media Access Control (MAC), operating at 10/100 Mbits/s mixed mode.

Envoy-2GE Device (Dual Gigabit Ethernet Controller). A 2-port Gigabit Ethernet to POS-PHY Level 2/3 bridging device. Each GMII port is connected to a Media Access Control (MAC), operating at 1 Gbits/s mode. The MAC is programmable to provide Full-Duplex operation.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

MFA Forum

MPLS & Frame Relay Alliance
48377, Fremont Blvd, Suite 117,
Fremont, California 94538

Tel: +1-510-492-4056
Fax: +1-510-492-4001
Web: www.mfaforum.org/about/contact2.shtml

ATIS

Alliance for Telecommunications Industry Solutions
1200 G Street, NW, Suite 500
Washington, D.C. 20005

Tel: 202.628.6380
Fax: 202.393.5453
Web: www.atis.org

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112

Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France

Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

IEEE (Corporate Office):

American Institute of Electrical Engineers
3 Park Avenue, 17th Floor
New York, New York 10016-5997 U.S.A.

Tel: (212) 419-7900 (within U.S.A.)
Tel: (800) 678-4333 (Members only)
Fax: (212) 752-4929
Web: www.ieee.org

ITU-T (International): (Formerly ANSI)

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
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700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.): (Formerly Bellcore)

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

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Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
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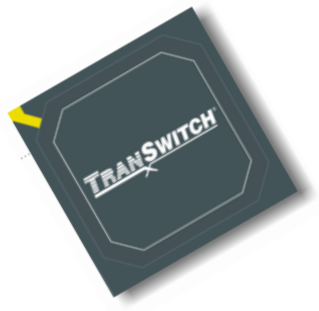

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