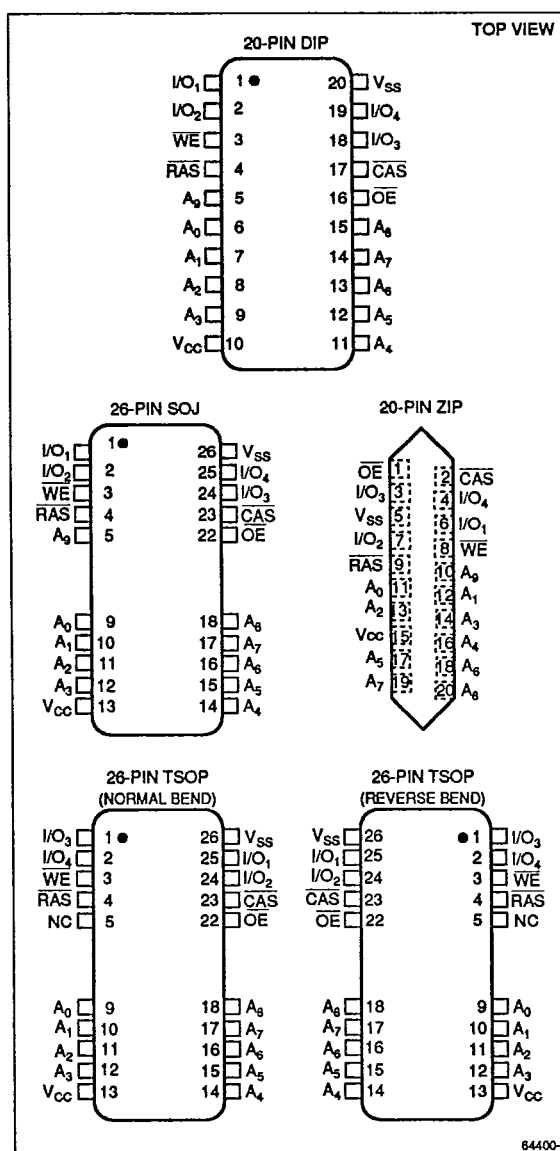


LH64400

PRELIMINARY**CMOS 4M (1M × 4) Dynamic RAM***T-46-23-18***FEATURES**

- 1,048,576 × 4 bit organization
- Access times: 80/100 ns (MAX.)
- Cycle times: 140/160 ns (MIN.)
- Cycle time in high speed page mode: 50/55 ns (MIN.)
- Power supply: +5 V ± 10%
- Power consumption (MAX.):
Operating: 523/468 mW (MAX.)
Standby: 5.5 mW (MAX.)
- TTL compatible I/O
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CAS}$ -before- $\overline{RAS}$ refresh capability
- 8-bit parallel test mode (contact SHARP for details)
- 1,024 refresh cycle (refresh period (MAX.) = 16 ms)
- Packages:
20-pin, 300-mil DIP
26-pin, 300-mil SOJ
20-pin, 400-mil ZIP
26-pin, 300-mil TSOP (normal/reverse bend pins)

PIN CONNECTIONS**DESCRIPTION**

The LH64400 is a 1,048,576 × 4 bit dynamic RAM which provides a high speed page mode operation.

The LH64400 is fabricated using advanced CMOS process technology. With multiplexed address inputs and standard 20-pin DIP/ZIP or 26-pin SOJ/TSOP packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH64400 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

Figure 1. Pin Connections for DIP, SOJ, ZIP, and TSOP Packages

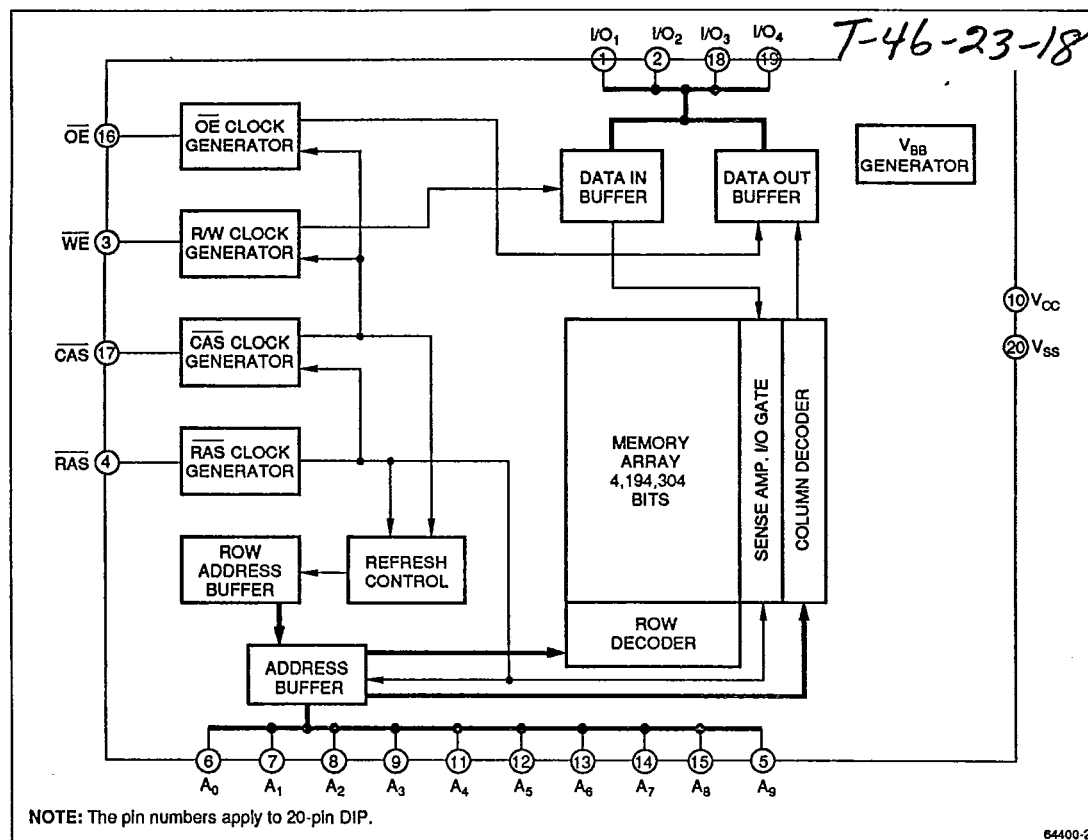


Figure 2. LH64400 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₉	Address input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O ₁ - I/O ₄	Data input/output
V _{cc}	Power supply (+5 V)
V _{ss}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _I	-1.0 to +7.0	V	1
Output short circuit current	I _{os}	50	mA	
Power consumption	P _D	1.0	W	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTE:

1. Referenced to V_{ss}

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8	V	1

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NOTE:

1. Referenced to V_{SS}

DC CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH64400-80	—	95	mA	1, 2, 3
	LH64400-10	—	85		
Supply current in standby mode	I_{CC2}	—	1.0	mA	1
Average supply current in high speed page mode	LH64400-80	—	70	mA	1, 2
	LH64400-10	—	60		
Average supply current in CAS before RAS refresh cycle	LH64400-80	—	95	mA	1, 2, 3
	LH64400-10	—	85		
Average supply current in RAS only refresh cycle	LH64400-80	—	95	mA	1, 2, 3
	LH64400-10	—	85		
Input leakage current	I_{LI}	-10	10	μA	
	$0\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ 0 V on all other pins				
Output leakage current	I_{LO}	-10	10	μA	
	$0\text{ V} \leq V_{OUT} \leq 6.5\text{ V}$ Output in high-impedance state				
Output "High" voltage	V_{OH}	2.4	—	V	
Output "Low" voltage	V_{OL}	—	0.4	V	

NOTES:

1. The output pins are in high-impedance state.
2. I_{CC1} , I_{CC3} , I_{CC5} and I_{CC7} depend on the cycle time.
3. Address transition occurs when $\overline{\text{RAS}} = V_{IH}$ and $\overline{\text{RAS}} = V_{IL}$.

CAPACITANCE ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0$ to 70°C , $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	$A_0 - A_9$	—	5	pF
	$\overline{\text{RAS}}, \overline{\text{CAS}}$	—	5	pF
	$\overline{\text{WE}}, \overline{\text{OE}}$	—	5	pF
Input/output capacitance	$I/O_1 - I/O_4$	—	7	pF

AC CHARACTERISTICS ^{1,2,3,4} (T_A = 0 to +70°C, V_{CC} = 5 V ± 10%)

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PARAMETER	SYMBOL	LH64400-80		LH64400-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
(1) READ CYCLE							
Random read/write cycle time	t _{RC}	140		160		ns	
Access time from RAS	t _{RAC}		80		100	ns	7
Access time from CAS	t _{CAG}		25		30	ns	7
Access time from column address	t _{AA}		40		50	ns	7
Access time from OE	t _{OE}		20		25	ns	7
Row address setup time	t _{ASR}	0		0		ns	
Row address hold time	t _{RAH}	10		15		ns	
Column address setup time	t _{ASC}	0		0		ns	
Column address delay time (RAS)	t _{RAD}	15	40	20	50	ns	5
Column address lead time (RAS)	t _{RAL}	40		50		ns	
Column address hold time (RAS)	t _{CAH}	15		20		ns	
RAS pulse width	t _{RAS}	80	10,000	100	10,000	ns	
RAS precharge time	t _{RP}	50		50		ns	
CAS precharge time (RAS fall)	t _{CRP}	0		0		ns	
CAS delay time (RAS)	t _{RCD}	20	55	25	70	ns	8
CAS lead time (RAS)	t _{RSL}	25		30		ns	
OE command RAS lead time	t _{ROL}	0		0		ns	
Output data disable time (CAS)	t _{OFF}		20		25	ns	
Output data disable time (OE)	t _{OEZ}		20		25	ns	
CAS pulse width	t _{CAS}	25	10,000	30	10,000	ns	
CAS hold time	t _{CSH}	80		100		ns	
Output data hold time (CAS)	t _{SOH}	0		0		ns	
Output data hold time (OE)	t _{OOH}	0		0		ns	
Read command setup time	t _{RCS}	0		0		ns	
Read command hold time (CAS)	t _{RCH}	10		10		ns	8
Read command hold time (RAS rise)	t _{RRH}	10		10		ns	8
Transition time (rise and fall)	t _T	3	50	3	50	ns	
Refresh time interval	t _{REF}		16		16	ms	
(2) HIGH SPEED PAGE MODE READ CYCLE							
High speed page mode cycle time	t _{PC}	50		55		ns	
CAS precharge time	t _{CP}	10		10		ns	
CAS precharge access time (CAS rise)	t _{CACP}	45		50		ns	7, 10
RAS pulse width	t _{RASP}	80	10,000	100	10,000	ns	
High speed page mode read write cycle time	t _{PRWC}	105		115		ns	11
(3) WRITE CYCLE EARLY WRITE)							
Data input setup time	t _{DS}	0		0		ns	
Data input hold time	t _{DH}	15		15		ns	
Write command set-up time	t _{WCS}	0		0		ns	9
Write command hold time	t _{WCH}	10		15		ns	
(OE CONTROL)							
CAS set-up time (WE)	t _{CWS}	0		0		ns	9
Write command lead time (RAS)	t _{RWL}	20		25		ns	
Write command lead time (CAS)	t _{CWL}	20		25		ns	
Write pulse width (WE)	t _{WP}	15		15		ns	
OE hold time (WE)	t _{OEH}	20		20		ns	
(4) READ-WRITE CYCLE							
Read-write cycle time	t _{RWC}	195		225		ns	11
WE delay time (RAS)	t _{RWD}	110		135		ns	11
Column address delay time (WE)	t _{AWD}	70		85		ns	11
WE delay time (CAS)	t _{CWD}	55		65		ns	11
OE delay time	t _{OED}	20		25		ns	
(5) CAS BEFORE RAS REFRESH CYCLE/HIDDEN REFRESH CYCLE							
CAS set-up time (RAS)	t _{CSR}	0		0		ns	
CAS hold time (RAS)	t _{CHR}	20		20		ns	
RAS/CAS precharge time (RAS rise)	t _{RPC}	10		10		ns	
WE precharge time (RAS)	t _{WRP}	0		0		ns	
WE/RAS hold time	t _{WRH}	10		10		ns	
CAS precharge time (RAS fall)	t _{CPN}	10		10		ns	

* See next page for notes.

NOTES:

- For proper operation, at least 200 μ s of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
- AC characteristic assume $t_r = 5$ ns. (t_r refers to the transition time between V_{IH} and V_{IL} .)
- Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
- I_{CC} when power on depends on $\overline{RAS}$ input level.
If $\overline{RAS} = V_{IL}$ when power on, LSI goes into an active cycle and may have a large current I_{CC} . It is recommended to rise $\overline{RAS}$ with V_{CC} or fix at V_{IH} when power on.
- t_{RCD} (MAX.), is the maximum point for t_{RAD} where t_{AA} (Max.) is ensured, and does not represent a limit of operation.
If $t_{RAD} \geq t_{RAD}$ (MAX.), the access time comes under the control of t_{AA} .
- t_{RCD} (MAX.), is the maximum point for t_{RAD} where t_{AC} (MAX.) is ensured, and does not represent a limit of operation.
If $t_{RCD} \geq t_{RCD}$ (MAX.), the access time will come under the control of t_{AC} .
- 2TTL + 100 pF load.
- The operation is ensured when either t_{RCH} or t_{RDH} is satisfied.
- t_{WCS} is not a restrictive operating parameter. It comes into early write cycle with the $\overline{WE} = \text{"Low"}$ at the falling edge of $\overline{CAS}$. Then, I/O pins remain inactive until the $\overline{CAS} = \text{"High"}$ irrespective of $\overline{WE}$.
- If $t_{ACAP} \geq t_{CP} + t_{AC} + t_r$, the access time depends upon t_{ACAP} .
- t_{RW} , t_{WD} , t_{WD} , t_{WD} and t_{RWC} are not restrictive operating parameters.

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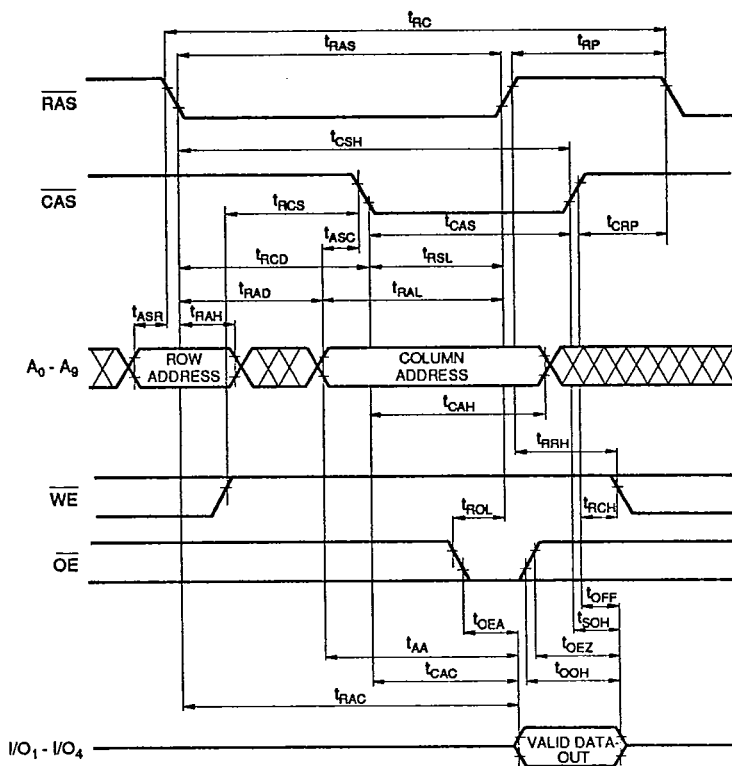
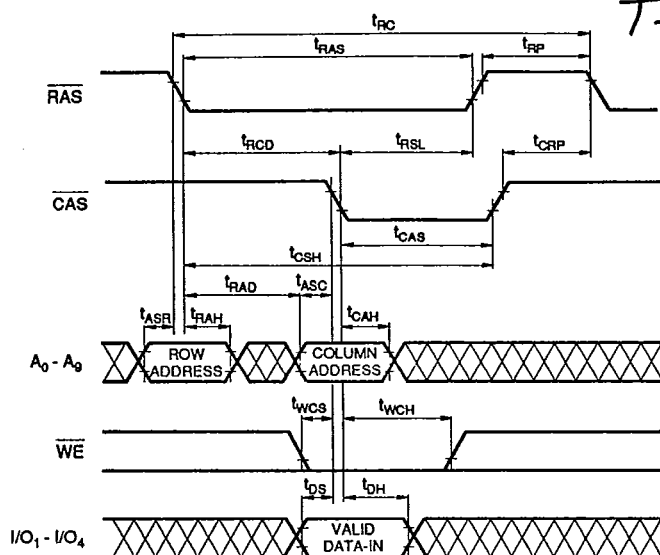


Figure 3. Read Cycle

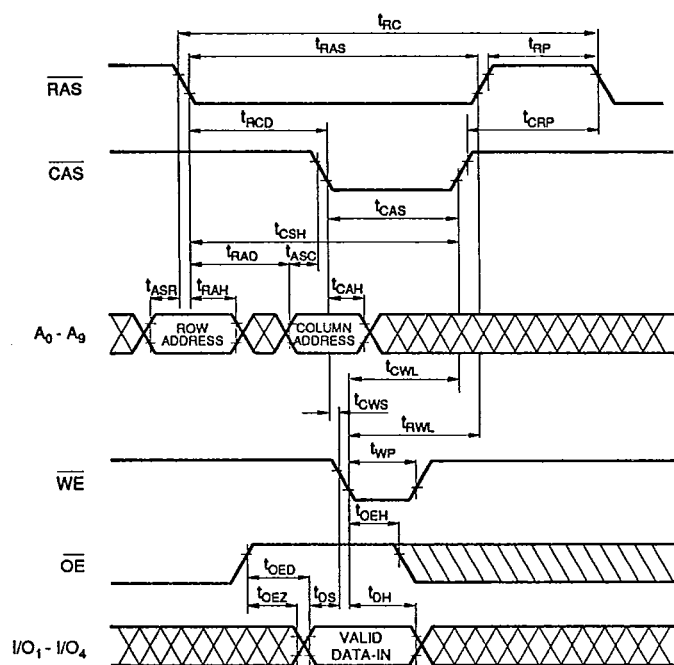
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NOTE: OE = Don't care

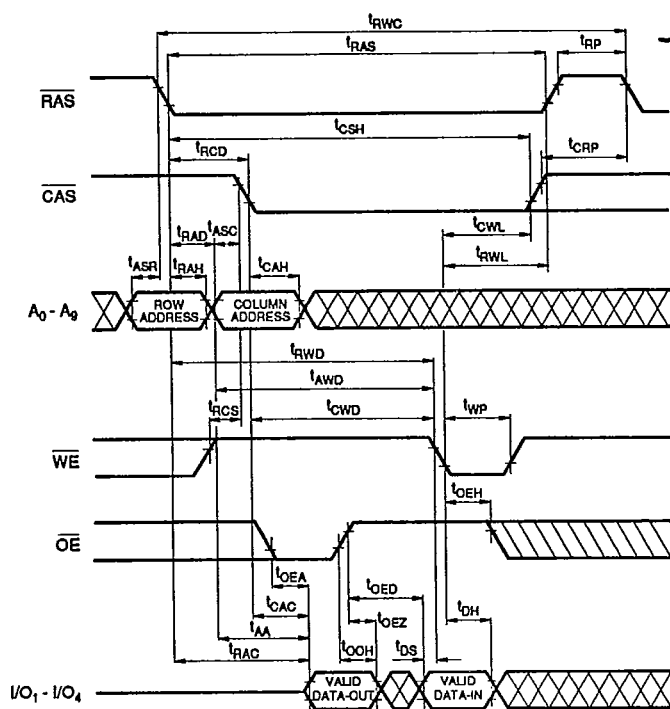
64400-4

Figure 4. Write Cycle (Early Write)



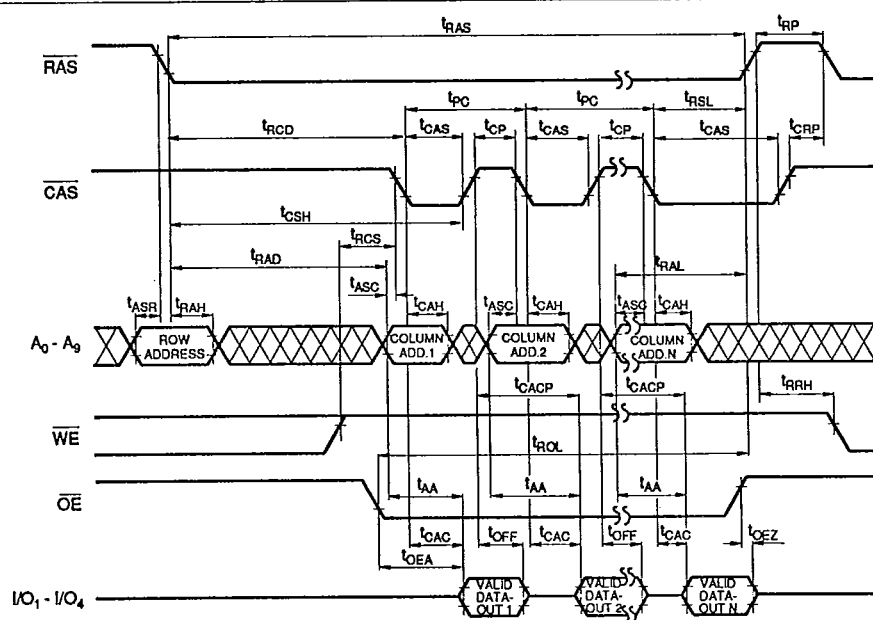
64400-5

Figure 5. Write Cycle (OE Control)



64400-6

Figure 6. Read/Write Cycle



64400-7

Figure 7. High Speed Page Mode Read Cycle

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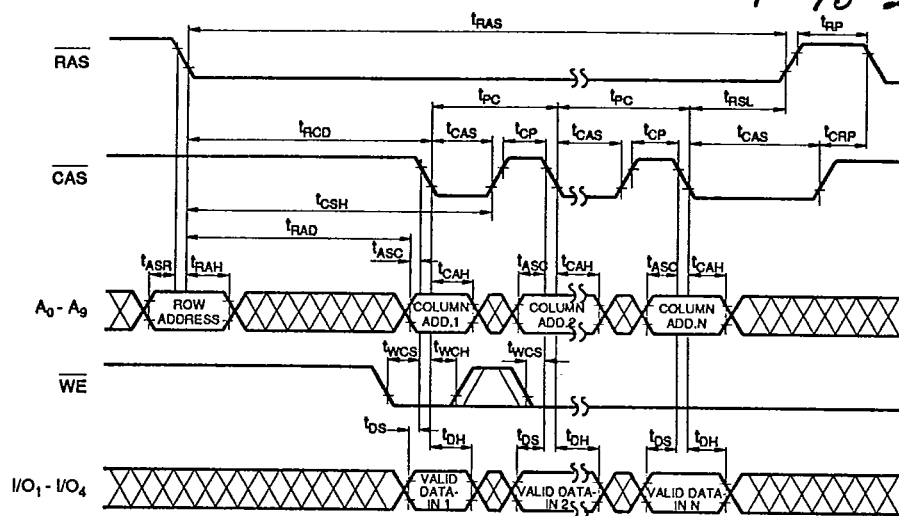


Figure 8. High Speed Page Mode Write Cycle

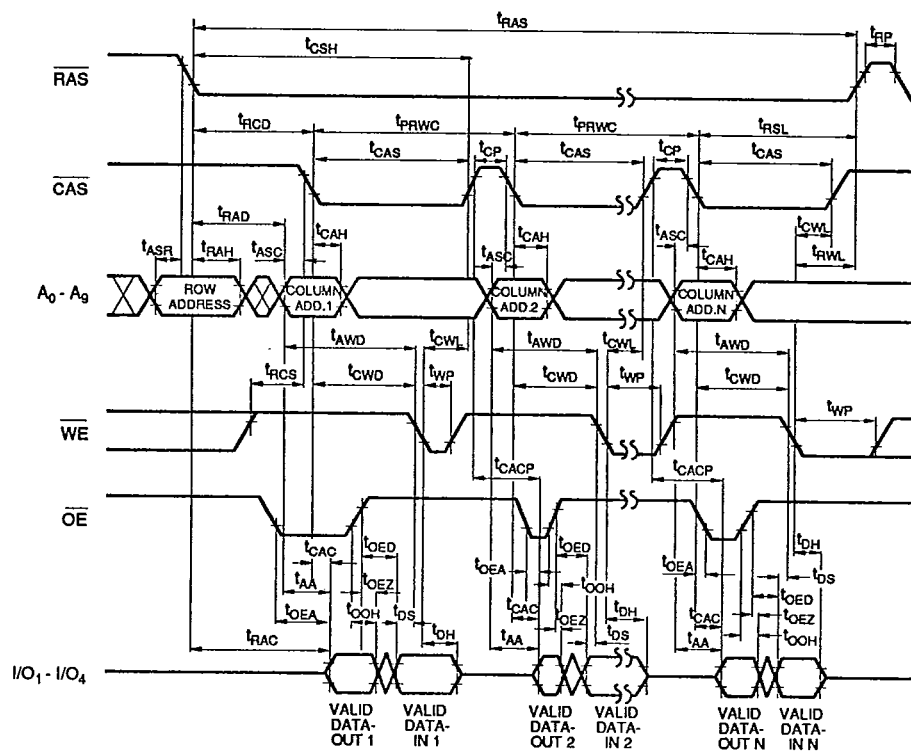
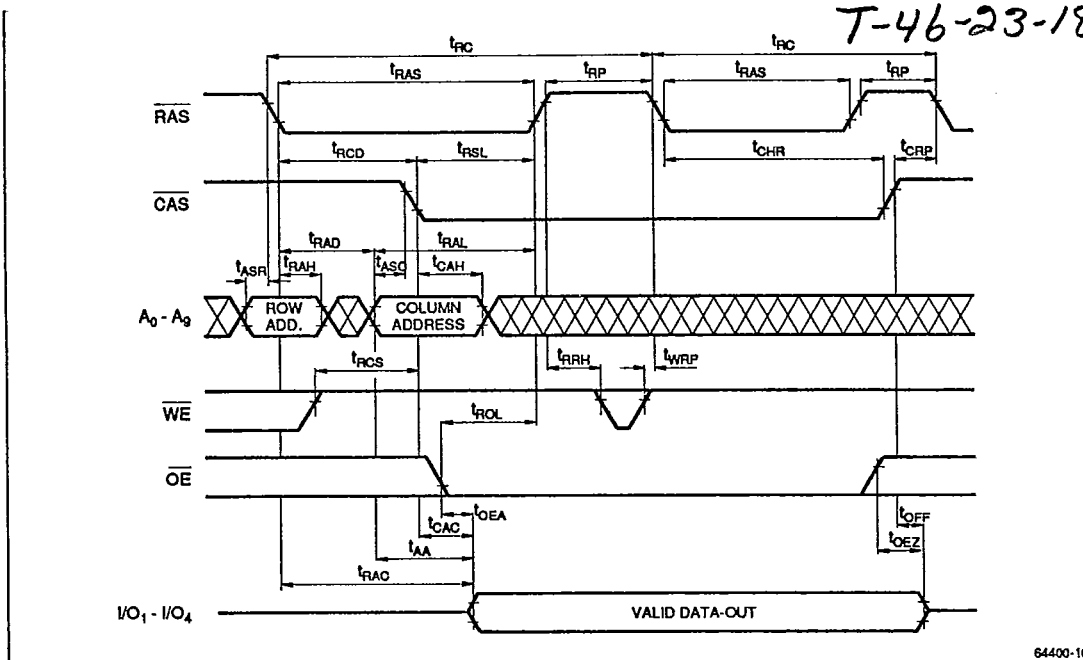


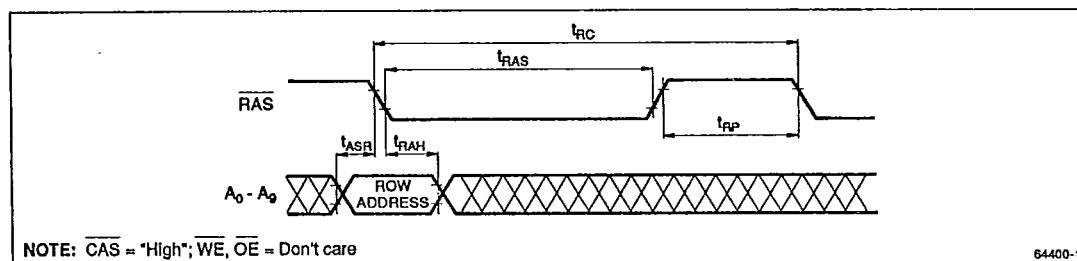
Figure 9. High Speed Page Mode Write Cycle

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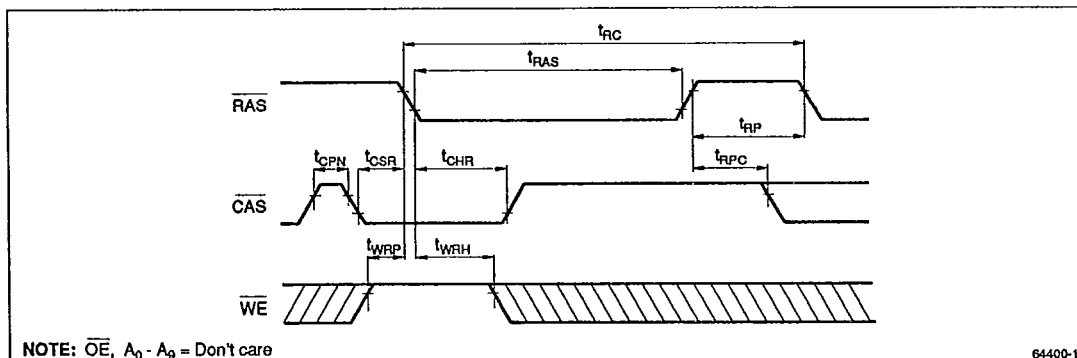
64400-10

Figure 10. Hidden Refresh Cycle



NOTE: CAS = "High"; WE, OE = Don't care

64400-11

Figure 11. $\overline{\text{RAS}}$ Only Refresh CycleNOTE: $\overline{\text{OE}}$, $A_0 - A_9$ = Don't care

64400-12

Figure 12. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

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LH64400 Device Type	X Package	- ## Speed	
		80 80 10 100	Access Time (ns)
			Blank 20-pin, 300-mil DIP (DIP 20-P-300A)
			K 26-pin, 300-mil SOJ (SOJ26-P-300)
			Z 20-pin, 400-mil ZIP (ZIP 20-P-400)
			S 26-pin TSOP (TSOP26-P-300 type II) Normal bend
			SR 26-pin TSOP (TSOP26-P-300 type II) Reverse bend
			CMOS 4M (1M x 4) Dynamic RAM

Example: LH64400K-80 (CMOS 4M (1M x 4) Dynamic RAM, 80 ns, 26-pin, 300-mil SOJ)

64400-13