4GB: 512Mx72 / 8GB: 1024Mx72 / 16GB: 2048M x 72
PC3-10600 / PC3-12800 / PC3-14900
Registered DDR3 SDRAM DIMM

Based on DDR3-1333/1600/1866 512Mx8/1024Mx4 (4GB/8GB/16GB) SDRAM B-Die

Features

•Performance:

Speed Sort	PC3-10600	PC3-12800	PC3-14900	Unit
	-CG	-DI	-EK	
DIMM CAS Latency	9	11	13	
fck – Clock Frequency	667	800	933	MHz
tck – Clock Cycle	1.5	1.25	1.07	ns
fDQ – DQ Burst Frequency	1333	1600	1866	Mbps

- 240-Pin Registered Dual In-Line Memory Module (RDIMM)
- 4GB/8GB: 512Mx72/1024Mx72 DDR3 Registered DIMM based on 512Mx8 DDR3 SDRAM B-Die devices
- 8GB/16GB: 1024Mx72/2048Mx72 DDR3 Registered DIMM based on 1024Mx4 DDR3 SDRAM B-Die devices
- Intended for 667MHz/800MHz/933MHz applications
- Inputs and outputs are SSTL-15 compatible
- $V_{DD} = V_{DDQ}$ = 1.5V ± 0.075V (for DDR3)
- $V_{DD} = V_{DDQ}$ = 1.35V -0.0675/+0.1V (for DDR3L) (Backward Compatible to VDD = VDDQ = 1.5V±0.075V)
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Nominal and Dynamic On-Die Termination support
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 5,6,7,8,9,10,11
  - Burst Type: Sequential or Interleave
  - Burst Length: BC4, BL8
  - Operation: Burst Read and Write
- Two different termination values (Rtt_Nom & Rtt_WR)
- 16/10/1 (row/column/rank) Addressing for 4GB
- 16/10/2 (row/column/rank) Addressing for 8GB(512Mx8 Device)
- 16/11/1 (row/column/rank) Addressing for 8GB(1024Mx4 Device)
- 16/11/2 (row/column/rank) Addressing for 16GB
- Extended operating temperature rage
- Auto Self-Refresh option
- Serial Presence Detect
- Gold contacts
- SDRAMs are in 78-ball BGA Package
- RoHS compliance and Halogen free

Description

NT4GC72B89B0NL(K) / NT4GC72C89B0NL(K) / NT8GC72B4PB0NL(K) / NT8GC72C4PB0NL(K) / NT8GC72B8PB0NL(K) / NT8GC72C8PB0NL(K) / NT16GC72B4NB0NL(K) and NT16GC72C4NB0NL(K) are 240-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Registered Dual In-Line Memory Module, organized as one rank of 512Mx72 (4GB), one rank or two ranks of 1024Mx72 (8GB) and two ranks of 2048Mx72 (16GB) high-speed memory array. Modules use nine 512Mx8 (4GB) 78-ball BGA packaged devices, eighteen 512Mx8/1024Mx4 (8GB) 78-ball BGA packaged devices and thirty-six 1024Mx4 (16GB) 78-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR3 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

The DIMM is intended for use in applications operating of 667MHz/800MHz/933MHz clock speeds and achieves high-speed data transfer rates of 1333Mbps/1600Mbps/1866Mbps. Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A15 and I/O inputs BA0~BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Power	Leads	Note
NT4GC72B89B0NL(K)-DI	DDR3-1600	PC3-12800	800MHz (1.25ns @ CL = 11)	512Mx72	1.5V	Gold	
NT8GC72B4PB0NL(K)-DI	DDR3-1600	PC3-12800	800MHz (1.25ns @ CL = 11)	1024Mx72			
NT8GC72B8PB0NL(K)-DI	DDR3-1600	PC3-12800	800MHz (1.25ns @ CL = 11)				
NT16GC72B4NB0NL(K)-DI	DDR3-1600	PC3-12800	800MHz (1.25ns @ CL = 11)	2048Mx72			
NT16GC72B4NB0NL(K)-EK	DDR3-1866	PC3-14900	933MHz (1.07ns @ CL = 13)				
NT4GC72C89B0NL(K)-CG	DDR3L-1333	PC3-10600	667MHz (1.5ns @ CL = 9)	512Mx72	1.35V		
NT8GC72C4PB0NL(K)-CG	DDR3L-1333	PC3-10600	667MHz (1.5ns @ CL = 9)	1024Mx72			
NT8GC72C8PB0NL(K)-CG	DDR3L-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				
NT16GC72C4NB0NL(K)-CG	DDR3L-1333	PC3-10600	667MHz (1.5ns @ CL = 9)	2048Mx72			
NT4GC72C89B0NL(K)-DI	DDR3L-1600	PC3-12800	800MHz (1.25ns @ CL = 11)	512Mx72			
NT8GC72C4PB0NL(K)-DI	DDR3L-1600	PC3-12800	800MHz (1.25ns @ CL = 11)	1024Mx72			
NT8GC72C8PB0NL(K)-DI	DDR3L-1600	PC3-12800	800MHz (1.25ns @ CL = 11)				
NT16GC72C4NB0NL(K)-DI	DDR3L-1600	PC3-12800	800MHz (1.25ns @ CL = 11)	2048Mx72			

Note : L is Inphi Register, K is IDT Register.

Pin Description

Pin Name	Description	Pin Name	Description
CK0, CK1	Clock Inputs, positive line	ODT0, ODT1	Active termination control lines
$\overline{CK0}$, $\overline{CK1}$	Clock Inputs, negative line	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS17	Data strobes
$\overline{RAS}$	Row Address Strobe	$\overline{DQS0}$-$\overline{DQS17}$	Data strobes complement
$\overline{CAS}$	Column Address Strobe	TDQS9-TDQS17	Termination data strobes
$\overline{WE}$	Write Enable	$\overline{TDQS9}$-$\overline{TDQS17}$	Termination data strobes
$\overline{S0}$-$\overline{S3}$	Chip Selects	DM0-DM8	Data Masks
A0-A9, A11, A13-A15	Address Inputs	CB0-CB7	ECC Check Bits
A10/AP	Address Input/Auto-Precharge	$\overline{EVENT}$	Temperature event pin
A12/$\overline{BC}$	Address Input/Burst Chop	$\overline{RESET}$	Reset pin
BA0-BA2	SDRAM Bank Address Inputs	V_{REFDQ} , V_{REFCA}	Input/Output Reference
SCL	Serial Presence Detect Clock Input	V_{DDSPD}	SPD and Temp sensor power
SDA	Serial Presence Detect Data input/output	SA0, SA1, SA2	Serial Presence Detect Address Inputs
Par_In	Parity bit for the Address and Control bus	Vtt	Termination voltage
$\overline{Err\_Out}$	Parity error found on the Address and Control bus	V_{SS}	Ground
NC	No Connect	V_{DD}	Core and I/O power

DDR3 SDRAM Pin Assignment

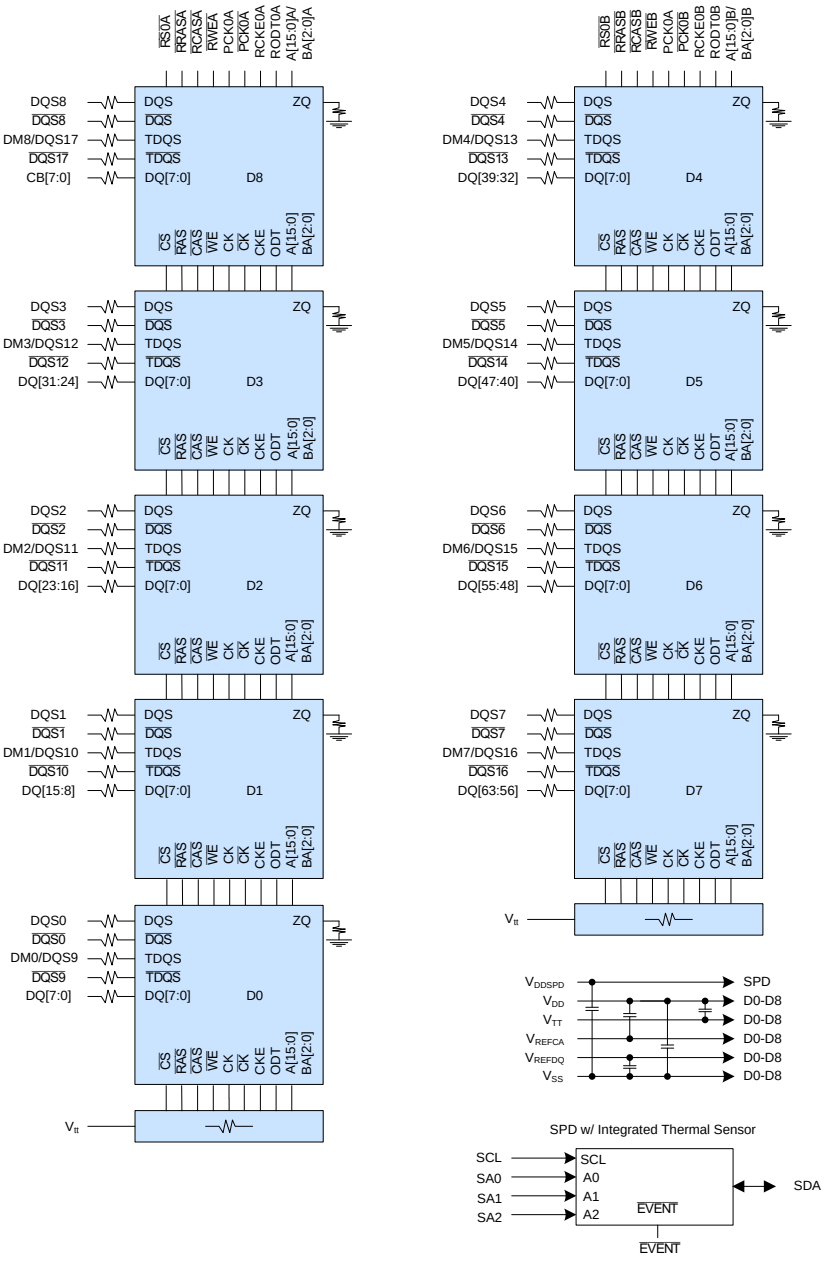
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	121	V_{SS}	31	DQ25	151	V_{SS}	61	A2	181	A1	91	DQ41	211	V_{SS}
2	V_{SS}	122	DQ4	32	V_{SS}	152	DM3/DQS12 /TDQS12	62	V_{DD}	182	V_{DD}	92	V_{SS}	212	DM5/DQS14 /TDQS14
3	DQ0	123	DQ5	33	$\overline{DQS3}$	153	NC/$\overline{DQS12}$ /$\overline{TDQS12}$	63	NC	183	V_{DD}	93	$\overline{DQS5}$	213	NC/$\overline{DQS14}$ /$\overline{TDQS14}$
4	DQ1	124	V_{SS}	34	DQS3	154	V_{SS}	64	NC	184	CK0	94	DQS5	214	V_{SS}
5	V_{SS}	125	DM0/DQS9/ TDQS9	35	V_{SS}	155	DQ30	65	V_{DD}	185	$\overline{CK0}$	95	V_{SS}	215	DQ46
6	$\overline{DQS0}$	126	NC/$\overline{DQS9}$ /$\overline{TDQS9}$	36	DQ26	156	DQ31	66	V_{DD}	186	V_{DD}	96	DQ42	216	DQ47
7	DQS0	127	V_{SS}	37	DQ27	157	V_{SS}	67	V_{REFCA}	187	$\overline{EVENT}$	97	DQ43	217	V_{SS}
8	V_{SS}	128	DQ6	38	V_{SS}	158	CB4	68	Par_In/NC	188	A0	98	V_{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0	159	CB5	69	V_{DD}	189	V_{DD}	99	DQ48	219	DQ53
10	DQ3	130	V_{SS}	40	CB1	160	V_{SS}	70	A10/AP	190	BA1	100	DQ49	220	V_{SS}
11	V_{SS}	131	DQ12	41	V_{SS}	161	DM8/DQS17 /TDQS17	71	BA0	191	V_{DD}	101	V_{SS}	221	DM6/DQS15 /TDQS15
12	DQ8	132	DQ13	42	$\overline{DQS8}$	162	NC/$\overline{DQS17}$ /$\overline{TDQS17}$	72	V_{DD}	192	$\overline{RAS}$	102	$\overline{DQS6}$	222	NC/$\overline{DQS15}$ /$\overline{TDQS15}$
13	DQ9	133	V_{SS}	43	DQS8	163	V_{SS}	73	$\overline{WE}$	193	$\overline{S0}$	103	DQS6	223	V_{SS}
14	V_{SS}	134	DM1/DQS10 /TDQS10	44	V_{SS}	164	CB6	74	$\overline{CAS}$	194	V_{DD}	104	V_{SS}	224	DQ54
15	$\overline{DQS1}$	135	NC/$\overline{DQS10}$ /$\overline{TDQS10}$	45	CB2	165	CB7	75	V_{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	V_{SS}	46	CB3	166	V_{SS}	76	$\overline{S1}$/NC	196	A13	106	DQ51	226	V_{SS}
17	V_{SS}	137	DQ14	47	V_{SS}	167	NC	77	ODT1/NC	197	V_{DD}	107	V_{SS}	227	DQ60
18	DQ10	138	DQ15	48	V_{TT}/NC	168	$\overline{RESET}$	78	V_{DD}	198	$\overline{S3}$/NC	108	DQ56	228	DQ61
19	DQ11	139	V_{SS}	49	V_{TT}/NC	169	CKE1/NC	79	$\overline{S2}$/NC	199	V_{SS}	109	DQ57	229	V_{SS}
20	V_{SS}	140	DQ20	50	CKE0	170	V_{DD}	80	V_{SS}	200	DQ36	110	V_{SS}	230	DM7/DQS16 /TDQS16
21	DQ16	141	DQ21	51	V_{DD}	171	A15	81	DQ32	201	DQ37	111	$\overline{DQS7}$	231	NC/$\overline{DQS16}$ /$\overline{TDQS16}$
22	DQ17	142	V_{SS}	52	BA2	172	A14	82	DQ33	202	V_{SS}	112	DQS7	232	V_{SS}
23	V_{SS}	143	DM2/DQS11 /TDQS11	53	$\overline{Err\_Out}$/NC	173	V_{DD}	83	V_{SS}	203	DM4/DQS13 /TDQS13	113	V_{SS}	233	DQ62
24	$\overline{DQS2}$	144	NC/$\overline{DQS11}$ /$\overline{TDQS11}$	54	V_{DD}	174	A12/$\overline{BC}$	84	$\overline{DQS4}$	204	NC/$\overline{DQS13}$ /$\overline{TDQS13}$	114	DQ58	234	DQ63
25	DQS2	145	V_{SS}	55	A11	175	A9	85	DQS4	205	V_{SS}	115	DQ59	235	V_{SS}
26	V_{SS}	146	DQ22	56	A7	176	V_{DD}	86	V_{SS}	206	DQ38	116	V_{SS}	236	V_{DDSPD}
27	DQ18	147	DQ23	57	V_{DD}	177	A8	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V_{SS}	58	A5	178	A6	88	DQ35	208	V_{SS}	118	SCL	238	SDA
29	V_{SS}	149	DQ28	59	A4	179	V_{DD}	89	V_{SS}	209	DQ44	119	SA2	239	V_{SS}
30	DQ24	150	DQ29	60	V_{DD}	180	A3	90	DQ40	210	DQ45	120	V_{TT}	240	V_{TT}

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1 $\overline{CK0}$, $\overline{CK1}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock. However, CK1 and $\overline{CK1}$ are terminated but not used on RDIMMs.
CKE0, CKE1	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$ – $\overline{S3}$	Input	Active Low	Enable the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, $\overline{S2}$ and $\overline{S3}$ operate similarly to $\overline{S0}$ and $\overline{S1}$ for the second set of register outputs or register control words.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
ODT0, ODT1	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0 – DQS17 $\overline{DQS0}$ – $\overline{DQS17}$	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the cross point of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to V_{SS} and DDR3 SDRAM mode registers programmed appropriately.
TDQS9 – TDQS17 $\overline{TDQS9}$ – $\overline{TDQS17}$	Output		TDQS/$\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via mode register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function $\overline{TDQS}$ is not used. X4/x16 DRAMs must disable the TDQS function via mode register A11=0 in MR1.
BA0, BA1, BA2	Input	-	Selects which DDR3 SDRAM internal bank of four or eight is activated.
A0 – A9 A10/AP A11 A12/$\overline{BC}$ A13-A15	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0 – DQ63	Input	-	Data Input/Output pins.
CB0 – CB7	I/O	-	Check bits are used for ECC.
V_{DD}, V_{DDSPD}, V_{SS}	Supply	-	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ}, V_{REFCA}	Supply	-	Reference voltage for SSTL15 inputs.
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and temp sensor. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0 – SA2	Input	-	Address pins used to select the Serial Presence Detect and Temp sensor base address.
$\overline{EVENT}$	Output	-	The $\overline{EVENT}$ pin is reserved for use to flag critical module temperature.
$\overline{RESET}$	Input	-	This signal resets the DDR3 SDRAM.
Par_In	Input	-	Parity bit for the Address and Control bus.
$\overline{Err\_Out}$	Output	-	Parity error detected on the Address and Control bus. A resistor may be connected from bus line to V_{DD} on the system planar to act as a pull up.

Functional Block Diagram (Part 1 of 2)

[4GB – 1 Rank, 512Mx8 DDR3 SDRAMs]

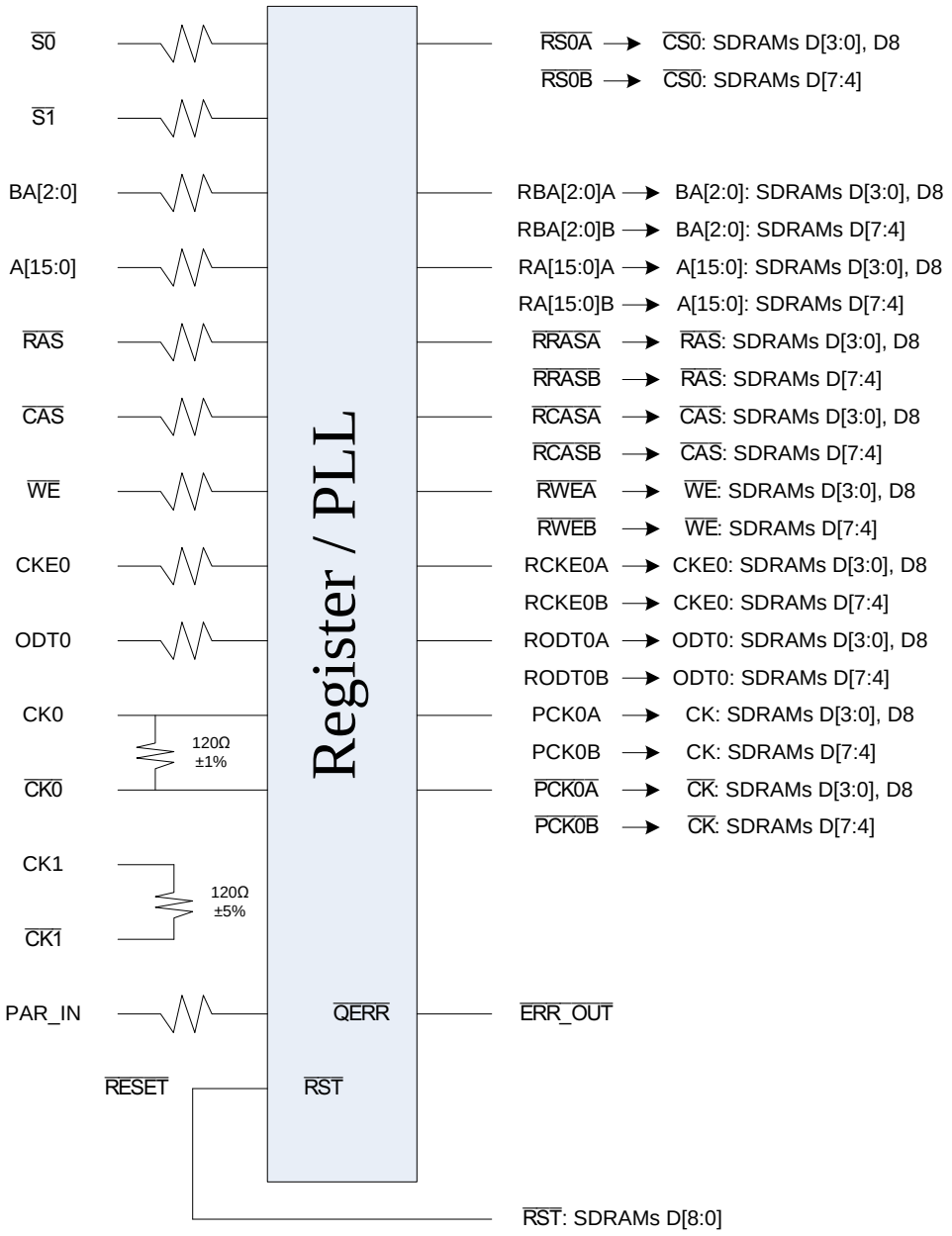


Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.

Functional Block Diagram (Part 2 of 2)

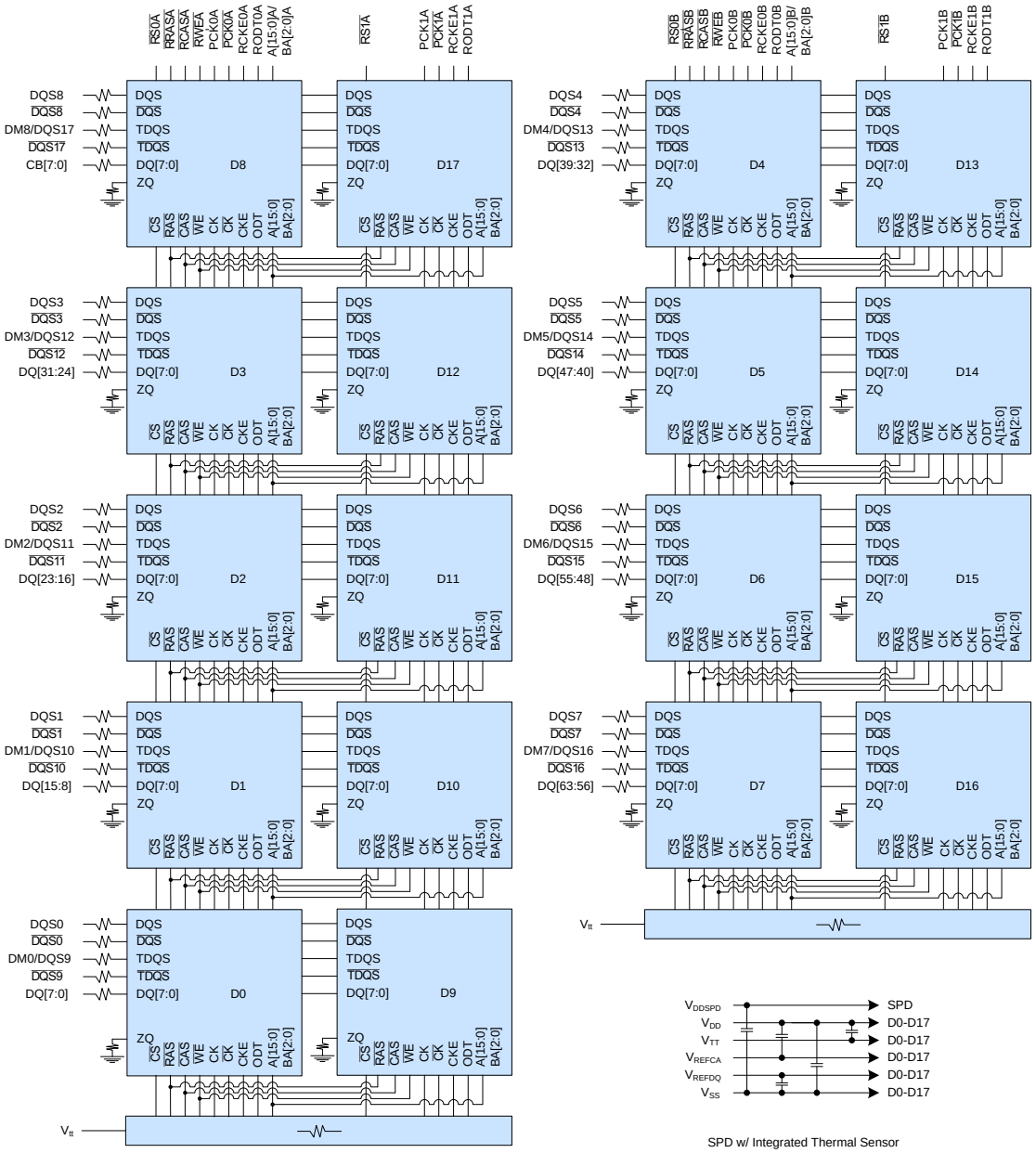
[4GB – 1 Rank, 512Mx8 DDR3 SDRAMs]



Note: S[3:2], CKE1, ODT1 are NC
(Unused register inputs ODT1 and CKE1 have a 330Ω resistor to ground)

Functional Block Diagram (Part 1 of 2)

[8GB – 2 Ranks, 512Mx8 DDR3 SDRAMs]

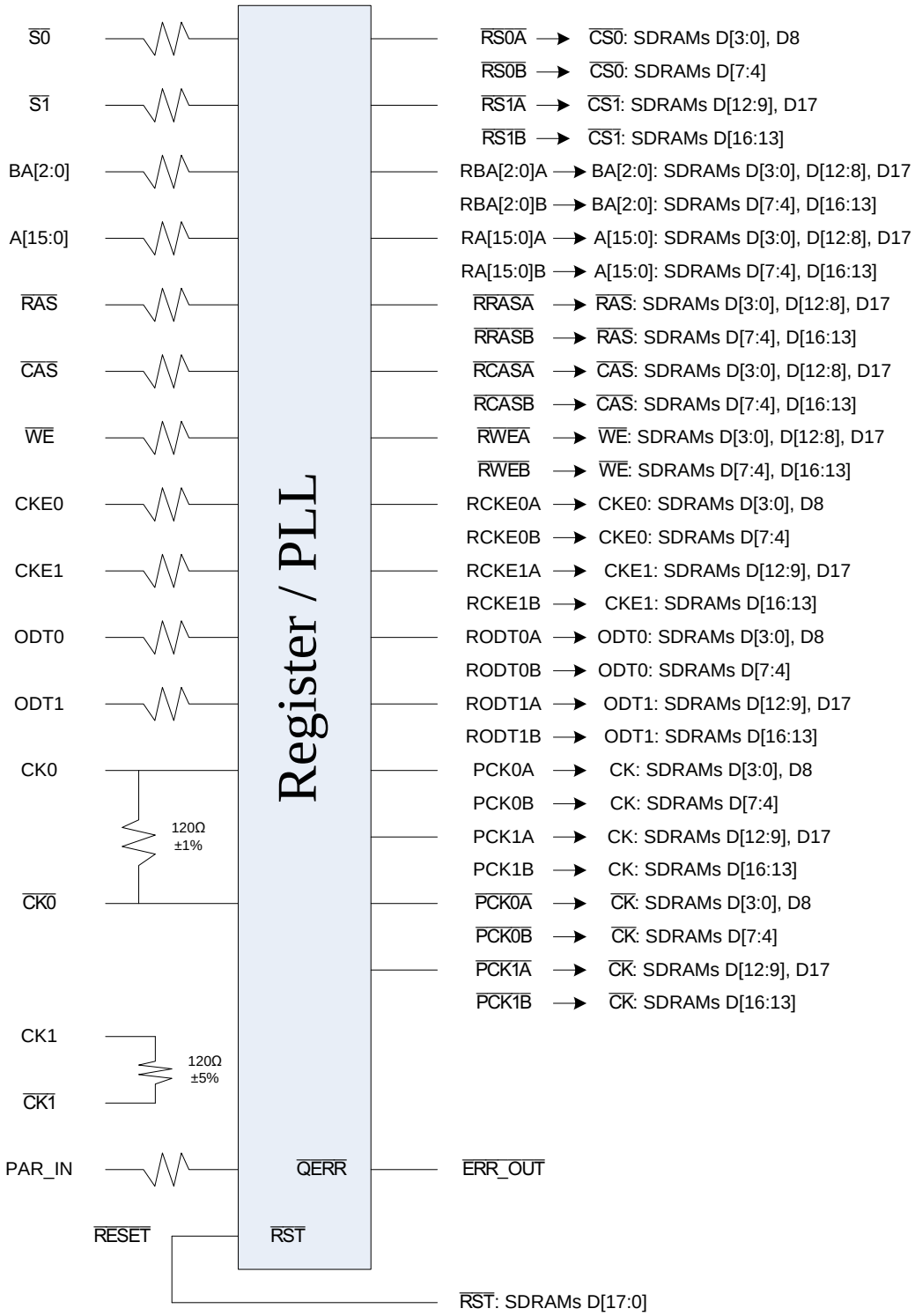


Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
3. Unless otherwise noted, resistor values are 15Ω ± 5%.
4. See the wiring diagrams for all resistors associated with the command, address and control bus.

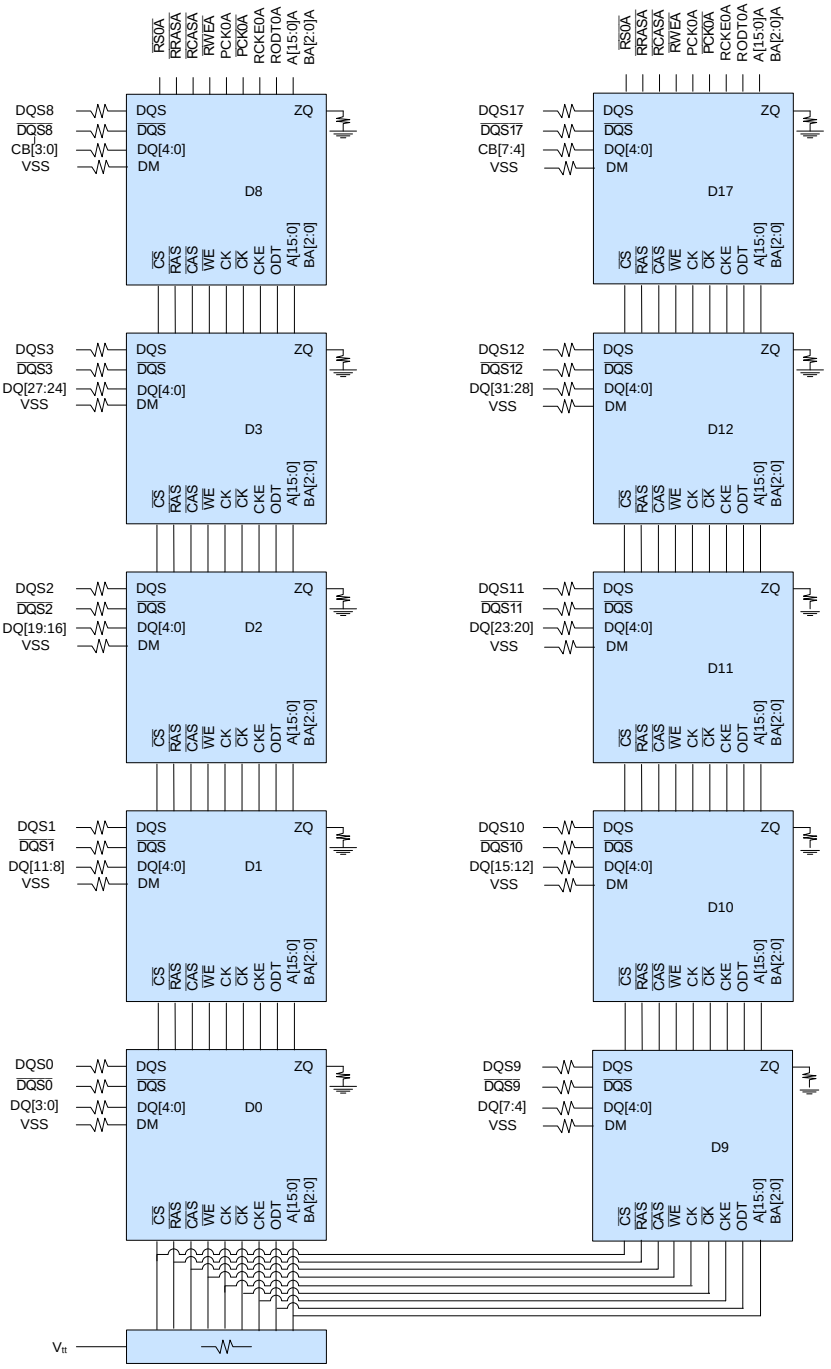
Functional Block Diagram (Part 2 of 2)

[8GB – 2 Ranks, 512Mx8 DDR3 SDRAMs]



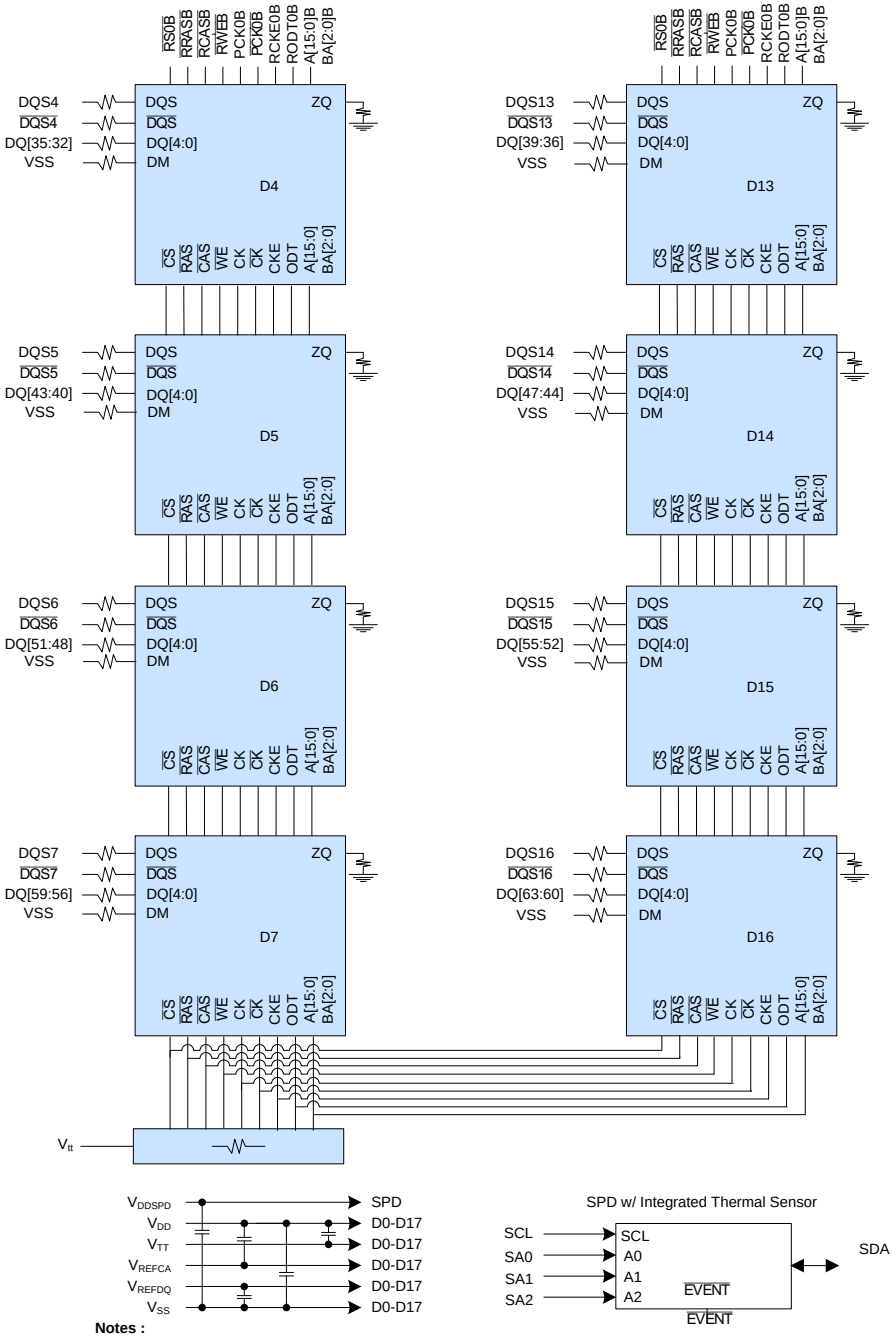
Functional Block Diagram (Part 1 of 3)

[8GB – 1 Rank, 1024Mx4 DDR3 SDRAMs]



Functional Block Diagram (Part 2 of 3)

[8GB – 1 Rank, 1024Mx4 DDR3 SDRAMs]

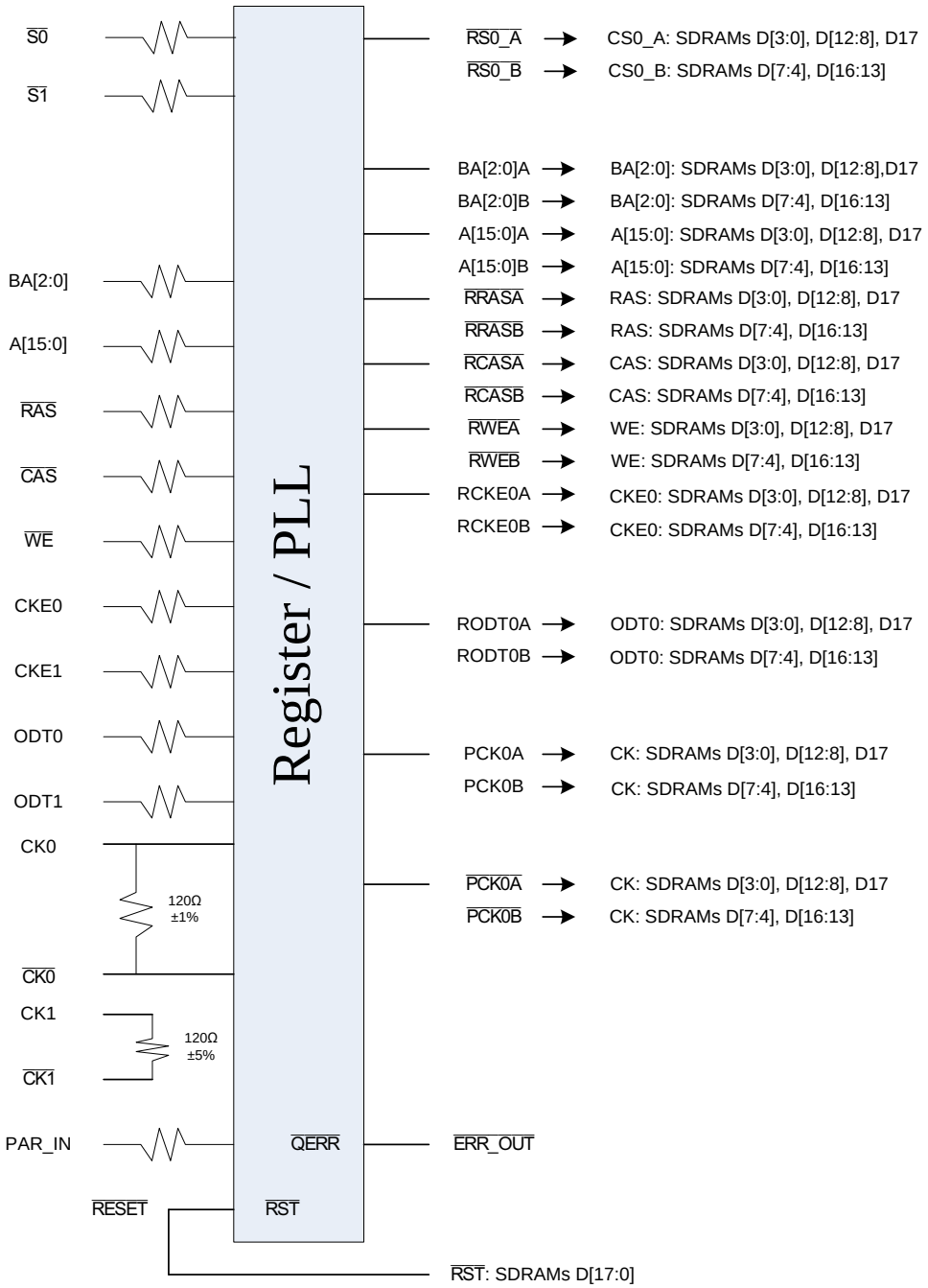


Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
3. Unless otherwise noted, resistor values are 15Ω ± 5%.
4. See the wiring diagrams for all resistors associated with the command, address and control bus.

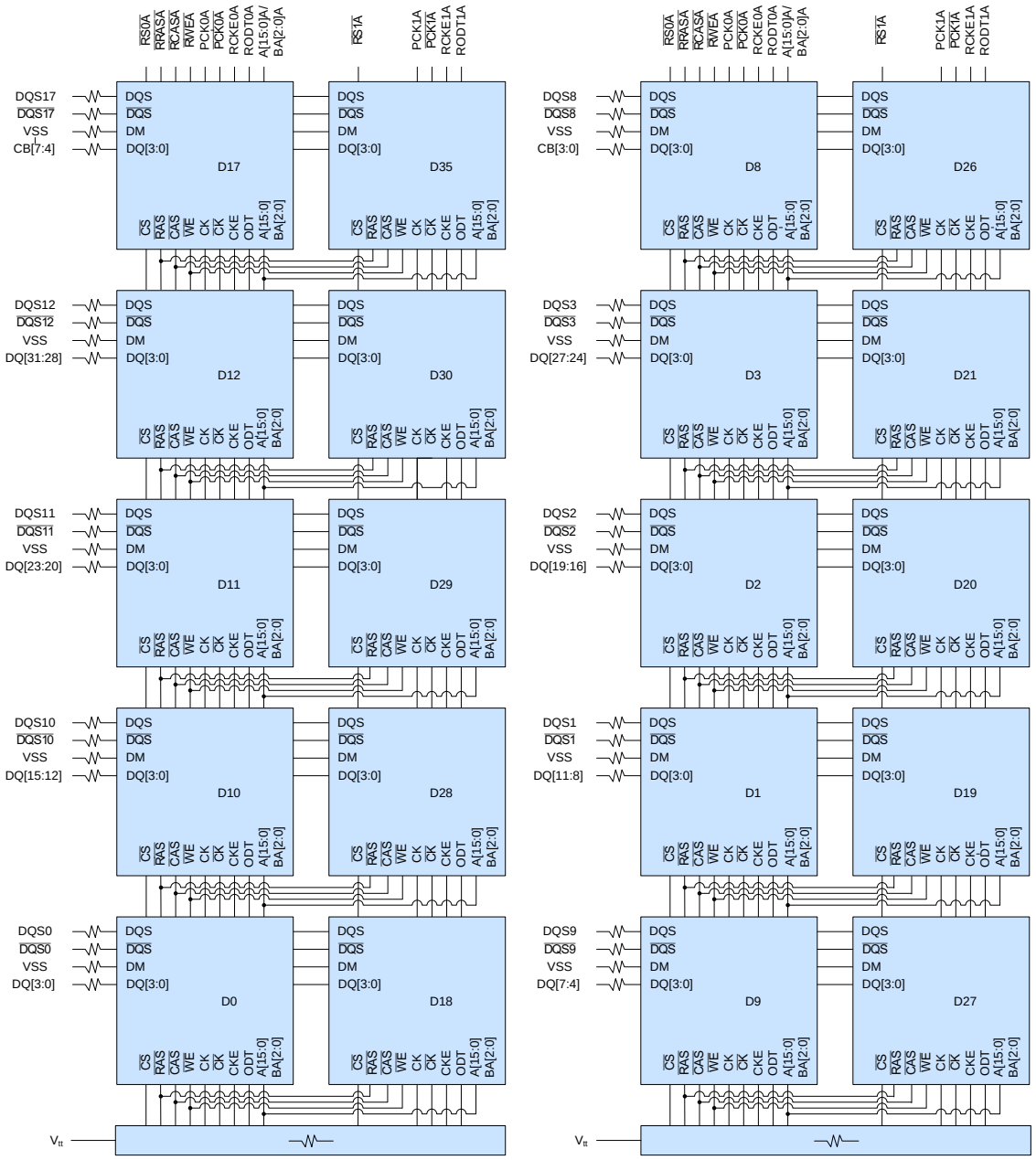
Functional Block Diagram (Part 3 of 3)

[8GB – 1 Rank, 1024Mx4 DDR3 SDRAMs]



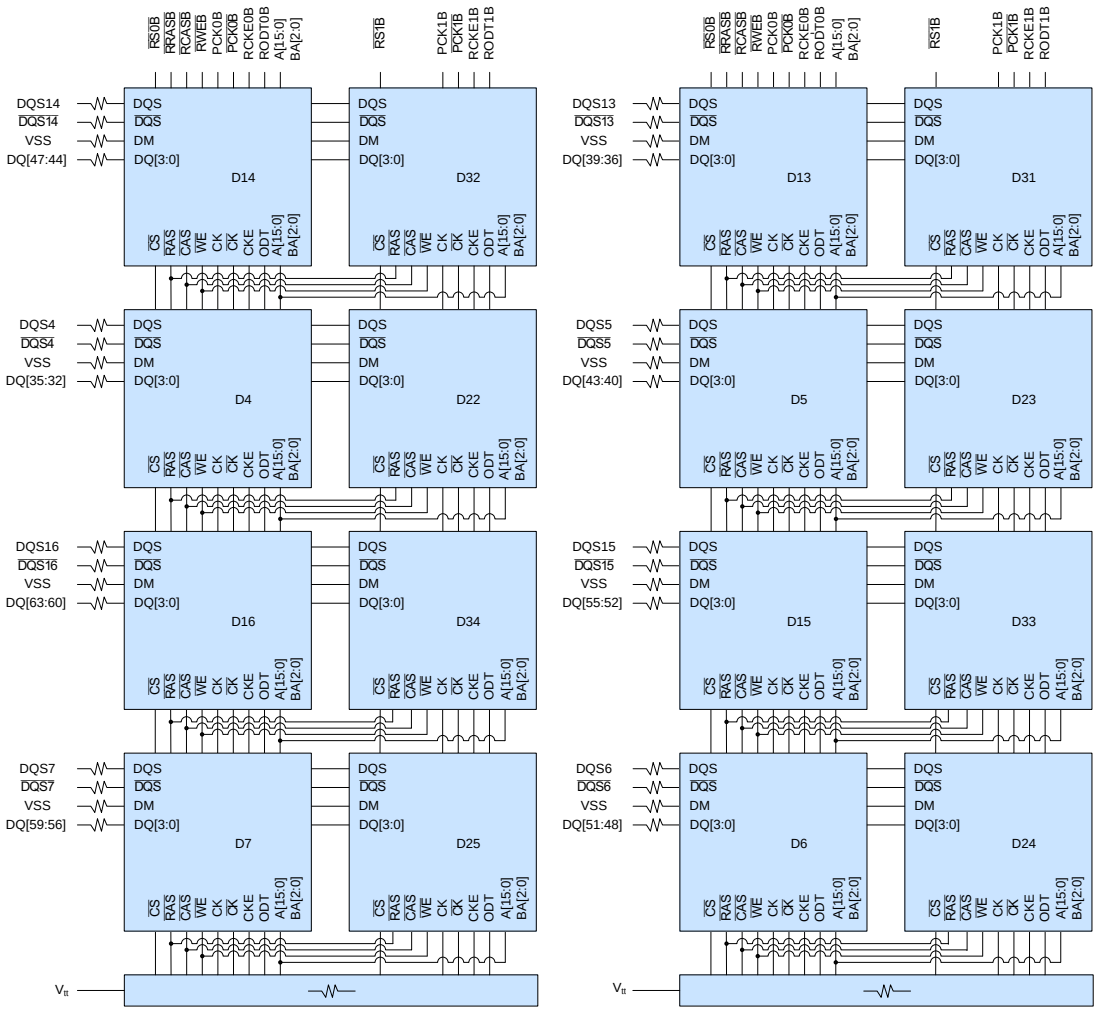
Functional Block Diagram (Part 1 of 3)

[16GB – 2 Ranks, 1024Mx4 DDR3 SDRAMs]



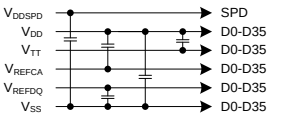
Functional Block Diagram (Part 2 of 3)

[16GB – 2 Ranks, 1024Mx4 DDR3 SDRAMs]

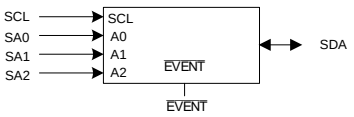


Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ pins of each SDRAM are connected to individual RZQ resistors (240Ω ± 1%).
3. See the wiring diagrams for resistor values.

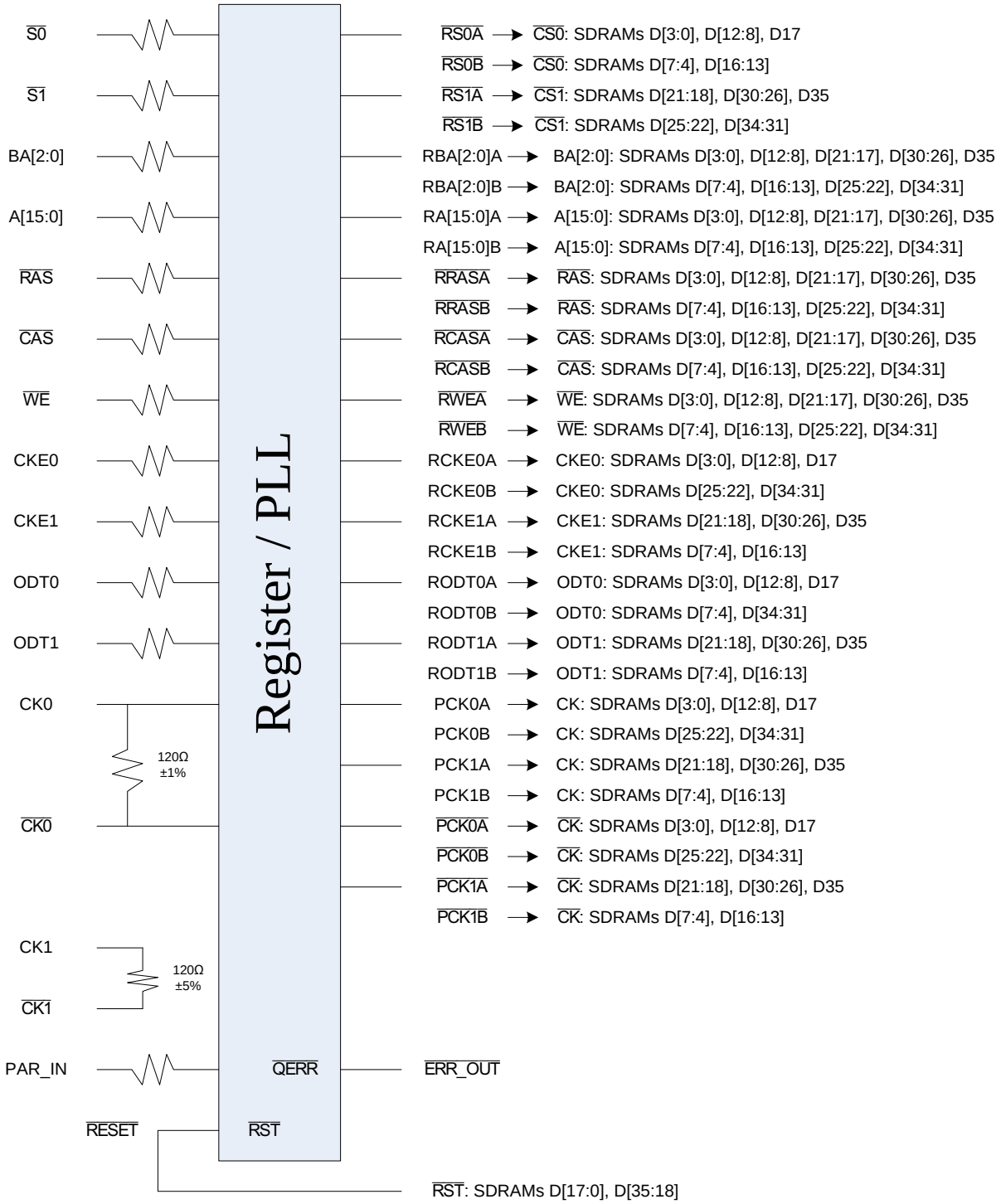


SPD w/ Integrated Thermal Sensor



Functional Block Diagram (Part 3 of 3)

[16GB – 2 Ranks, 1024Mx4 DDR3 SDRAMs]



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Environmental Requirements

Symbol	Parameter	Rating	Units	Note
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
V_{DD}	Voltage on VDD pins relative to Vss	-0.4 V ~ 1.975 V	V	1, 3
V_{DDQ}	Voltage on VDDQ pins relative to Vss	-0.4 V ~ 1.975 V	V	1, 3
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1, 2
	Extended Temperature Range (Optional)	85 to 95	°C	1, 3

Note:
1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Type	Max	Units	Notes
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Output Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DD}	Supply Voltage	1.28	1.35	1.45	V	DDR3L
V_{DDQ}	Output Supply Voltage	1.28	1.35	1.45	V	DDR3L

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-1066 (BE)		DDR3-1333 (CG)		DDR3-1600(DI)		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
VIH.CA(DC)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1, 5
VIL.CA(DC)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1, 6
VIH.CA(AC)	AC Input Logic High	Vref + 0.175	Note 2	Vref + 0.175	Note 2	Vref + 0.175	Note 2	V	1, 2, 7
VIL.CA(AC)	AC Input Logic Low	Note 2	Vref - 0.175	Note 2	Vref - 0.175	Note 2	Vref - 0.175	V	1, 2, 8
VIH.CA(AC150)	AC Input Logic High	Vref + 0.15	Note 2	Vref + 0.15	Note 2	Vref + 0.15	Note 2	V	1, 2, 7
VIL.CA(AC150)	AC Input Logic Low	Note 2	Vref - 0.15	Note 2	Vref - 0.15	Note 2	Vref - 0.15	V	1, 2, 8
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:
1. For input only pins except RESET#. Vref = VrefCA(DC).
2. See 9.6 “Overshoot and Undershoot Specifications” on page 126.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefCA(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.CA(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.CA(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.CA(AC175) and VIH.CA(AC150); VIH.CA(AC175) value is used when Vref + 0.175V is referenced and VIH.CA(AC150) value is used when Vref + 0.150V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.CA(AC175) and VIL.CA(AC150); VIL.CA(AC175) value is used when Vref - 0.175V is referenced and VIL.CA(AC150) value is used when Vref - 0.150V is referenced.

Symbol	Parameter	DDR3L-1066 (BE)		DDR3L-1333 (CG)		DDR3L-1600(DI)		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
VIH.CA(DC90)	DC Input Logic High	Vref + 0.09	VDD	Vref + 0.09	VDD	Vref + 0.09	VDD	V	1
VIL.CA(DC90)	DC Input Logic Low	VSS	Vref - 0.09	VSS	Vref - 0.09	VSS	Vref - 0.09	V	1
VIH.CA(AC160)	AC Input Logic High	Vref + 0.160	Note 2	Vref + 0.160	Note 2	Vref + 0.160	Note 2	V	1, 2
VIL.CA(AC160)	AC Input Logic Low	Note 2	Vref - 0.160	Note 2	Vref - 0.160	Note 2	Vref - 0.160	V	1, 2
VIH.CA(AC135)	AC Input Logic High	Vref + 0.135	Note 2	Vref + 0.135	Note 2	Vref + 0.135	Note 2	V	1, 2
VIL.CA(AC135)	AC Input Logic Low	Note 2	Vref - 0.135	Note 2	Vref - 0.135	Note 2	Vref - 0.135	V	1, 2
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:
1 For input only pins except RESET#. Vref = VrefCA(DC).
2 See JESD79-3E, 9.6 “Overshoot and Undershoot Specifications”, 9.6.1.
3 The AC peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV).
4 For reference: approx. VDD/2 +/- 13.5 mV
5 These levels apply for 1.35 Volt (see Table 23) operation only. If the device is operated at 1.5 V (see Table 24), the respective levels in JESD79-3 (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), etc.) apply. The 1.5 V levels (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), etc.) do not apply when the device is operated in the 1.35 voltage range.

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-1066 (BE)		DDR3-1333 (CG) DDR3-1600 (DI)		DDR3-1866 (EK)		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
VIH.DQ(DC100)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1,5
VIL.DQ(DC100)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1,6
VIH.DQ(AC175)	AC Input Logic High	Vref + 0.175	Note 2	-	-	-	-	V	1, 2, 7
VIL.DQ(AC175)	AC Input Logic Low	Note 2	Vref - 0.175	-	-	-	-	V	1, 2, 8
VIH.DQ(AC150)	AC Input Logic High	Vref + 0.15	Note 2	Vref + 0.15	Note 2	-	-	V	1, 2, 7
VIL.DQ(AC150)	AC Input Logic Low	Note 2	Vref - 0.15	Note 2	Vref - 0.15	-	-	V	1, 2, 8
VIH.DQ(AC135)	AC Input Logic High	-	-	-	-	Vref + 0.135	Note 2	V	1, 2, 7
VIL.DQ(AC135)	AC Input Logic Low	-	-	-	-	Note 2	Vref - 0.135	V	1, 2, 8
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:
1. Vref = VrefDQ(DC).
2. See 9.6 “Overshoot and Undershoot Specifications” on page 126.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.DQ(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.DQ(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.DQ(AC175), VIH.DQ(AC150), and VIH.DQ(AC135); VIH.DQ(AC175) value is used when Vref + 0.175V is referenced, VIH.DQ(AC150) value is used when Vref + 0.150V is referenced, and VIH.DQ(AC135) value is used when Vref + 0.135V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.DQ(AC175), VIL.DQ(AC150), and VIL.DQ(AC135); VIL.DQ(AC175) value is used when Vref - 0.175V is referenced, VIL.DQ(AC150) value is used when Vref -0.150V is referenced, and VIL.DQ(AC135) value is used when Vref - 0.135V is referenced.

Symbol	Parameter	DDR3L-1066 (BE)		DDR3L-1333 (CG) DDR3L-1600 (DI)		Units	Note
		Min.	Max.	Min.	Max.		
VIH.DQ(DC90)	DC Input Logic High	Vref + 0.09	VDD	Vref + 0.09	VDD	V	1
VIL.DQ(DC90)	DC Input Logic Low	VSS	Vref - 0.09	VSS	Vref - 0.09	V	1
VIH.DQ(AC160)	AC Input Logic High	Vref + 0.160	Note 2	-	-	V	1, 2, 5
VIL.DQ(AC160)	AC Input Logic Low	Note 2	Vref - 0.160	-	-	V	1, 2, 5
VIH.DQ(AC135)	AC Input Logic High	Vref + 0.135	Note2	Vref + 0.135	Note2	V	1, 2, 5
VIL.DQ(AC135)	AC Input Logic Low	Note2	Vref - 0.135	Note2	Vref - 0.135	V	1, 2, 5
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:
1 For input only pins except RESET#. Vref = VrefDQ(DC).
2 See JESD79-3E, 9.6 “Overshoot and Undershoot Specifications”, 9.6.2.
3 The AC peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV).
4 For reference: approx. VDD/2 +/- 13.5 mV.
5 These levels apply for 1.35 Volt (see Table 23) operation only. If the device is operated at 1.5 V (see Table 24), the respective levels in JESD79-3 (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), etc.) apply. The 1.5 V levels (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), etc.) do not apply when the device is operated in the 1.35 voltage range.

Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V [4GB – 1 Rank, 512Mx8 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-12800 (-DI)	Unit
IDD0	Operating One Bank Active-Precharge Current	792	mA
IDD1	Operating One Bank Active-Read-Precharge Current	990	mA
IDD2P0	Precharge Power-Down Current Slow Exit	248	mA
IDD2P1	Precharge Power-Down Current Fast Exit	396	mA
IDD2Q	Precharge Quiet Standby Current	495	mA
IDD2N	Precharge Standby Current	495	mA
IDD3P	Active Power-Down Current	594	mA
IDD3N	Active Standby Current	614	mA
IDD4R	Operating Burst Read Current	1851	mA
IDD4W	Operating Burst Write Current	1911	mA
IDD5B	Burst Refresh Current	2010	mA
IDD6	Self Refresh Current: Normal Temperature Range	248	mA
IDD7	Operating Bank Interleave Read Current	2772	mA

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.35V -0.0675/+0.1V [4GB – 1 Rank, 512Mx8 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-10600 (-CG)	PC3-12800 (-DI)	Unit
IDD0	Operating One Bank Active-Precharge Current	644	743	mA
IDD1	Operating One Bank Active-Read-Precharge Current	842	891	mA
IDD2P0	Precharge Power-Down Current Slow Exit	248	248	mA
IDD2P1	Precharge Power-Down Current Fast Exit	317	366	mA
IDD2Q	Precharge Quiet Standby Current	436	465	mA
IDD2N	Precharge Standby Current	465	465	mA
IDD3P	Active Power-Down Current	495	495	mA
IDD3N	Active Standby Current	564	614	mA
IDD4R	Operating Burst Read Current	1653	1782	mA
IDD4W	Operating Burst Write Current	1535	1881	mA
IDD5B	Burst Refresh Current	1931	2010	mA
IDD6	Self Refresh Current: Normal Temperature Range	248	248	mA
IDD7	Operating Bank Interleave Read Current	2653	2653	mA

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V [8GB – 1 Rank, 1024Mx4 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-12800 (-DI)	Unit
IDD0	Operating One Bank Active-Precharge Current	1584	mA
IDD1	Operating One Bank Active-Read-Precharge Current	941	mA
IDD2P0	Precharge Power-Down Current Slow Exit	495	mA
IDD2P1	Precharge Power-Down Current Fast Exit	792	mA
IDD2Q	Precharge Quiet Standby Current	990	mA
IDD2N	Precharge Standby Current	990	mA
IDD3P	Active Power-Down Current	1188	mA
IDD3N	Active Standby Current	1228	mA
IDD4R	Operating Burst Read Current	3465	mA
IDD4W	Operating Burst Write Current	3069	mA
IDD5B	Burst Refresh Current	4019	mA
IDD6	Self Refresh Current: Normal Temperature Range	495	mA
IDD7	Operating Bank Interleave Read Current	4950	mA

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.35V -0.0675/+0.1V [8GB – 1 Rank, 1024Mx4 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-10600 (-CG)	PC3-12800 (-DI)	Unit
IDD0	Operating One Bank Active-Precharge Current	1287	1386	mA
IDD1	Operating One Bank Active-Read-Precharge Current	743	792	mA
IDD2P0	Precharge Power-Down Current Slow Exit	495	495	mA
IDD2P1	Precharge Power-Down Current Fast Exit	634	733	mA
IDD2Q	Precharge Quiet Standby Current	871	931	mA
IDD2N	Precharge Standby Current	931	931	mA
IDD3P	Active Power-Down Current	990	990	mA
IDD3N	Active Standby Current	1129	1228	mA
IDD4R	Operating Burst Read Current	3069	3267	mA
IDD4W	Operating Burst Write Current	2673	3069	mA
IDD5B	Burst Refresh Current	3861	4019	mA
IDD6	Self Refresh Current: Normal Temperature Range	495	495	mA
IDD7	Operating Bank Interleave Read Current	4950	4950	mA

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V [8GB – 2 Rank, 512Mx8 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-12800 (-DI)	Unit
IDD0	Operating One Bank Active-Precharge Current	1287	mA
IDD1	Operating One Bank Active-Read-Precharge Current	1485	mA
IDD2P0	Precharge Power-Down Current Slow Exit	495	mA
IDD2P1	Precharge Power-Down Current Fast Exit	792	mA
IDD2Q	Precharge Quiet Standby Current	990	mA
IDD2N	Precharge Standby Current	990	mA
IDD3P	Active Power-Down Current	1188	mA
IDD3N	Active Standby Current	1109	mA
IDD4R	Operating Burst Read Current	2346	mA
IDD4W	Operating Burst Write Current	2406	mA
IDD5B	Burst Refresh Current	2505	mA
IDD6	Self Refresh Current: Normal Temperature Range	495	mA
IDD7	Operating Bank Interleave Read Current	3267	mA

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.35V -0.0675/+0.1V [8GB – 2 Rank, 512Mx8 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-10600 (-CG)	PC3-12800 (-DI)	Unit
IDD0	Operating One Bank Active-Precharge Current	1109	1208	mA
IDD1	Operating One Bank Active-Read-Precharge Current	1307	1356	mA
IDD2P0	Precharge Power-Down Current Slow Exit	495	495	mA
IDD2P1	Precharge Power-Down Current Fast Exit	634	733	mA
IDD2Q	Precharge Quiet Standby Current	871	931	mA
IDD2N	Precharge Standby Current	931	931	mA
IDD3P	Active Power-Down Current	990	990	mA
IDD3N	Active Standby Current	1030	1079	mA
IDD4R	Operating Burst Read Current	2119	2247	mA
IDD4W	Operating Burst Write Current	2000	2346	mA
IDD5B	Burst Refresh Current	2396	2475	mA
IDD6	Self Refresh Current: Normal Temperature Range	495	495	mA
IDD7	Operating Bank Interleave Read Current	3119	3119	mA

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V [16GB – 2 Rank, 1024Mx4 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-12800 (-DI)	PC3-14900 (-EK)	Unit
IDD0	Operating One Bank Active-Precharge Current	2574		mA
IDD1	Operating One Bank Active-Read-Precharge Current	2871		mA
IDD2P0	Precharge Power-Down Current Slow Exit	990		mA
IDD2P1	Precharge Power-Down Current Fast Exit	1584		mA
IDD2Q	Precharge Quiet Standby Current	1980		mA
IDD2N	Precharge Standby Current	1980		mA
IDD3P	Active Power-Down Current	2376		mA
IDD3N	Active Standby Current	2218		mA
IDD4R	Operating Burst Read Current	4455		mA
IDD4W	Operating Burst Write Current	4059		mA
IDD5B	Burst Refresh Current	5009		mA
IDD6	Self Refresh Current: Normal Temperature Range	990		mA
IDD7	Operating Bank Interleave Read Current	5940		mA

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.35V -0.0675/+0.1V [16GB – 2 Rank, 1024Mx4 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-10600 (-CG)	PC3-12800 (-DI)	Unit
IDD0	Operating One Bank Active-Precharge Current	2218	2317	mA
IDD1	Operating One Bank Active-Read-Precharge Current	2416	2515	mA
IDD2P0	Precharge Power-Down Current Slow Exit	990	990	mA
IDD2P1	Precharge Power-Down Current Fast Exit	1267	1465	mA
IDD2Q	Precharge Quiet Standby Current	1742	1861	mA
IDD2N	Precharge Standby Current	1861	1861	mA
IDD3P	Active Power-Down Current	1980	1980	mA
IDD3N	Active Standby Current	2059	2158	mA
IDD4R	Operating Burst Read Current	4000	4198	mA
IDD4W	Operating Burst Write Current	3604	4000	mA
IDD5B	Burst Refresh Current	4792	4950	mA
IDD6	Self Refresh Current: Normal Temperature Range	990	990	mA
IDD7	Operating Bank Interleave Read Current	5881	5881	mA

Standard Speed Bins

DDR3-1066MHz

Speed Bin			DDR3-1066		Unit
CL-nRCD-nRP			7-7-7 (-BE)		
Parameter		Symbol	Min	Max	
Internal read command to first data		tAA	13.125	20.000	ns
ACT to internal read or write delay time		tRCD	13.125	-	ns
PRE command period		tRP	13.125	-	ns
ACT to ACT or REF command period		tRC	50.625	-	ns
ACT to PRE command period		tRAS	37.500	9*tREFI	ns
CL=5	CWL=5	tCK(AVG)	3.000	3.300	ns
	CWL=6	tCK(AVG)	Reserved		ns
CL=6	CWL=5	tCK(AVG)	2.500	3.300	ns
	CWL=6	tCK(AVG)	Reserved		ns
CL=7	CWL=5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
CL=8	CWL=5	tCK(AVG)	Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
Supported CL Settings			5,6,7,8		nCK
Supported CWL Settings			5,6		nCK

DDR3-1333MHz

Speed Bin			DDR3-1333		Unit
CL-nRCD-nRP			9-9-9 (-CG)		
Parameter		Symbol	Min	Max	
Internal read command to first data		tAA	13. 5 (13.125)[5,11]	20.000	ns
ACT to internal read or write delay time		tRCD	13. 5 (13.125)[5,11]	-	ns
PRE command period		tRP	13. 5 (13.125)[5,11]	-	ns
ACT to ACT or REF command period		tRC	49.5 (49.125)[5,11]	-	ns
ACT to PRE command period		tRAS	36.000	9*tREFI	ns
CL=5	CWL=5	tCK(AVG)	3.0	3.3	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=6	CWL=5	tCK(AVG)	2.500	3.300	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=7	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	1.875*	<2.5*	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=8	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=9	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	1.500	<1.875	ns
CL=10	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	1.500*	<1.875*	ns
Supported CL Settings			5,6,8,(7),9,(10)		nCK
Supported CWL Settings			5,6,7		nCK

DDR3-1600MHz

Speed Bin			DDR3-1600		Unit
CL-nRCD-nRP			11-11-11 (-DI)		
Parameter		Symbol	Min	Max	
Internal read command to first data		tAA	13.75 (13.125)[5,11]	20.000	ns
ACT to internal read or write delay time		tRCD	13.75 (13.125)[5,11]	-	ns
PRE command period		tRP	13.75 (13.125)[5,11]	-	ns
ACT to ACT or REF command period		tRC	48.75 (48.125)[5,11]	-	ns
ACT to PRE command period		tRAS	35.000	9*tREFI	ns
CL=5	CWL=5	tCK(AVG)	3.000	3.300	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=6	CWL=5	tCK(AVG)	2.500	3.300	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=7	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	1.875*	<2.5*	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=8	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
CL=9	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	1.500	<1.875	ns
CL=10	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	1.500*	<1.875*	ns
CL=11	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	Reserved	Reserved	ns
	CWL=8	tCK(AVG)	1.25*	<1.5*	ns
Supported CL Settings			5,6,(7),8,(9),10,11		nCK
Supported CWL Settings			5,6,7,8		nCK
*: Optional					

DDR3-1866MHz

Speed Bin			DDR3-1866		Unit
CL-nRCD-nRP			13-13-13 (-EK)		
Parameter		Symbol	Min	Max	
Internal read command to first data		tAA	13.91 (13.125)	20.000	ns
ACT to internal read or write delay time		tRCD	13.91 (13.125)	-	ns
PRE command period		tRP	13.91 (13.125)	-	ns
ACT to ACT or REF command period		tRC	47.91 (47.125)	-	ns
ACT to PRE command period		tRAS	34.000	9*tREFI	ns
CL=5	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6, 7, 8, 9	tCK(AVG)	Reserved	Reserved	ns
CL=6	CWL=5	tCK(AVG)	2.500	3.300	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7, 8, 9	tCK(AVG)	Reserved	Reserved	ns
CL=7	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7, 8, 9	tCK(AVG)	Reserved	Reserved	ns
CL=8	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	1.875	<2.5	ns
	CWL=7, 8, 9	tCK(AVG)	Reserved	Reserved	ns
CL=9	CWL=5	tCK(AVG)	Reserved	Reserved	ns
	CWL=6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7, 8, 9	tCK(AVG)	Reserved	Reserved	ns
CL=10	CWL=5, 6	tCK(AVG)	Reserved	Reserved	ns
	CWL=7	tCK(AVG)	1.500	<1.875	ns
	CWL=8	tCK(AVG)	Reserved	Reserved	ns
CL=11	CWL=5, 6, 7	tCK(AVG)	Reserved	Reserved	ns
	CWL=8	tCK(AVG)	Reserved	Reserved	ns
	CWL=9	tCK(AVG)	Reserved	Reserved	ns
CL=12	CWL=5, 6, 7, 8	tCK(AVG)	Reserved	Reserved	ns
	CWL=9	tCK(AVG)	Reserved	Reserved	ns
CL=13	CWL=5, 6, 7, 8	tCK(AVG)	Reserved	Reserved	ns
	CWL=9	tCK(AVG)	1.07	<1.25*	ns
Supported CL Settings			6,(7), 8,(9), 10, (11),13		nCK
Supported CWL Settings			5,6,7,8, 9		nCK
*: Optional					

AC Timing Specifications for DDR3 SDRAM Devices Used on Module (1066MHz)

Parameter	Symbol	DDR3-1066		Units	Notes
		Min.	Max.		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	ns	
Average Clock Period	tCK(avg)	Refer to "Standard Speed Bins)		ps	
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max		ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)	
Absolute clock LOW pulse width	tCL(abs)	0.43	-	tCK(avg)	
Clock Period Jitter	JIT(per)	-90	90	ps	
Clock Period Jitter during DLL locking period	JIT(per, lck)	-80	80	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	180	180	ps	
Cycle to Cycle Period Jitter during DLL locking period	JIT(cc, lck)	160	160	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-132	132	ps	
Cumulative error across 3 cycles	tERR(3per)	-157	157	ps	
Cumulative error across 4 cycles	tERR(4per)	-175	175	ps	
Cumulative error across 5 cycles	tERR(5per)	-188	188	ps	
Cumulative error across 6 cycles	tERR(6per)	-200	200	ps	
Cumulative error across 7 cycles	tERR(7per)	-209	209	ps	
Cumulative error across 8 cycles	tERR(8per)	-217	217	ps	
Cumulative error across 9 cycles	tERR(9per)	-224	224	ps	
Cumulative error across 10 cycles	tERR(10per)	-231	231	ps	
Cumulative error across 11 cycles	tERR(11per)	-237	237	ps	
Cumulative error across 12 cycles	tERR(12per)	-242	242	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		ps	
Data Timing					
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	150	ps	
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)	
DQ low-impedance time from CK, CK#	tLZ(DQ)	-600	300	ps	
DQ high impedance time from CK, CK#	tHZ(DQ)	-	300	ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC175	25		ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	75		ps	
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100	100		ps	
DQ and DM Input pulse width for each input	tDIPW	490		ps	
Data Strobe Timing					
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	tCK(avg)	
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	tCK(avg)	
DQS, DQS# differential output high time	tQSH	0.38	-	tCK(avg)	
DQS, DQS# differential output low time	tQSL	0.38	-	tCK(avg)	
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-300	300	tCK(avg)	
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-600	300	tCK(avg)	
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	300	tCK(avg)	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)	
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)	
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	tCK(avg)	
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	tCK(avg)	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	tCK(avg)	
Command and Address Timing					

DLL locking time	tDLLK	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -			
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:			
WRITE recovery time	tWR	15	-	ns	
Mode Register Set command cycle time	tMRD	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:			
ACT to internal read or write delay time	tRCD				
PRE command period	tRP				
ACT to ACT or REF command period	tRC				
CAS# to CAS# command delay	tCCD	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))		nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins			
ACTIVE to ACTIVE command period for 1KB page size	tRRD	tRRDmin : max(4nCK, 7.5ns) tRRDmax : -			
ACTIVE to ACTIVE command period for 2KB page size	tRRD	tRRDmin : max(4nCK,10ns) tRRDmax : -		-	
Four activate window for 1KB page size	tFAW	37.5	-	ns	
Four activate window for 2KB page size	tFAW	50	-	ns	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	125	-	ps	
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	200	-	ps	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	125+150	-	ps	
Control and Address Input pulse width for each input	tIPW	780	-	ps	
Calibration Timing					
Power-up and RESET calibration time	tZQinit	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	nCK	
Reset Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -			
Self Refresh Timings					
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -			
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -		nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -			
Power Down Timings					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 7.5ns) tXPmax.: -			
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -			
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK 5.625ns) tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 1 tCPDEDmin.: -		nCK	
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI			
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -		nCK	

Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -		nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -		nCK	
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -		nCK	
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -			
ODT Timings					
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -		nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -		nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns	
RTT turn-on	tAON	-300	300	ps	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	
Write Leveling Timings					
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	245	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	245	-	ps	
Write leveling output delay	tWLO	0	9	ns	
Write leveling output error	tWLOE	0	2	ns	

AC Timing Specifications for DDR3 SDRAM Devices Used on Module (1333MHz)

Parameter	Symbol	DDR3-1333		Units	Notes
		Min.	Max.		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	ns	
Average Clock Period	tCK(avg)	Refer to "Standard Speed Bins)		ps	
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max		ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)	
Absolute clock LOW pulse width	tCL(abs)	0.43	-	tCK(avg)	
Clock Period Jitter	JIT(per)	-80	80	ps	
Clock Period Jitter during DLL locking period	JIT(per, lck)	-70	70	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	160	160	ps	
Cycle to Cycle Period Jitter during DLL locking period	JIT(cc, lck)	140	140	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-118	118	ps	
Cumulative error across 3 cycles	tERR(3per)	-140	140	ps	
Cumulative error across 4 cycles	tERR(4per)	-155	155	ps	
Cumulative error across 5 cycles	tERR(5per)	-168	168	ps	
Cumulative error across 6 cycles	tERR(6per)	-177	177	ps	
Cumulative error across 7 cycles	tERR(7per)	-186	186	ps	
Cumulative error across 8 cycles	tERR(8per)	-193	193	ps	
Cumulative error across 9 cycles	tERR(9per)	-200	200	ps	
Cumulative error across 10 cycles	tERR(10per)	-205	205	ps	
Cumulative error across 11 cycles	tERR(11per)	-210	210	ps	
Cumulative error across 12 cycles	tERR(12per)	-215	215	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		ps	
Data Timing					
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	125	ps	
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)	
DQ low-impedance time from CK, CK#	tLZ(DQ)	-500	250	ps	
DQ high impedance time from CK, CK#	tHZ(DQ)	-	250	ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC175	-		ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	30		ps	
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100	65		ps	
DQ and DM Input pulse width for each input	tDIPW	400	-	ps	
Data Strobe Timing					
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	tCK(avg)	
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	tCK(avg)	
DQS, DQS# differential output high time	tQSH	0.4	-	tCK(avg)	
DQS, DQS# differential output low time	tQSL	0.4	-	tCK(avg)	
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-255	255	tCK(avg)	
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-500	250	tCK(avg)	
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	250	tCK(avg)	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)	
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)	
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	tCK(avg)	
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	tCK(avg)	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	tCK(avg)	
Command and Address Timing					

DLL locking time	tDLLK	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -			
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:			
WRITE recovery time	tWR	15	-	ns	
Mode Register Set command cycle time	tMRD	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:			
ACT to internal read or write delay time	tRCD				
PRE command period	tRP				
ACT to ACT or REF command period	tRC				
CAS# to CAS# command delay	tCCD	4		nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))		nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins			
ACTIVE to ACTIVE command period for 1KB page size	tRRD	tRRDmin.: max(4nCK, 6ns) tRRDmax.:			
ACTIVE to ACTIVE command period for 2KB page size	tRRD	tRRDmin.: max(4nCK, 7.5ns) tRRDmax.:			
Four activate window for 1KB page size	tFAW	30	0	ns	
Four activate window for 2KB page size	tFAW	45	0	ns	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65	-	ps	
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	ps	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	65+125	-	ps	
Control and Address Input pulse width for each input	tIPW	620	-	ps	
Calibration Timing					
Power-up and RESET calibration time	tZQinit	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	nCK	
Reset Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -			
Self Refresh Timings					
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -			
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -		nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -			
Power Down Timings					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns) tXPmax.: -			
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -			
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK ,5.625ns) tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 1 tCPDEDmin.: -		nCK	
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI			
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -		nCK	

Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -		nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -		nCK	
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -		nCK	
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -			
ODT Timings					
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -		nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -		nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns	
RTT turn-on	tAON	-250	250	ps	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	
Write Leveling Timings					
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	195	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	195	-	ps	
Write leveling output delay	tWLO	0	9	ns	
Write leveling output error	tWLOE	0	2	ns	

AC Timing Specifications for DDR3 SDRAM Devices Used on Module (1600MHz)

Parameter	Symbol	DDR3-1600		Units	Notes
		Min.	Max.		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	ns	
Average Clock Period	tCK(avg)	Refer to "Standard Speed Bins)		ps	
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max		ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)	
Absolute clock LOW pulse width	tCL(abs)	0.43	-	tCK(avg)	
Clock Period Jitter	JIT(per)	-70	70	ps	
Clock Period Jitter during DLL locking period	JIT(per, lck)	-60	60	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140	140	ps	
Cycle to Cycle Period Jitter during DLL locking period	JIT(cc, lck)	120	120	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-103	103	ps	
Cumulative error across 3 cycles	tERR(3per)	-122	122	ps	
Cumulative error across 4 cycles	tERR(4per)	-136	136	ps	
Cumulative error across 5 cycles	tERR(5per)	-147	147	ps	
Cumulative error across 6 cycles	tERR(6per)	-155	155	ps	
Cumulative error across 7 cycles	tERR(7per)	-163	163	ps	
Cumulative error across 8 cycles	tERR(8per)	-169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	-175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	-180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	-184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	-188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		ps	
Data Timing					
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	100	ps	
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)	
DQ low-impedance time from CK, CK#	tLZ(DQ)	-450	225	ps	
DQ high impedance time from CK, CK#	tHZ(DQ)	-	225	ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC175	-		ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	10		ps	
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100	45		ps	
DQ and DM Input pulse width for each input	tDIPW	360	-	ps	
Data Strobe Timing					
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	tCK(avg)	
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	tCK(avg)	
DQS, DQS# differential output high time	tQSH	0.4	-	tCK(avg)	
DQS, DQS# differential output low time	tQSL	0.4	-	tCK(avg)	
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-255	255	tCK(avg)	
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-450	225	tCK(avg)	
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	225	tCK(avg)	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)	
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)	
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	tCK(avg)	
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	tCK(avg)	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	tCK(avg)	
Command and Address Timing					

DLL locking time	tDLLK	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -			
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:			
WRITE recovery time	tWR	15	-	ns	
Mode Register Set command cycle time	tMRD	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:			
ACT to internal read or write delay time	tRCD				
PRE command period	tRP				
ACT to ACT or REF command period	tRC				
CAS# to CAS# command delay	tCCD	4		nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))		nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins			
ACTIVE to ACTIVE command period for 1KB page size	tRRD	tRRDmin.: max(4nCK, 6ns) tRRDmax.:			
ACTIVE to ACTIVE command period for 2KB page size	tRRD	tRRDmin.: max(4nCK, 7.5ns) tRRDmax.:			
Four activate window for 1KB page size	tFAW	30	-	ns	
Four activate window for 2KB page size	tFAW	40	-	ns	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	45	-	ps	
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	120	-	ps	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	170	-	ps	
Control and Address Input pulse width for each input	tIPW	560	-	ps	
Calibration Timing					
Power-up and RESET calibration time	tZQinit	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	nCK	
Reset Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -			
Self Refresh Timings					
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -			
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -		nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -			
Power Down Timings					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns) tXPmax.: -			
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -			
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK ,5ns) tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 1 tCPDEDmin.: -		nCK	
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI			
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -		nCK	

Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -		nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -		nCK	
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -		nCK	
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -			
ODT Timings					
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -		nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -		nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns	
RTT turn-on	tAON	-225	225	ps	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	
Write Leveling Timings					
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	165	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	165	-	ps	
Write leveling output delay	tWLO	0	7.5	ns	
Write leveling output error	tWLOE	0	2	ns	

AC Timing Specifications for DDR3 SDRAM Devices Used on Module (1866MHz)

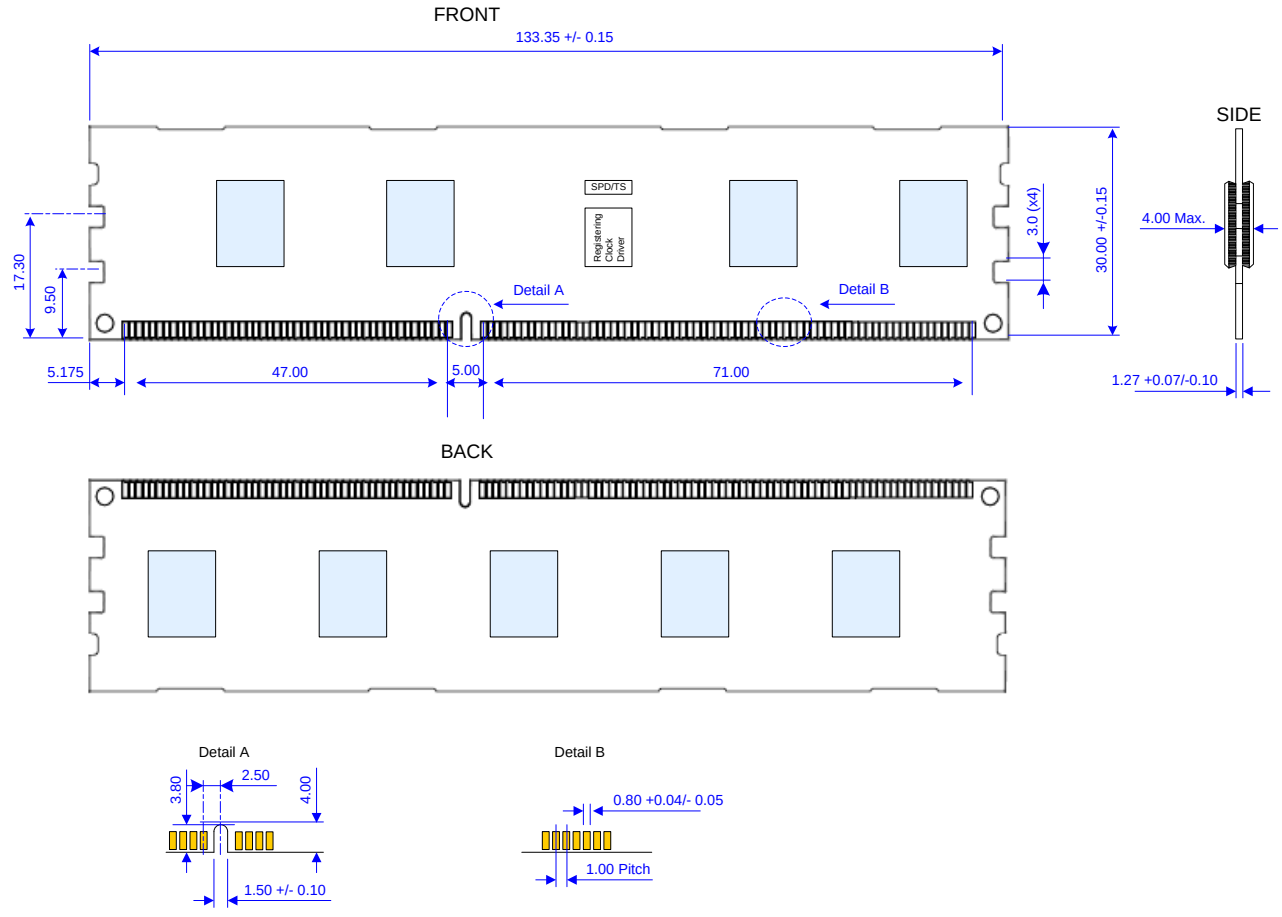
Parameter	Symbol	DDR3-1866		Units	Notes
		Min.	Max.		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	ns	
Average Clock Period	tCK(avg)	Refer to "Standard Speed Bins)		ps	
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max		ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)	
Absolute clock LOW pulse width	tCL(abs)	0.43	-	tCK(avg)	
Clock Period Jitter	JIT(per)	-60	60	ps	
Clock Period Jitter during DLL locking period	JIT(per, lck)	-50	50	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	120	120	ps	
Cycle to Cycle Period Jitter during DLL locking period	JIT(cc, lck)	100	100	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-88	88	ps	
Cumulative error across 3 cycles	tERR(3per)	-105	105	ps	
Cumulative error across 4 cycles	tERR(4per)	-117	117	ps	
Cumulative error across 5 cycles	tERR(5per)	-126	126	ps	
Cumulative error across 6 cycles	tERR(6per)	-133	133	ps	
Cumulative error across 7 cycles	tERR(7per)	-139	139	ps	
Cumulative error across 8 cycles	tERR(8per)	-145	145	ps	
Cumulative error across 9 cycles	tERR(9per)	-150	150	ps	
Cumulative error across 10 cycles	tERR(10per)	-154	154	ps	
Cumulative error across 11 cycles	tERR(11per)	-158	158	ps	
Cumulative error across 12 cycles	tERR(12per)	-161	161	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		ps	
Data Timing					
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	100	ps	
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)	
DQ low-impedance time from CK, CK#	tLZ(DQ)	-390	195	ps	
DQ high impedance time from CK, CK#	tHZ(DQ)	-	195	ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC175	-		ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	-		ps	
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100	-		ps	
DQ and DM Input pulse width for each input	tDIPW	320	-	ps	
Data Strobe Timing					
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	tCK(avg)	
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	tCK(avg)	
DQS, DQS# differential output high time	tQSH	0.4	-	tCK(avg)	
DQS, DQS# differential output low time	tQSL	0.4	-	tCK(avg)	
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-195	195	tCK(avg)	
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-390	195	tCK(avg)	
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	195	tCK(avg)	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)	
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)	
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	tCK(avg)	
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	tCK(avg)	
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	tCK(avg)	
Command and Address Timing					

DLL locking time	tDLLK	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -			
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:			
WRITE recovery time	tWR	15	-	ns	
Mode Register Set command cycle time	tMRD	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:			
ACT to internal read or write delay time	tRCD				
PRE command period	tRP				
ACT to ACT or REF command period	tRC				
CAS# to CAS# command delay	tCCD	4		nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))		nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins			
ACTIVE to ACTIVE command period for 1KB page size	tRRD	tRRDmin.: max(4nCK, 5ns) tRRDmax.:			
ACTIVE to ACTIVE command period for 2KB page size	tRRD	tRRDmin.: max(4nCK, 6ns) tRRDmax.:			
Four activate window for 1KB page size	tFAW	27	-	ns	
Four activate window for 2KB page size	tFAW	35	-	ns	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	-	-	ps	
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	-	-	ps	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	-	-	ps	
Control and Address Input pulse width for each input	tIPW	535	-	ps	
Calibration Timing					
Power-up and RESET calibration time	tZQinit	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	nCK	
Reset Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -			
Self Refresh Timings					
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -			
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -		nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -			
Power Down Timings					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns) tXPmax.: -			
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -			
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK ,5ns) tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 2 tCPDEDmin.: -		nCK	
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI			
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -		nCK	

Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -		nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -		nCK	
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg)) tWRPDENmax.: -		nCK	
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -		nCK	
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -		nCK	
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -			
ODT Timings					
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -		nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -		nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns	
RTT turn-on	tAON	-195	195	ps	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	
Write Leveling Timings					
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	140	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	140	-	ps	
Write leveling output delay	tWLO	0	7.5	ns	
Write leveling output error	tWLOE	0	2	ns	

Package Dimensions

[4GB – 1 Rank, 512Mx8 DDR3 SDRAMs]

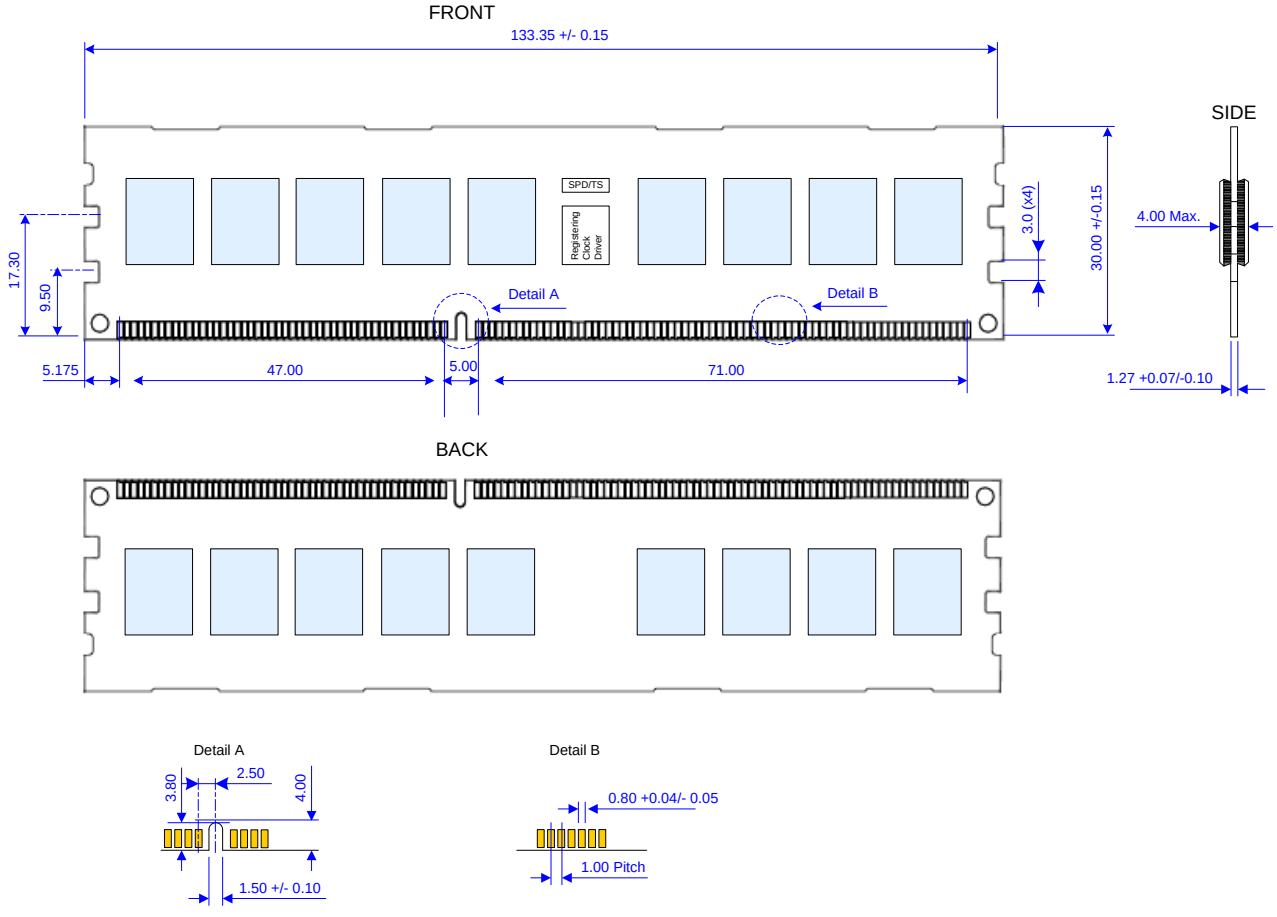


Units: Millimeters

Note: Device position and scale are only for reference.

Package Dimensions

[8GB – 2 Ranks, 512Mx8 DDR3 SDRAMs]

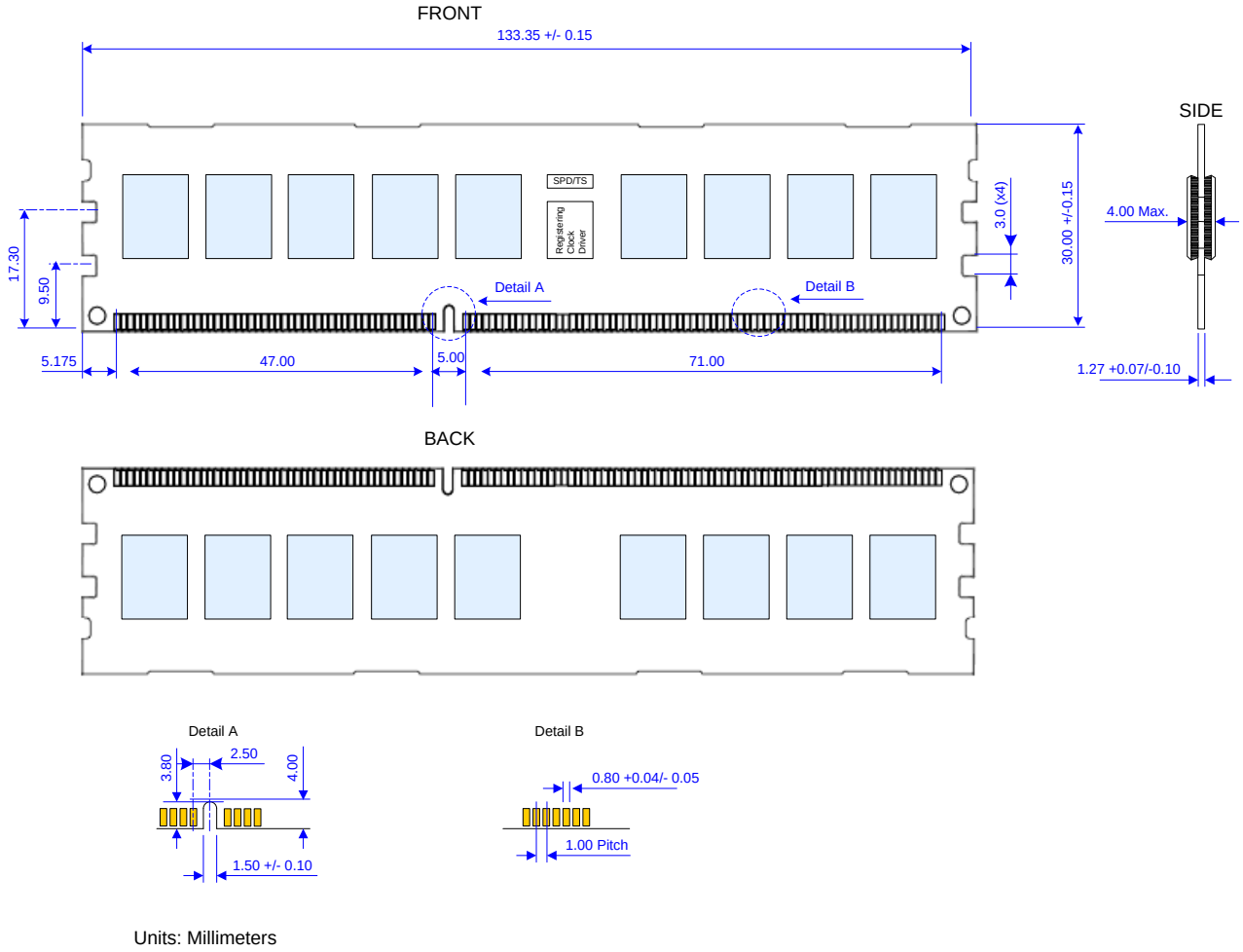


Units: Millimeters

Note: Device position and scale are only for reference.

Package Dimensions

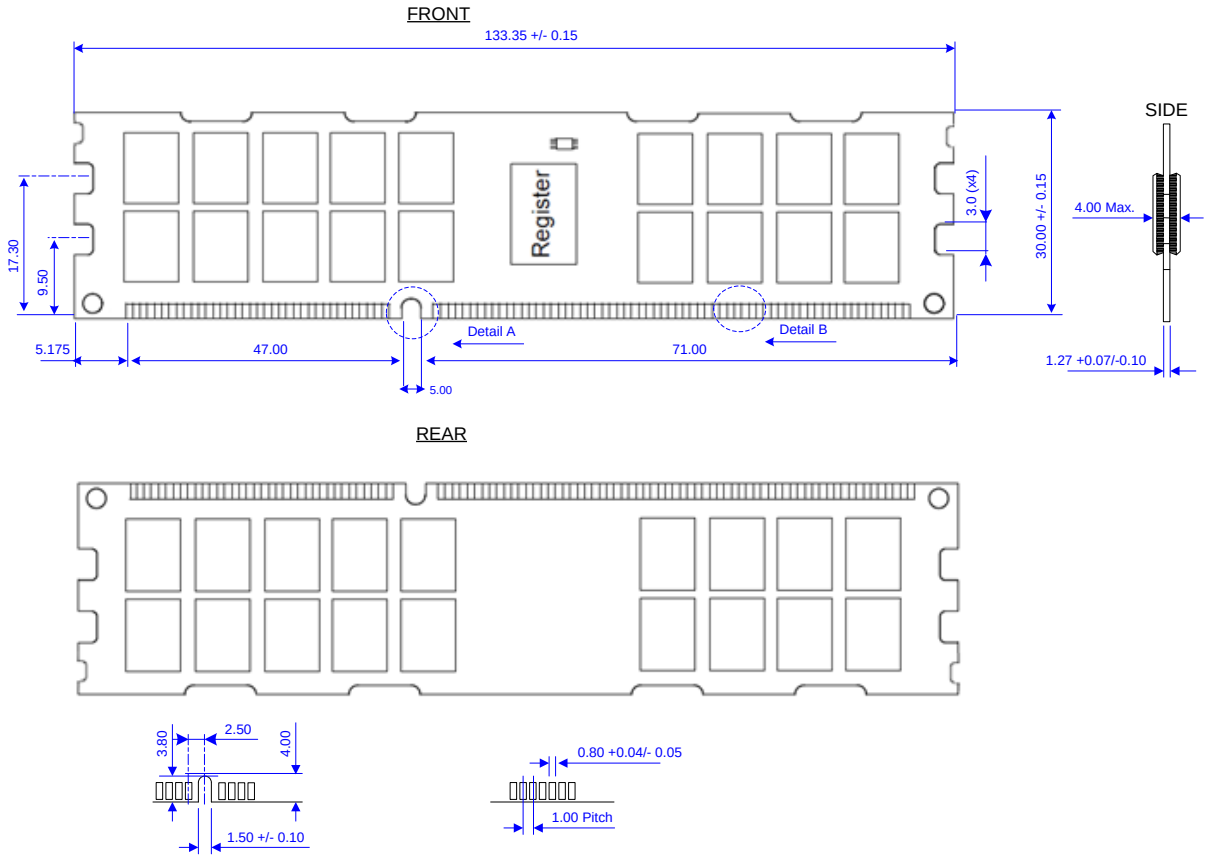
[8GB – 1 Rank, 1024Mx4 DDR3 SDRAMs]



Units: Millimeters

Note: Device position and scale are only for reference.

[16GB – 2 Ranks, 1024Mx4 DDR3 SDRAMs without H/S]



Units: Millimeters

Note: Device position and scale are only for reference.

Revision Log

Rev	Date	Modification
0.1	10/2011	Preliminary Release
1.0	1/2012	Official Release

Nanya Technology Corporation

Hwa Ya Technology Park 669

Fu Hsing 3rd Rd., Kueishan,

Taoyuan, 333, Taiwan, R.O.C.

Tel: +886-3-328-1688

Please visit our home page for more information: www.nanya.com