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MV1444

COMBINED PCM TIMESLOT ZERO TRANSMITTER AND HDB3 ENCODER

The MV1444 combines the Timeslot Zero Transmitter and HDB3 Encoder functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations and forms part of the GPS 2Mbit PCM signalling series of devices. The circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The Timeslot Zero Transmitter half of the circuit is responsible for generating the timeslot zero synchronising word of a 2Mbit PCM link in accordance with CCITT Recommendation G.704. This function is performed by alternately generating sync frames, containing the CCITT Frame Alignment Signal, and non-sync frames containing user data bits.

The data being output from the Timeslot Zero Transmitter is multiplexed together with data for the remaining 31 timeslots by the transmission multiplexer and the PCM data stream thus created is fed in to the HDB3 Encoder.

The HDB3 Encoder half of the circuit is responsible for converting the incoming PCM data stream from the transmission multiplexer from NRZ form in to pseudo-ternary HDB3 transmission code for transmission over a 2Mbit PCM link. This process is carried out in accordance with Annex A to CCITT Recommendation G. 703 and ensures adequate clock recovery at the PCM receiver.

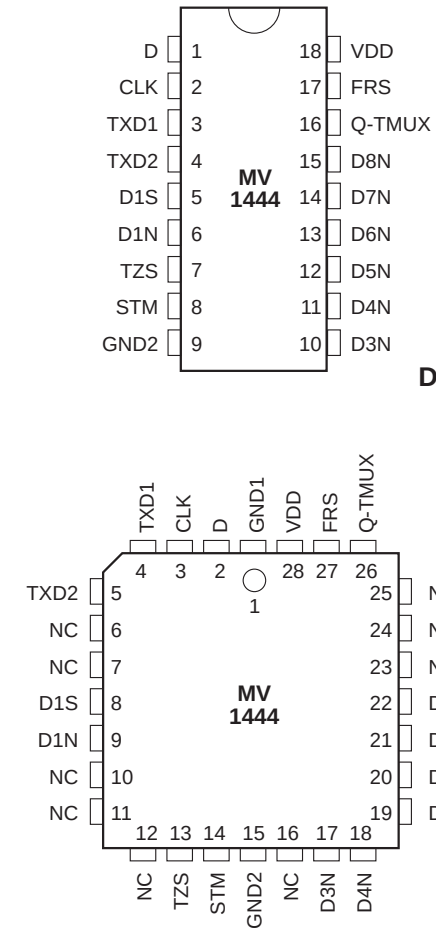


Fig. 1 Pin connections - top view

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- Timeslot Zero Transmitter generates Frame Alignment Signal in accordance with CCITT Recommendation G.704.
- Enables access to 6 User data bits and 2 International data bits of Timeslot Zero.
- On-chip Transmission Multiplexer allows combination of Timeslot Zero data with remaining 31 Timeslots of data.
- HDB3 Encoding carried out in Accordance with Annex A to CCITT Recommendation G.703.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

ORDERING INFORMATION

MV1444/IG/DGAS
MV1444/IG/DPAS
MV1444/IG/HGAS
MV1444/IG/HPAS

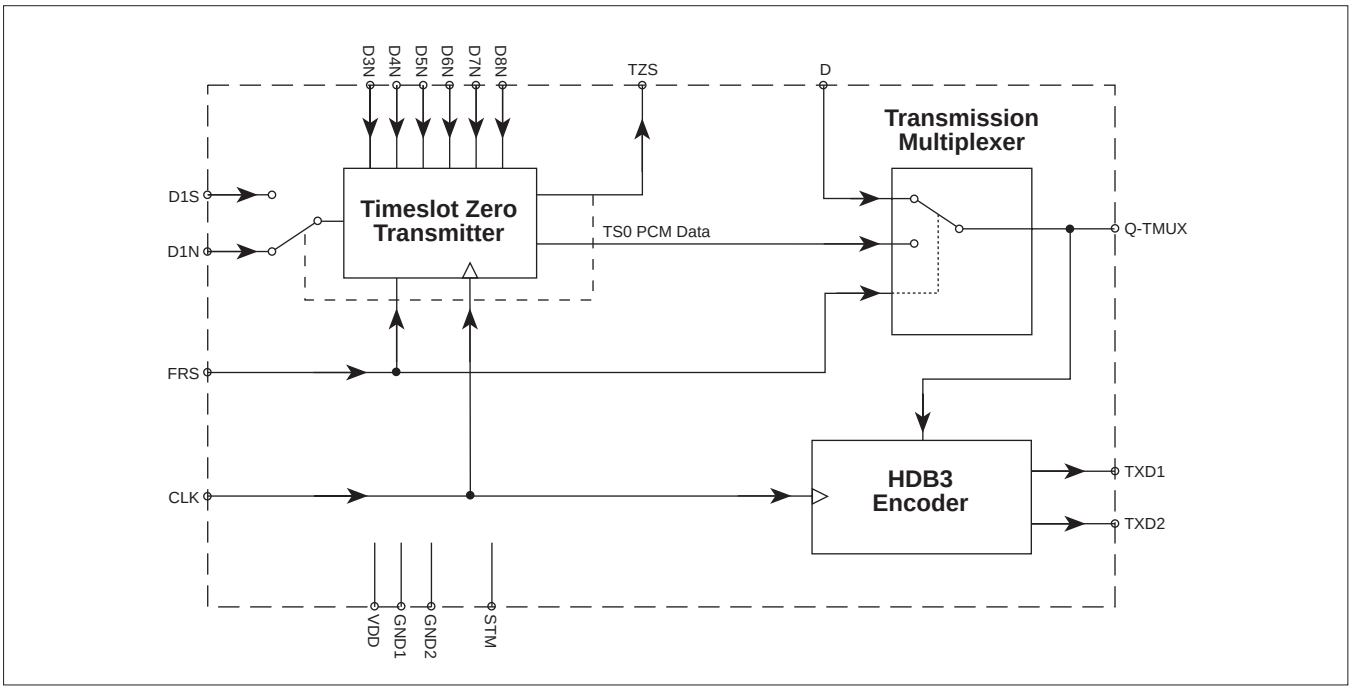


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The MV1444 combines the Timeslot Zero Transmitter, Transmission Multiplexer and HDB3 Encoder functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The block diagram of the MV1444 is shown in Fig. 2, and the function of each block is now described separately.

Timeslot Zero Transmitter

The Timeslot Zero Transmitter circuit generates the timeslot zero synchronising word required by a 2.048Mbit PCM link in accordance with CCITT Recommendation G.704. During alternate frames, denoted sync frames, the CCITT Frame Alignment Signal (FAS - 0011011) is combined with the International / CRC data bit input, D1S, for bit 1 and injected in to the transmission multiplexer for HDB3 Encoding. During the other interleaved frames, denoted non-sync frames, bit 2 of timeslot zero is set to '1' to avoid imitation of the FAS and this is combined with the second International / CRC data bit, D1N, for bit 1 and the user data bits, D3N-D8N, for bits 3 to 8, and again output to the transmission multiplexer.

In order to perform this function the Timeslot Zero Transmitter requires 2 timing inputs in addition to the parallel data bit inputs, pins CLK and FRS. The CLK input is a 2.048MHz clock input whilst FRS is a high going pulse, 8 clock periods long, which is required to mask timeslot zero of each frame. In addition to the PCM data stream output the Timeslot Zero Transmitter produces a timing output, TZS, which changes state one clock period after the end of Timeslot Zero and is high during the transmission of timeslot zero of sync frames. The timing diagram of the entire MV1444 is shown in Fig.3.

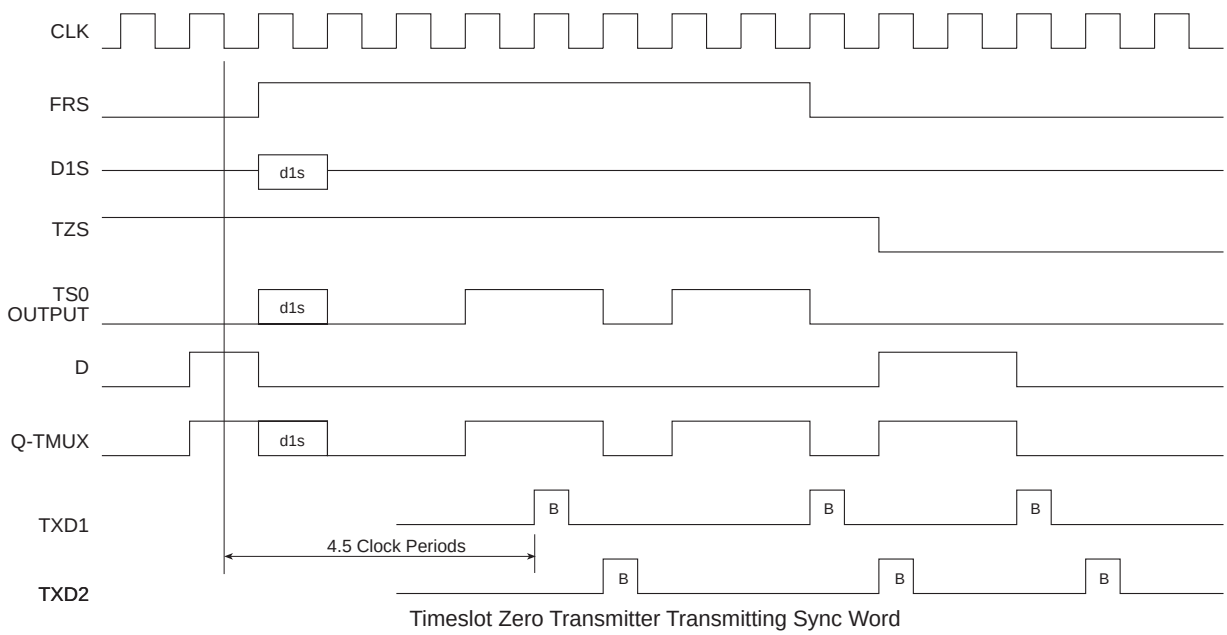
Transmission Multiplexer

The Transmission Multiplexer circuit mutiplexes together the output from the Timeslot Zero Transmitter with the PCM data stream for the remaining 31 timeslots being input on the D pin. This multiplexing is carried out under control of the FRS input such that the output from the Timeslot Zero Transmitter is selected whenever FRS is high. The output from the transmission multiplexer is input to the HDB3 Encoder and is also available as a device output on the Q-TMUX pin.

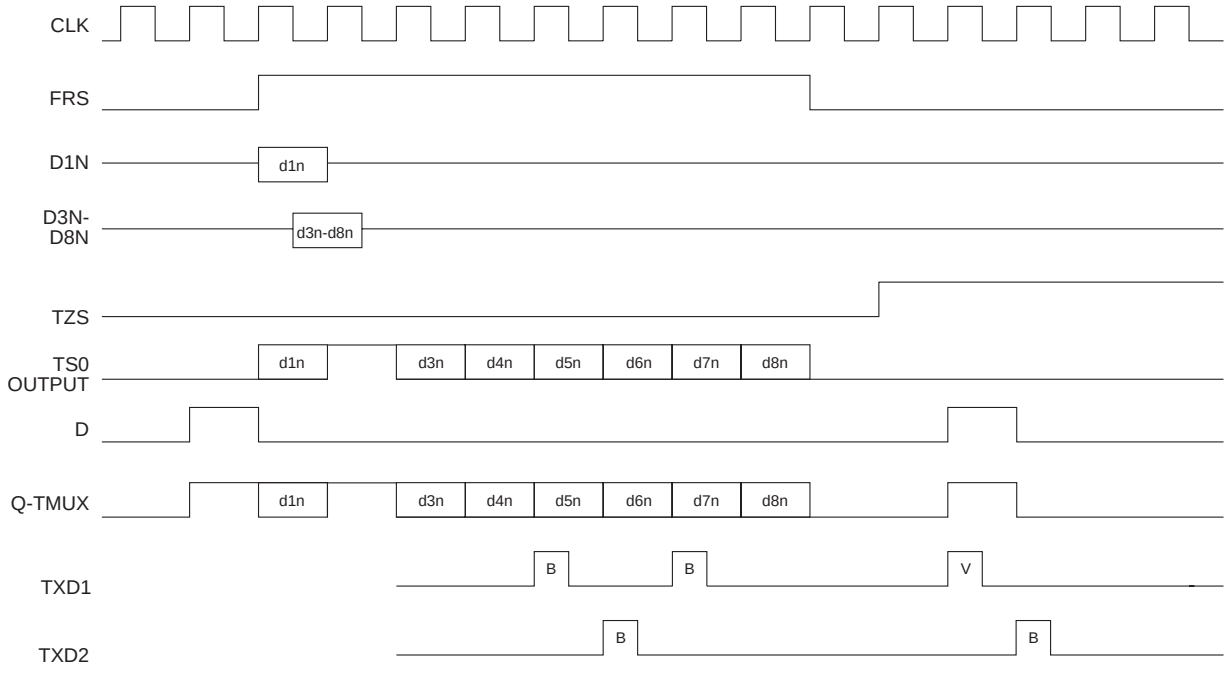
HDB3 Encoder

The HDB3 Encoder is responsible for converting the NRZ data being output by the transmission multiplexer into pseudo-ternary form for transmission over a 2.048Mbit PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A.

High Density Bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zeroes, the last zero is substituted by a mark of the same polarity of the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal. The data to be encoded is the PCM data stream being output by the transmission multiplexer and this is latched into the HDB3 Encoder by the falling edge of CLK. The HDB3 Encoder has two outputs, TXD1 and TXD2, which represent the HDB3 encoded PCM data stream in pseudo-ternary form. If a mark or violation is to be transmitted the output pulses high after the rising edge of clock, with the length of the pulse set by the clock high pulse width.



Timeslot Zero Transmitter Transmitting Sync Word



Timeslot Zero Transmitter Transmitting Non-sync Word

NOTES

1) The encoded HDB3 outputs, TXD1/2 are delayed by 4.5 clock periods with respect to Q-TMUX.
2) B is a mark, V is a HDB3 violation.
3) The TXD outputs are produced under the assumption that d1s=d1n=1, d3n-d8n=0.
4) Both diagrams assume the last mark and last violation occured on TXD2.

Fig. 3 MV1444 Timing diagrams

PIN DESCRIPTIONS

Pin name	Pin no.		Pin description
	DG18	HG28	
GND1	-	1	Digital Ground. OV (Note 1)
D	1	2	2.048Mbit PCM Voice Channel Input to Transmission Multiplexer. Data on this pin is input to the transmission multiplexer during timeslots 1-31 of a CCITT PCM frame for HDB3 encoding. After multiplexing this data is latched in to the HDB3 Encoder by the falling edge of CLK.
CLK	2	3	2.048MHz System Clock Input to Timeslot Zero Transmitter and HDB3 Encoder.
TXD1	3	4	HDB3 Encoded Pseudo-Ternary Output 1 from HDB3 Encoder. The PCM data stream produced by the transmission multiplexer is HDB3 encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK to TXD1.
TXD2	4	5	HDB3 Encoded Pseudo-Ternary Output 2 from HDB3 Encoder. See Pin TXD1 description.
D1S	5	8	International / CRC Data Bit Input to Timeslot ZeroTransmitter for Sync Frames. The data on this pin is output to the transmission multiplexer during bit 1, timeslot zero of sync frames and must be set up prior to the rising edge of FRS during sync frames.
D1N	6	9	International / CRC Data Bit Input to Timeslot Zero Transmitter for Non-Sync Frames. The data on this pin is output to the transmission multiplexer during bit 1, timeslot zero of non-sync frames and must be set up prior to the rising edge of FRS during non-sync frames.
TZS	7	13	Timeslot Zero Sync Frame Output from Timeslot Zero Transmitter. This 4KHz output changes state at the end of bit 1, timeslot 1 (Note 2) of every frame and is high during timeslot zero of sync frames.
STM	8	14	Scan Path Test Global Mode Pin. A logic high on this pin configures the MV1444 in scan test mode. For normal operation this pin should be tied low.
GND2	9	15	Digital Ground. OV (Note 1)

PIN DESCRIPTIONS (continued)

Pin name	Pin no.		Pin description
	DG18	HG28	
D3N D4N D5N D6N D7N D8N	10 11 12 13 14 15	17 18 19 20 21 22	User Data Bit Inputs to Timeslot Zero Transmitter. These 6 parallel data inputs are inserted by the Timeslot Zero Transmitter into bits 8-3 of timeslot zero during non-sync words. These inputs must be set up prior to the rising edge of CLK at the end of bit 1, timeslot zero of non-sync frames.
Q-TMUX	16	26	PCM Data Stream Output from Transmission Multiplexer. During Timeslot Zero this output represents the data stream being produced by the Timeslot Zero Transmitter. During any other timeslot it represents the data being input on the D pin.
FRS	17	27	Timeslot Zero Frame Sync Input of Timeslot ZeroTransmitter and Transmission Multiplexer. This input is required to be an 8 bit long, high going pulse masking timeslot zero. This input is latched by the falling edge of CLK although the first bit of timeslot zero is output asynchronously immediately after the rising edge of FRS. This input is also used as the select input to the transmission multiplexer,which selects the output of the Timeslot zero transmitter as long as FRS is high, the D input whenever FRS is low.
V_{DD}	18	28	Digital Supply Voltage. 5 Volt ±10%

NOTES

1. In order to aid adequate supply decoupling, both digital ground pins of the HG28 and HP28 variants should be connected to 0V.
2. The bits of a timeslot are numbered from 1 to 8 whereas the timeslots of a frame are numbered from 0 to 31 and the frames of a CCITT multiframe are numbered from 0 to 15.
3. All inputs have 100K on-chip pull down resistors.

ELECTRICAL CHARACTERISTICS TEST CONDITIONS:

Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT}	2.4			V	Isource=2mA
	V_{OHC}	V_{DD}-1.0			V	Isource=lmA
Input Leakage Current	I_{IL}	-10		200	uA	Vin=V_{DD} or V_{SS}
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	t_{CP}	400			ns	See Fig. 4
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 4
Clock High/Low Time	t_{CH}/t_{CL}	150			ns	See Fig. 4
FRS Rising Hold Time	t_{FRH}	100			ns	See Fig. 5
FRS Rising Setup Time	t_{FRS}	100			ns	See Fig. 5
FRS Falling Hold Time	t_{FFH}	100			ns	See Fig. 5
FRS Falling Setup Time	t_{FFS}	100			ns	See Fig. 5
International Data Bit Setup Time	t_{IDS}	50			ns	See Fig. 5
International Data Bit Hold Time	t_{IDH}	70			ns	See Fig. 5
User Data Setup Time	t_{UDS}	50			ns	See Fig. 5
User Data Hold Time	t_{UDH}	50			ns	See Fig. 5
TZS Propagation Delay	t_{SFPD}			60	ns	See Fig. 5, Note 1.
PCM Data Setup Time	t_{PDS}	50			ns	See Fig. 5
PCM Data Hold Time	t_{PDH}	50			ns	See Fig. 5
Q-TMUX Propagation Delay from FRS (for bit 1, TS0)	t_{QPDF}			70	ns	See Fig. 5, Note 1.
Q-TMUX Propagation Delay from CLK (for bits 2-8, TS0)	t_{QPDC}			75	ns	See Fig. 5, Note 1.
Q-TMUX Propagation Delay from D (for Timeslots 1-31)	t_{QPDD}			60	ns	See Fig. 5, Note 1.
TXD1/2 Output Propagation Delay	t_{TPDR}/ t_{TPDF}			60	ns	See Fig. 5, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.

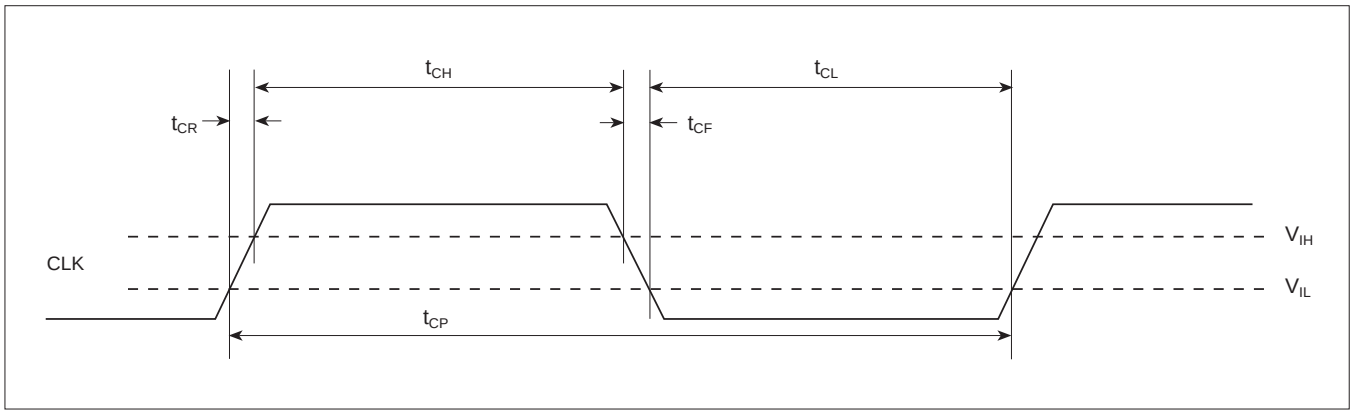


Fig. 4 Clock timing parameters

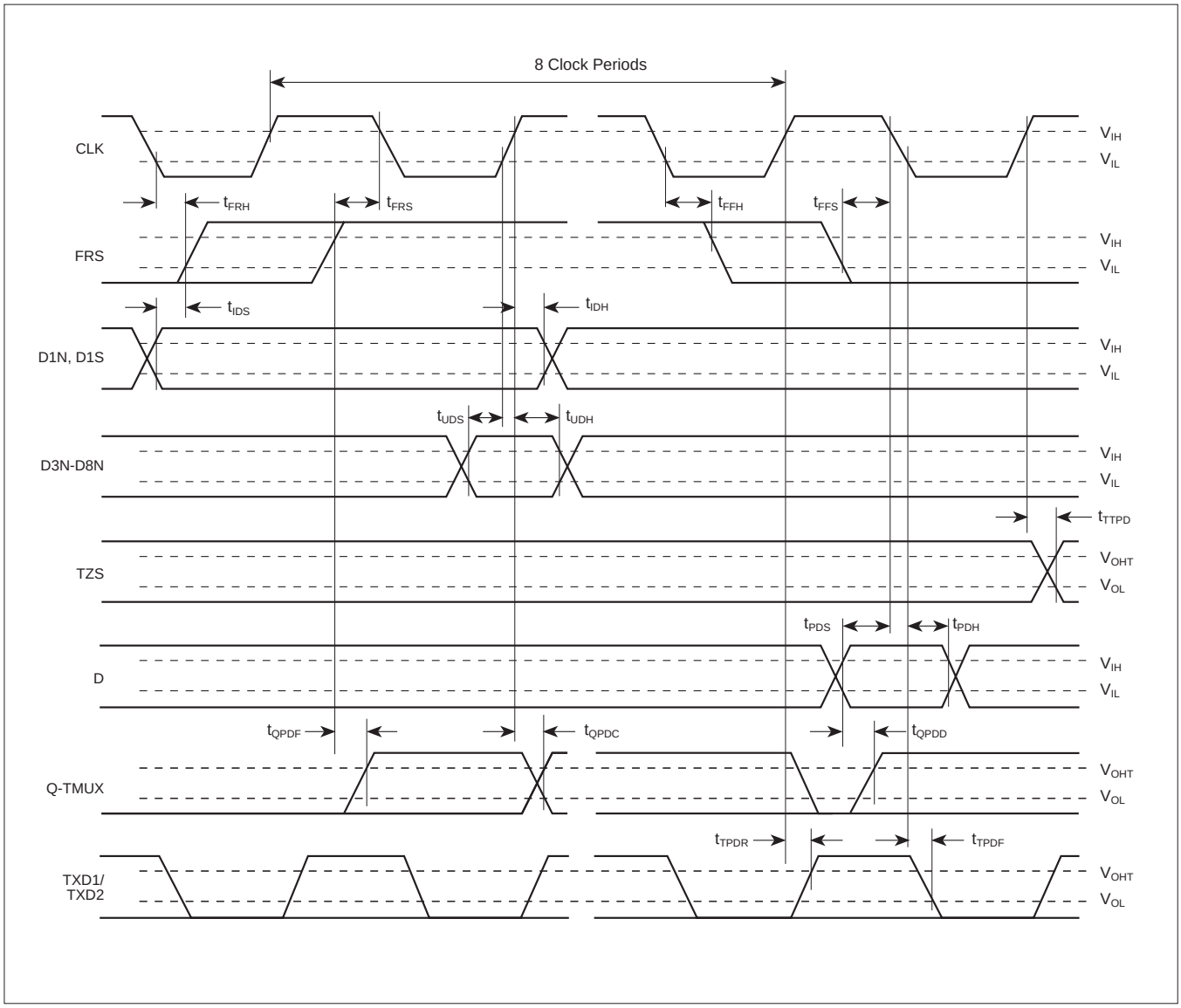


Fig. 5 MV1444 Timing parameters

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