1x512Kx32bit DRAM Card
2x512Kx32bit DRAM Card

MF12M1-L57ATXX
MF14M1-L57ATXX

Connector Type

Two-piece 88-pin

DESCRIPTION

These DRAM CARDs are developed based on JEIDA DRAM CARD GUIDELINE Ver 2.0.
These cards are made using industry standard 512K × 8 Dynamic RAM and interface IC's in TSOP.

FEATURES

- Operating Voltage : V_{CC} = 5 V ± 5 %
- All inputs expect $\overline{RAS}$ inputs are buffered.
- Standard card size : 54 mm (W) × 85.6 mm (L) × 3.3mm (T)
- 88pin 2 piece connector type.
- $\overline{RAS}$ only refresh mode, $\overline{CAS}$ before $\overline{RAS}$ refresh mode and Page mode functions are available.
- Extend refresh mode is available. (128 ms/ 1024 cycle)

APPLICATIONS

Main/expansion memory unit for Personal Computer. Laser-Printer, FAX etc.

PRODUCT LIST

Product No.	Type name \ Item	Memory capacity	Data bus width (bits)	Access time (t_{RAC}) (ns)	Connector type	Number of pins	Outline drawing
No. 1	MF12M1-L57ATXX	2 MB	32	70	Two-Piece	88	88P-001
No. 2	MF14M1-L57ATXX	4 MB		70			

MITSUBISHI ELECTRIC

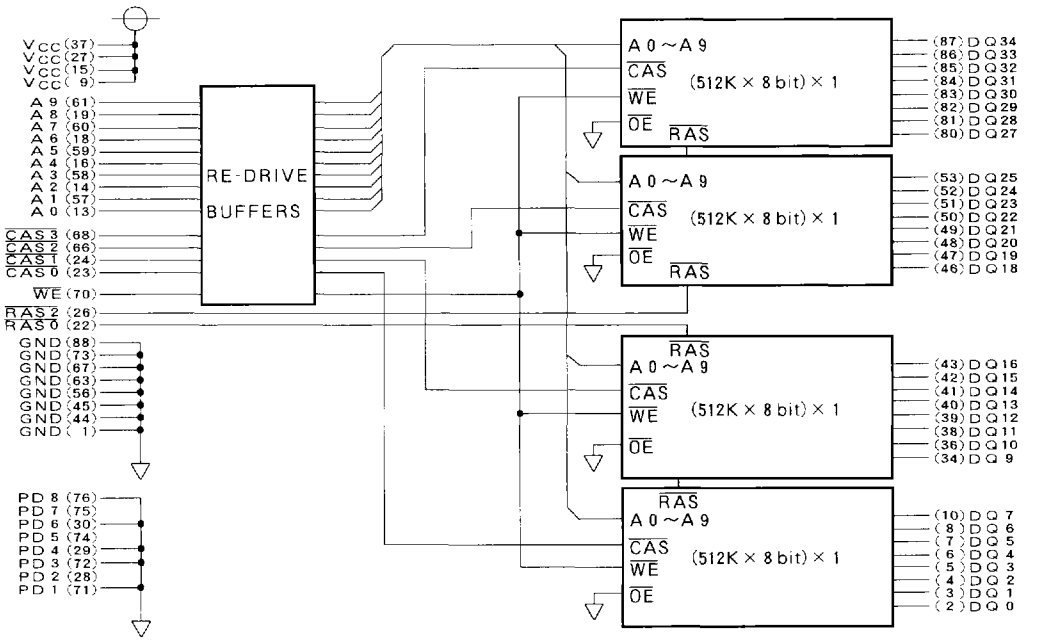
PIN ASSIGNMENT (No.1)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ 0	Data I/O	46	DQ18	Data I/O
3	DQ 1		47	DQ19	
4	DQ 2		48	DQ20	
5	DQ 3		49	DQ21	
6	DQ 4		50	DQ22	
7	DQ 5		51	DQ23	
8	DQ 6		52	DQ24	
9	N.C.	Power supply voltage	53	DQ25	
10	DQ 7	Data I/O	54	N.C.	No connection
11	N.C.	No connection	55	N.C.	
12	N.C.		56	GND	Ground
13	A 0	Address input	57	A 1	Address input
14	A 2		58	A 3	
15	Vcc	Power supply voltage	59	A 5	
16	A 4	Address input	60	A 7	
17	N.C.	No connection	61	A 9	
18	A 6	Address input	62	N.C.	No connection
19	A 8		63	GND	Ground
20	N.C.	No connection	64	N.C.	No connection
21	N.C.		65	N.C.	
22	$\overline{RAS}$ 0	Row address strobe 0	66	$\overline{CAS}$ 2	Column address strobe 2
23	$\overline{CAS}$ 0	Column address strobe 0	67	GND	Ground
24	$\overline{CAS}$ 1	Column address strobe 1	68	$\overline{CAS}$ 3	Column address strobe 3
25	N.C.	No connection	69	N.C.	No connection
26	$\overline{RAS}$ 2	Row address strobe 2	70	$\overline{WE}$	Write enable
27	Vcc	Power supply voltage	71	PD 1 (N.C.)	Presence detect 1
28	PD 2 (GND)	Presence detect 2	72	PD 3 (GND)	Presence detect 3
29	PD 4 (GND)	Presence detect 4	73	GND	Ground
30	PD 6 (GND)	Presence detect 6	74	PD 5 (N.C.)	Presence detect 5
31	N.C.	No connection	75	PD 7 (N.C.)	Presence detect 7
32	N.C.		76	PD 8 (N.C.)	Presence detect 8
33	N.C.		77	N.C.	No connection
34	DQ 9	Data I/O	78	N.C.	
35	N.C.	No connection	79	N.C.	
36	DQ10	Data I/O	80	DQ27	Data I/O
37	Vcc	Power supply voltage	81	DQ28	
38	DQ11	Data I/O	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13		84	DQ31	
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16		87	DQ34	
44	GND	Ground	88	GND	Ground

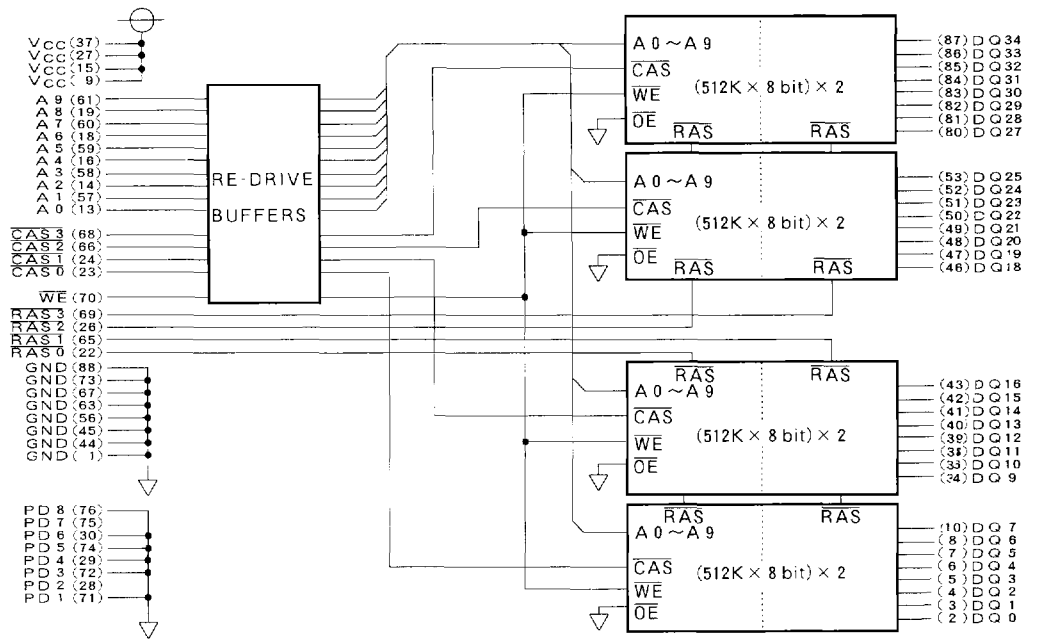
PIN ASSIGNMENT (No.2)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ0	Data I/O	46	DQ18	Data I/O
3	DQ1		47	DQ19	
4	DQ2		48	DQ20	
5	DQ3		49	DQ21	
6	DQ4		50	DQ22	
7	DQ5		51	DQ23	
8	DQ6		52	DQ24	
9	Vcc	Power supply voltage	53	DQ25	
10	DQ7	Data I/O	54	N.C.	No connection
11	N.C.	No connection	55	N.C.	
12	N.C.		56	GND	Ground
13	A0	Address input	57	A1	Address input
14	A2		58	A3	
15	Vcc	Power supply voltage	59	A5	
16	A4	Address input	60	A7	
17	N.C.	No connection	61	A9	
18	A6	Address input	62	N.C.	No connection
19	A8		63	GND	Ground
20	N.C.	No connection	64	N.C.	No connection
21	N.C.		65	$\overline{RAS1}$	Row address strobe 1
22	$\overline{RAS0}$	Row address strobe 0	66	$\overline{CAS2}$	Column address strobe 2
23	$\overline{CAS0}$	Column address strobe 0	67	GND	Ground
24	$\overline{CAS1}$	Column address strobe 1	68	$\overline{CAS3}$	Column address strobe 3
25	N.C.	No conneciton	69	$\overline{RAS3}$	Row address strobe 3
26	$\overline{RAS2}$	Row address strobe 2	70	$\overline{WE}$	Write enable
27	Vcc	Power supply voltage	71	PD1 (N.C.)	Presence detect 1
28	PD2 (GND)	Presence detect 2	72	PD3 (GND)	Presence detect 3
29	PD4 (GND)	Presence detect 4	73	GND	Ground
30	PD6 (GND)	Presence detect 6	74	PD5 (GND)	Presence detect 5
31	N.C.	No connection	75	PD7 (N.C.)	Presence detect 7
32	N.C.		76	PD8 (N.C.)	Presence detect 8
33	N.C.		77	N.C.	No connection
34	DQ9	Data I/O	78	N.C.	
35	N.C.	No conneciton	79	N.C.	
36	DQ10	Data I/O	80	DQ27	Data I/O
37	Vcc	Power supply voltage	81	DQ28	
38	DQ11	Data I/O	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13		84	DQ31	
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16		87	DQ34	
44	GND	Ground	88	GND	Ground

BLOCK DIAGRAM (No.1)



BLOCK DIAGRAM (No.2)



FUNCTION TABLE

Operation	Input					input/output		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open
Odd numbered $\overline{RAS}$ signals ($\overline{RAS1}$, $\overline{RAS3}$) and even numbered $\overline{RAS}$ signals ($\overline{RAS0}$, $\overline{RAS2}$) should not be active at the same time during Read and Early write cycles. This comment cloes not apply to MF12M1-L57ATXX series cards.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
V_{CC}	Supply voltage	With respect to GND	−0.5～7		V
V_I	Input voltage		−0.5～V_{CC}+0.5 (7 V MAX)		V
V_O	Output voltage		−0.5～7		V
I_O	Output current		50		mA
P_d	Power dissipation	T_a=25℃	No1	No2	W
			4	8	
T_{opr}	Operating temperature		0～55		℃
T_{stg}	Storage temperature		−40～80		℃

RECOMMENDED OPERATING CONDITIONS (T_a= 0～55℃, unless otherwise noted) : (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage	0	0	0	V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

Note 2 : With respect to GND

ELECTRICAL CHARACTERISTICS (T_a = 0 ~55℃, V_{CC} = 5V ± 5 %, GND = 0 V) : (Note 3)
(MF12M1-L57ATXX)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage	I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current	0V ≦ V_{out} ≦ V_{CC}	No.1 −10 / No.2 −20		No.1 10 / No.2 20	μA
I_I	Input current	0V ≦ V_{in} ≦ V_{CC} other input pins = 0V	−20		20	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 4, 5)	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min, output open			No.1 460 / No.2 480	mA
$I_{CC2(AV)}$	Supply current from V_{CC}, Standby	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.2V other input pins ≧ V_{CC} − 0.2V or ≦ 0.2V, output open			No.1 0.6 / No.2 1	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 4)	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min, output open			No.1 460 / No.2 890	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, Page-mode (Note 4, 5)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{RC} = min, output open			No.1 520 / No.2 550	mA
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 4)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min, output open			No.1 390 / No.2 770	mA
$I_{CC8(AV)}$	Average supply current from V_{CC}, Extended refresh mode (Note 6)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{WE}$ ≧ V_{CC} − 0.2V other input pins ≧ V_{CC} − 0.2V or ≦ 0.2V, output open t_{RC} = 125 μs, t_{RAS} (min) ~1 μs			No.1 1.8 / No.2 3	mA

Note 3 : Current flowing into a CARD is positive, out is negative.
4 : I_{CC}1 (AV), I_{CC}3 (AV), I_{CC}4 (AV) and I_{CC}6 (AV) are dependent on cycle rate.
Specified values are obtained at the fastest cycle rate.
5 : I_{CC}1 (AV) and I_{CC}4 (AV) are dependent on output loading.
Specified values are obtained with the outputs open.

SWITCHING CHARACTERISTICS (T_a = 0 ~ 55℃, V_{CC} = 5V ± 5 %, GND = 0 V) : (Note 6)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7, 8)		27	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7, 9)		70	ns
t_{CAA}	Column Address access time (Note 7, 10)		42	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 11)	0	27	ns

Note 6 : An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 2TTL Load and 100pF.

8 : Assumes that $t_{RCD} \geqq t_{RCD}(max)$ and $t_{ASC} \geqq t_{ASC}(max)$.

9 : Assumes that $t_{RCD} \leqq t_{RCD}(max)$ and $t_{RAD} \leqq t_{RAD}(max)$.

10 : Assumes that $t_{RAD} \geqq t_{RAD}(max)$ and $t_{ASC} \leqq t_{ASC}(max)$.

11 : $t_{OFF}(max)$ define the time at which the output achieves the high impedance state (MF12M1-L57ATXX: $|I_{OUT}| \leqq 10\,\mu A$, MF14M1-L57ATXX: $|I_{OUT}| \leqq 20\,\mu A$) and are not reference to $V_{OH}(min)$ or $V_{OL}(max)$.

TIMING REQUIREMENTS (T_a = 0 ~ 55℃, V_{CC} = 5 V ± 5 %, GND = 0 V) : (Note 12, 13)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{REF}	Refresh cycle time		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note14)	20	43	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low (Note15)	17		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time.	0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note16)	17	28	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	10		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note17)	5	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		ns
t_T	Transition time (Note18)	3	50	ns

Note 12 : The timing requirements are assumed t_T = 5 ns.

13 : $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.

14 : $t_{RCD}(max)$ is specified as a reference point only.
If $t_{RCD} \geqq t_{RCD}(max)$, access time is defined as t_{CAC} and t_{CAA}.

15 : t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

16 : $t_{RAD}(max)$ is specified as a reference point only.
If $t_{RAD} \geqq t_{RAD}(max)$, $t_{ASC} \leqq t_{ASC}(max)$, access time is assumed by t_{CAA} for read cycle.

17 : $t_{ASC}(max)$ is specfied as a reference point only of address access time.

18 : t_T is mearured between $V_{IH}(min)$ and $V_{IL}(max)$.

Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RC}	Read cycle time	130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	5		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{WC}	Write cycle time	130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		ns
t_{DS}	Data setup time	10		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	22		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{PC}	Read, Write cycle time	55		ns
t_{CP}	$\overline{CAS}$ high pulse width	10		ns
t_{RAS}	$\overline{RAS}$ low pulse width (Note 19)	125	10000	ns

Note 19 : $t_{RAS}(min)$ is specified the following formula as two cycles of $\overline{CAS}$ input are executed.
$t_{RAS}(min) = t_{CSH}(min) + t_{PC}(min)$.

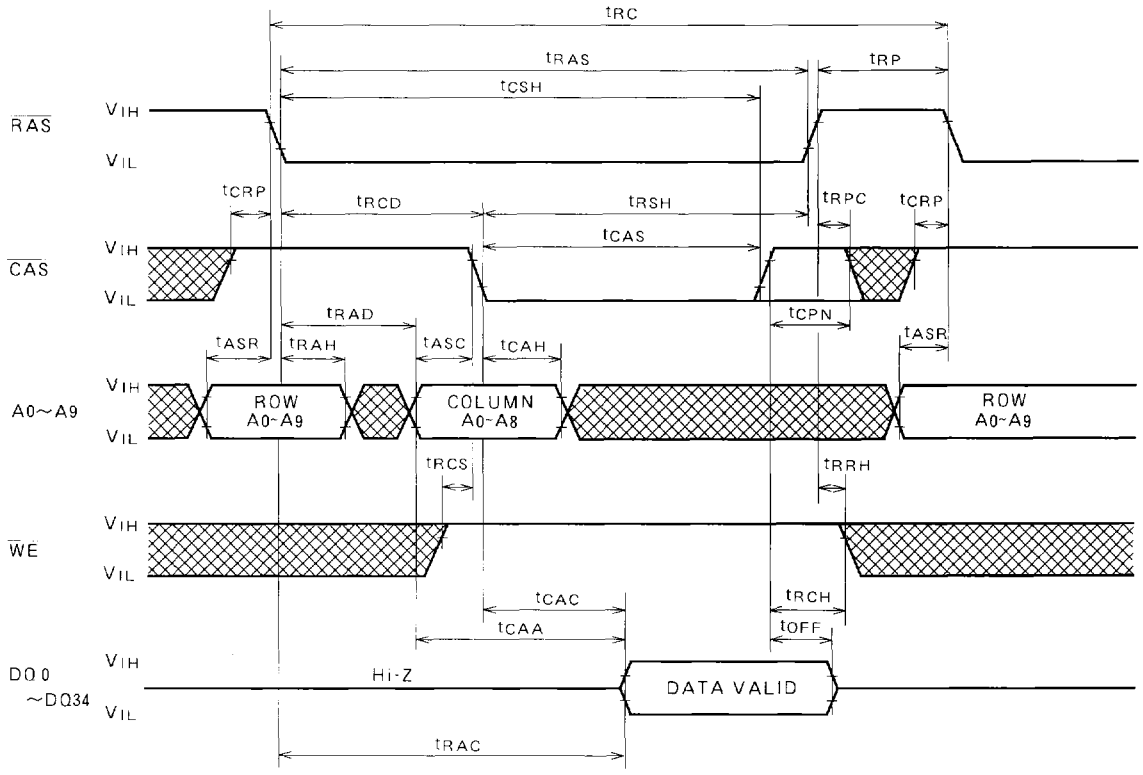
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 20)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		ns

Note 20 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

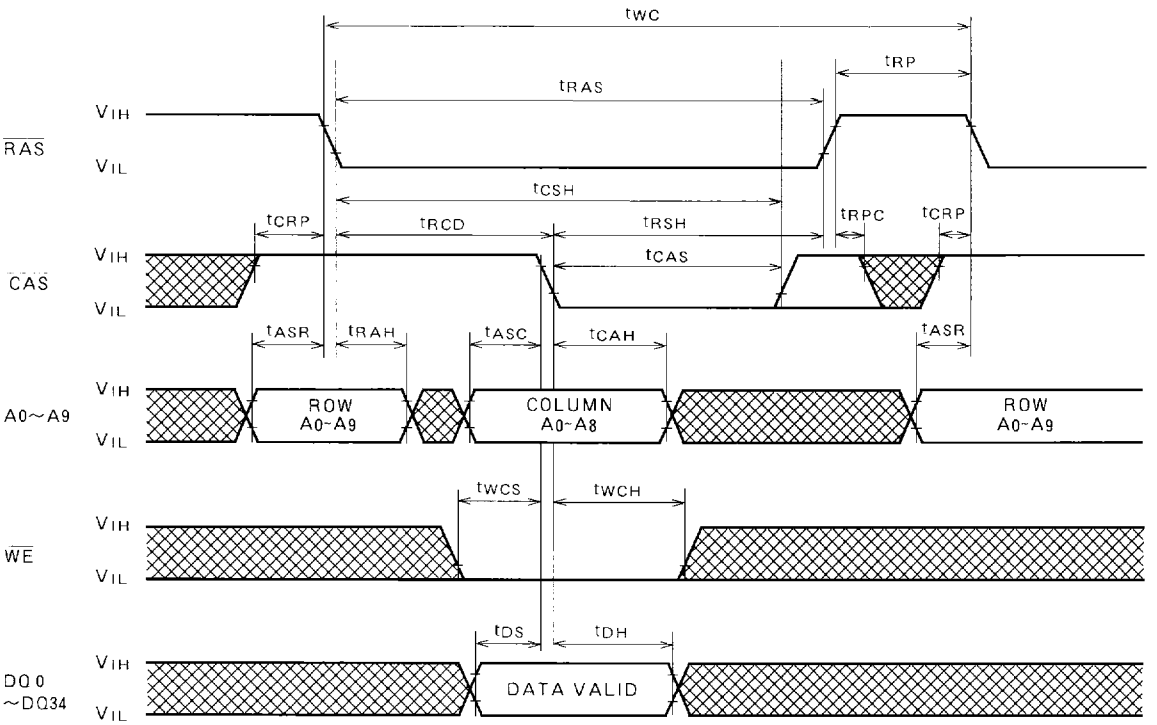
TIMING DIAGRAMS (Note 21)

Read Cycle

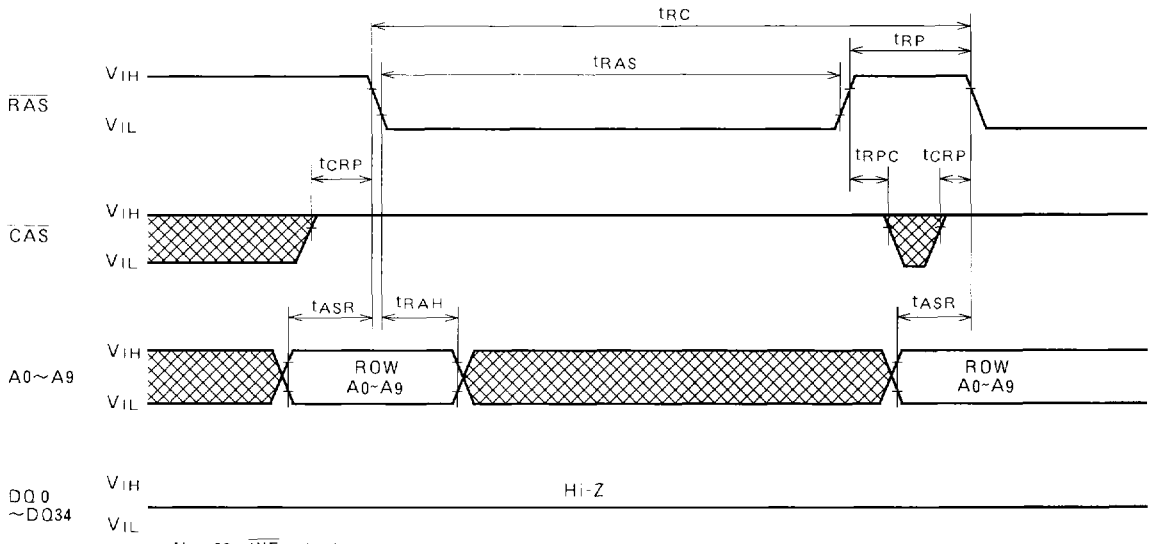


Note21 :  indicates the don't care input

Early Write Cycle

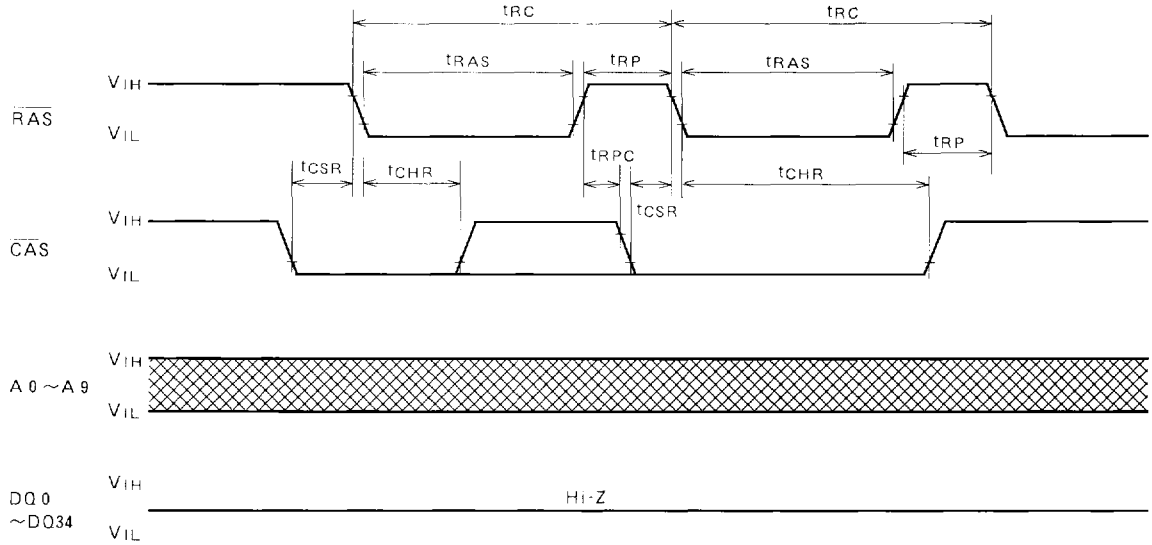


$\overline{RAS}$ only Refresh Cycle (Note 22)



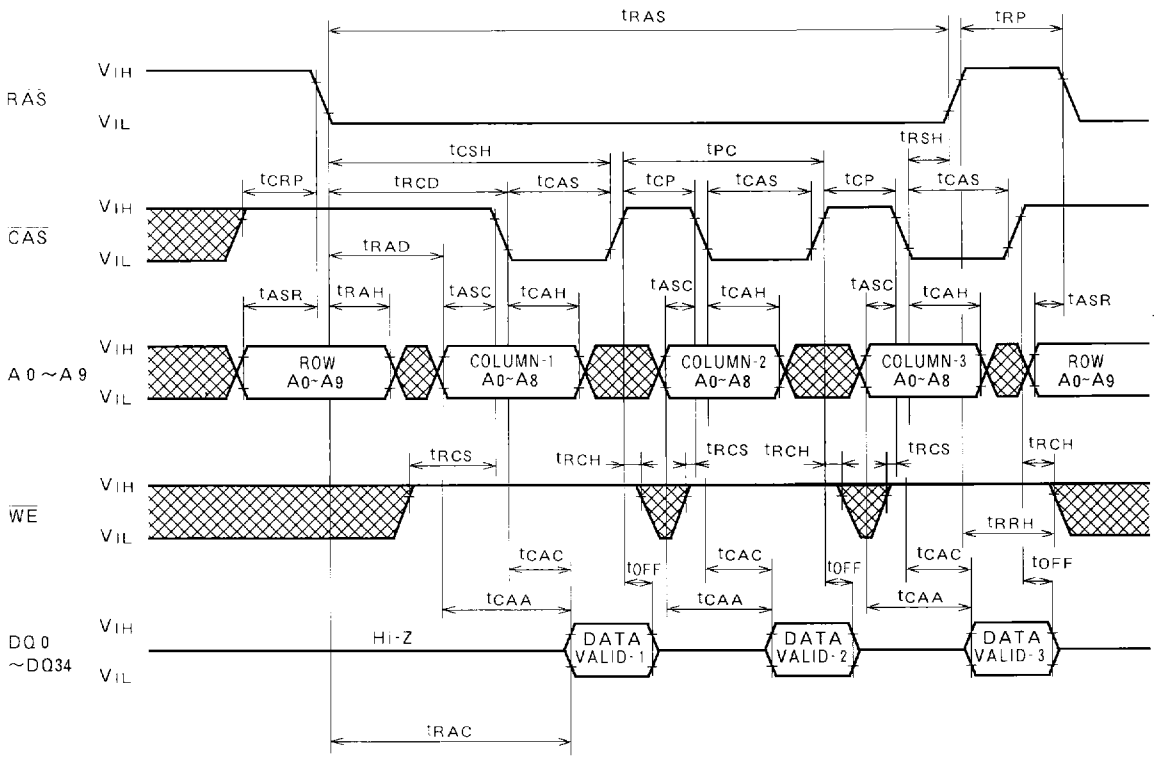
Note22 : $\overline{WE}$ = don't care

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 23)



Note23 : $\overline{WE}$ = V_{IH}

Page-Mode Read Cycle



Page-Mode Early Write Cycle