Chapter 4
Electrical Specifications

4. ELECTRICAL SPECIFICATIONS

4.1 Electrical Connections

4.1.1 Power and Ground Connections and Decoupling

Due to the high frequency of operation of the TI486SLC, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the TI486SLC and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the 14 V_{CC} and 18 GND pins.

4.1.2 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins which are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to V_{CC} and the pull-down resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pull-up or pull-down resistors.

Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	PIN	RESISTOR
A20M#	31	20-kΩ pull-up
BUSY#	34	20-kΩ pull-up
ERROR#	36	20-kΩ pull-up
FLT#	28	20-kΩ pull-up
FLUSH#	30	20-kΩ pull-up
KEN#	29	20-kΩ pull-up
PEREQ	37	20-kΩ pull-down
SUSP#	43	20-kΩ pull-up

It is recommended that the ADS# and LOCK# output pins be connected to pull-up resistors, as indicated in Table 4-2. The external pull-ups guarantee that the signals will remain negated during hold acknowledge states.

Table 4-2. Pins Requiring Additional External Pull-Up Resistors

SIGNAL	PIN	EXTERNAL RESISTOR
ADS#	16	20-kΩ pull-up
LOCK#	26	20-kΩ pull-up

4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 should be connected either to ground or to V_{CC}. Connect active-high inputs to ground through a 20 kΩ (± 10%) pull-down resistor and active-low inputs to V_{CC} through a 20 kΩ (± 10%) pull-up resistor to prevent possible spurious operation.

4.1.4 N/C Designated Pins

Pins designated N/C should be left disconnected. Connecting an N/C pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the TI486SLC and TI486SLC-V microprocessors. Stresses beyond those listed under Table 4-3 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" (Table 4-4) is possible. Exposure to conditions beyond Table 4-3 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-3) may also result in reduced useful life and reliability.

Table 4-3. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Case Temperature	-65°	+110°	C	Power Applied
Storage Temperature	-65°	+150°	C	No Bias
Supply Voltage, V_{CC}	-0.5	6.5	V	With Respect to V_{SS}
Voltage On Any Pin	-0.5	V_{CC} + 0.5	V	With Respect to V_{SS}
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

4.3 Recommended Operating Conditions

The following table presents the recommended operating conditions for the TI486SLC and TI486SLC-V devices. The TI486SLC-V can be operated as a TI486SLC.

Table 4-4. Recommended Operating Conditions

PARAMETER		TI486SLC		TI486SLC-V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
T_C	Case Temperature	0°	+100°	0°	+85°	C	Power Applied
V_{CC}	Supply Voltage	4.5	5.5	2.7	3.6	V	With Respect to V_{SS}
V_{IH}	High Level Input	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V	
V_{IL}	Low Level Input	-0.3	0.8	-0.3	0.6	V	
V_{ILC}	CLK2 Input LOW Voltage	-0.3	0.8	-0.3	0.5	V	
V_{IHC}	CLK2 Input HIGH Voltage	3.7	V_{CC} + 0.3	V_{CC} - 0.5	V_{CC} + 0.3	V	
I_{OH}	Output Current (High)		-1.0		-1.0	mA	$V_{OH}=V_{OH(min)}$
I_{OL}	Output Current (Low)		5.0		3.0	mA	$V_{OL}=V_{OL(max)}$
I_{IK}	Input Clamp Current		+10		+10	mA	$V_{IN}<V_{SS}$ or $V_{IN}>V_{CC}$
I_{OK}	Output Clamp Current		+25		+25	mA	$V_{OUT}<V_{SS}$ or $V_{OUT}>V_{CC}$

4.4 DC Electrical Characteristics

Table 4-5. DC Electrical Characteristics (at Recommended Operating Conditions)

PARAMETER		TI486SLC		TI486SLC-V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
V_{OL}	Output Low Voltage I_{OL} = 3 mA I_{OL} = 5 mA		 0.45		0.35	V	
V_{OH}	Output High Voltage I_{OH} = -1 mA I_{OH} = -0.2 mA	 2.4 V_{CC} - 0.5		 V_{CC} - 0.4 V_{CC} - 0.4		V	
I_{LI}	Input Leakage Current For all pins except for those listed in Table 4-1.		±15		±15	µA	$0 < V_{IN} < V_{CC}$
I_{IH}	Input Leakage Current PEREQ		200		200	µA	V_{IN} = 2.4 Note 1
I_{IL}	Input Leakage Current A20M#, BUSY#, ERROR#, FLT#, FLUSH#, KEN#, SUSP#		- 400		- 400	µA	V_{IL} = 0.45V Note 2
I_{CC}	Active I_{CC} 20 MHz (CLK2 = 40 MHz) 25 MHz (CLK2 = 50 MHz)	Typical: 380 435	 500 550	Typical: 175 220	 230 280	 mA mA	
I_{CCSM}	Suspend Mode ICC 25 MHz (CLK2 = 50 MHz)	Typical: 5.0	 10.0	Typical 3.0	 6.0	mA	Note 3
I_{CCSS}	Standby ICC 0 MHz (Suspended/CLK2 Stopped)	Typical: 100	 250	Typical: 60	 150	µA	Note 3
C_{IN}	Input Capacitance		10		10	pF	f_C = 1 MHz (Note 4)
C_{OUT}	Output or I/O Capacitance		12		12	pF	f_C = 1 MHz (Note 4)
C_{CLK}	CLK2 Capacitance		20		20	pF	f_C = 1 MHz (Note 4)

Notes: 1. PEREQ input has an internal pull-down resistor.
2. A20M#, BUSY#, ERROR#, FLT#, FLUSH#, KEN#, and SUSP# inputs each have an internal pull-up resistor.
3. All inputs at 0.4 or V_{CC}-0.4 (CMOS levels). All inputs held static, (except CLK2 as indicated). All outputs unloaded (static I_{OUT} = 0 mA).
4. Not 100% tested.

4.5 AC Characteristics

Tables 4-7 and 4-8 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figures 4-1 and 4-2. The rising clock edge reference level V_{REFC}, and other reference levels are shown in Table 4-6 below for the TI486SLC and TI486SLC-V. Input or output signals must cross these levels during testing.

Figure 4-1 shows delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

The outputs: A23-A1, ADS#, BHE#, BLE#, D/C#, HLDA, LOCK#, M/IO#, RPLVAL#, and W/R# change only at the beginning of phase one (Figure 4-1). D15-D0 (write cycles), RPLSET and SUSPA# change at the beginning of phase two.

The inputs: BUSY#, D15-D0 (read cycles), ERROR#, FLT#, HOLD, PEREQ, and READY# are sampled at the beginning of phase one (Figure 4-1). A20M#, FLUSH#, INTR, KEN#, NA#, NMI, and SUSP# are sampled at the beginning of phase two.

Table 4-6. Measurement Points for Switching Characteristics

SYMBOL	TI486SLC	TI486SLC-V	UNITS
V_{REFC}	2	1.5	V
V_{REF}	1.5	1.2	V
V_{IHC}	V_{CC} - 0.8	V_{CC} - 0.5	V
V_{ILC}	0.8	0.6	V
V_{IHD}	3	2.3	V
V_{ILD}	0	0	V

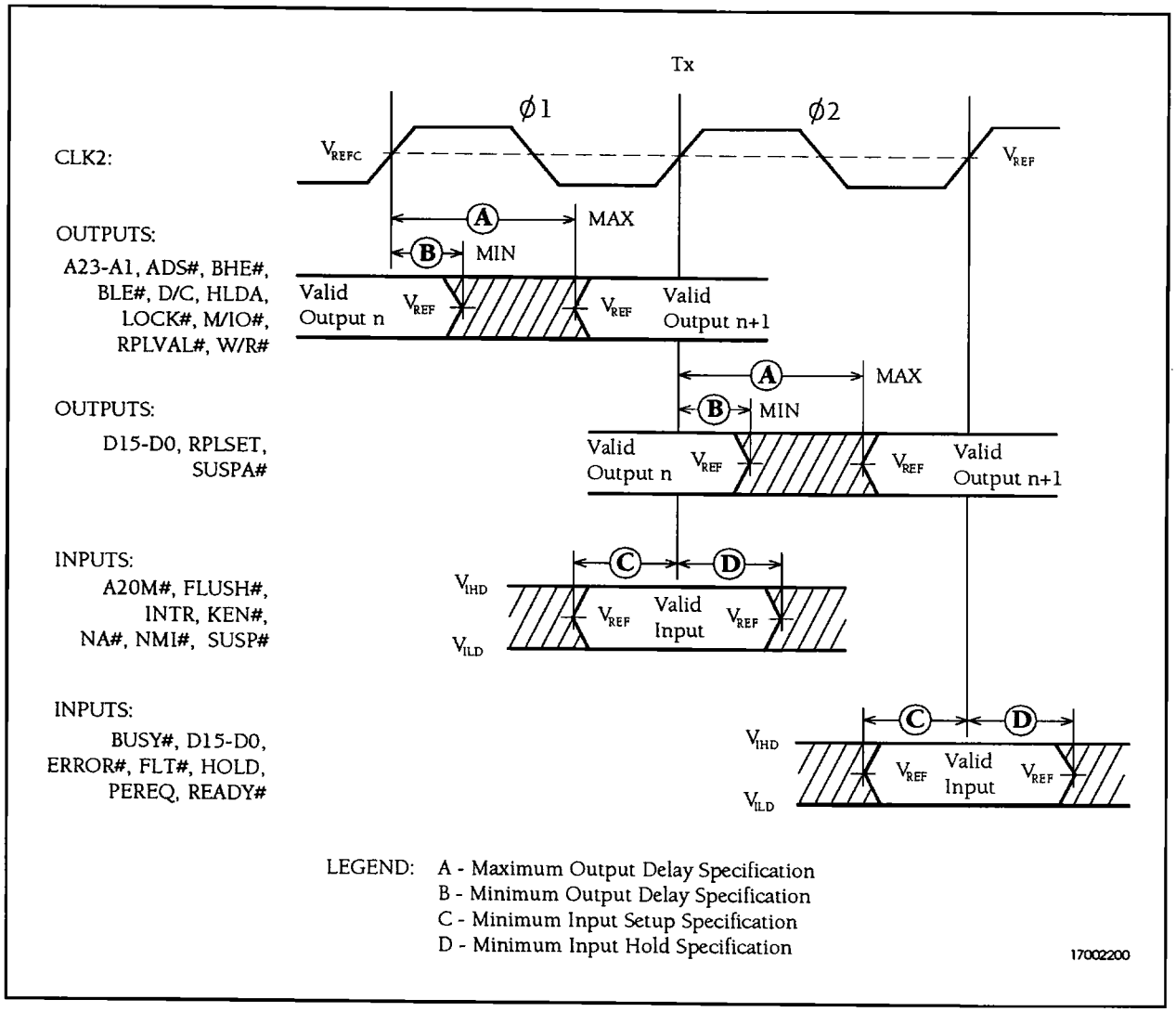

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics

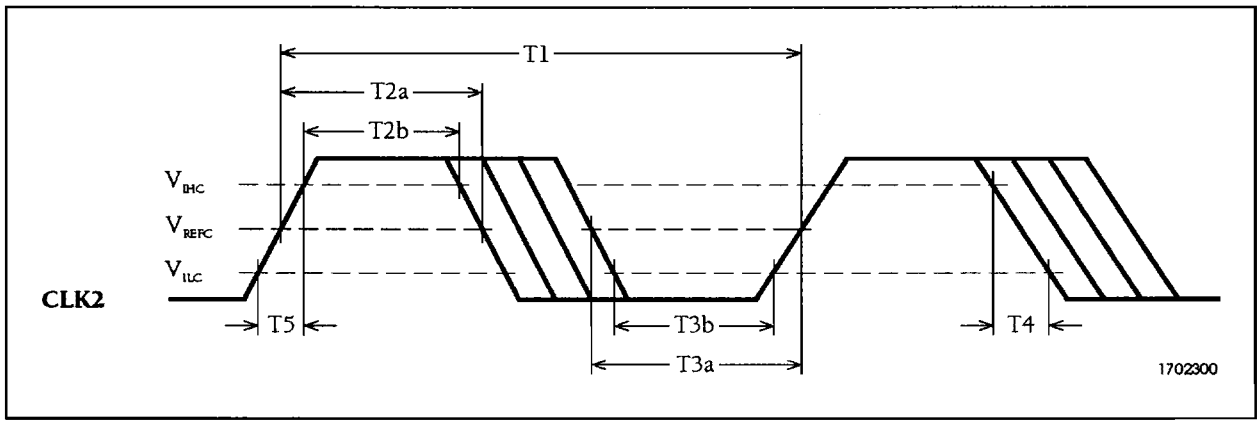

Figure 4-2. CLK2 Timing Measurement Points

Table 4-7. AC Characteristics for TI486SLC-V20

TI486SLC-V20: V_{CC} = 2.7 to 3.6 V, T_C = 0° to 85°C

SYMBOL	PARAMETER	20 MHz		FIGURE	NOTES
		MIN (ns)	MAX (ns)		
T1	CLK2 Period	25		4-2	Note 1
T2a	CLK2 High Time	8		4-2	Note 2
T2b	CLK2 High Time	5		4-2	Note 2
T3a	CLK2 Low Time	8		4-2	Note 2
T3b	CLK2 Low Time	6		4-2	Note 2
T4	CLK2 Fall Time		8	4-2	Note 2
T5	CLK2 Rise Time		8	4-2	Note 2
T6	A23-A1 Valid Delay	4	30	4-4, 4-6	C_L = 50 pF
T7	A23-A1 Float Delay	4	32	4-6	Note 3, Note 6
T8	BHE#, BLE#, LOCK# Valid Delay	4	30	4-4, 4-6	C_L = 50 pF
T9	BHE#, BLE#, LOCK# Float Delay	4	32	4-6	Note 3
T10	ADS#, D/C#, M/IO# RPLVAL#, W/R# Valid Delay	4	26	4-4, 4-6	C_L = 50 pF
T11	ADS#, D/C#, M/IO#, RPLVAL#, W/R# Float Delay	6	30	4-6	Note 3
T12	D15-D0 Write Data, RPLSET, SUSPA# Valid Delay	4	38	4-4, 4-5A	C_L = 50 pF, Note 5
T12A	D15-D0 Write Data Hold Time	4		4-5B	
T13	D15-D0 Write Data, RPLSET, SUSPA# Float Delay	4	27	4-6	Note 3
T14	HLDA Valid Delay	4	28	4-6	C_L = 50 pF
T15	NA#, SUSP#, FLUSH#, KEN#, A20M# Setup Time	5		4-3	
T16	NA#, SUSP#, FLUSH#, KEN#, A20M# Hold Time	12		4-3	
T19	READY# Setup Time	12		4-3	
T20	READY# Hold Time	4		4-3	
T21	D15-D0 Read Data Setup Time	9		4-3	
T22	D15-D0 Read Data Hold Time	6		4-3	
T23	HOLD Setup Time	17		4-3	
T24	HOLD Hold Time	5		4-3	
T25	RESET Setup Time	12		4-7	
T26	RESET Hold Time	4		4-7	
T27	NMI, INTR Setup Time	16		4-3	Note 4
T28	NMI, INTR Hold Time	16		4-3	Note 4
T29	PEREQ, ERROR#, BUSY# Setup Time	14		4-3	Note 4
T30	PEREQ, ERROR#, BUSY# Hold Time	5		4-3	Note 4

Table 4-8. AC Characteristics for TI486SLC-25, TI486SLC-V25

486SLC-25: V_{CC} = 5.0 V ± 10%, T_C = 0° to 100°C 486SLC-V25: V_{CC} = 2.7 to 3.6 V, T_C = 0° to 85° C

SYMBOL	PARAMETER	25 MHz		FIGURE	NOTES
		MIN (ns)	MAX (ns)		
T1	CLK2 Period	20		4-2	Note 1
T2a	CLK2 High Time	7		4-2	Note 2
T2b	CLK2 High Time	4		4-2	Note 2
T3a	CLK2 Low Time	7		4-2	Note 2
T3b	CLK2 Low Time	5		4-2	Note 2
T4	CLK2 Fall Time		7	4-2	Note 2
T5	CLK2 Rise Time		7	4-2	Note 2
T6	A23-A1 Valid Delay	4	21	4-4, 4-6	C_L = 50 pF
T7	A23-A1 Float Delay	4	30	4-6	Note 3, Note 6
T8	BHE#, BLE#, LOCK# Valid Delay	4	21	4-4, 4-6	C_L = 50 pF
T9	BHE#, BLE#, LOCK# Float Delay	4	30	4-6	Note 3
T10	ADS#, D/C#, M/IO#, RPLVAL#, W/R# Valid Delay	4	21	4-4, 4-6	C_L = 50 pF
T11	ADS#, D/C#, M/IO#, RPLVAL#, W/R# Float Delay	4	30	4-6	Note 3
T12	D15-D0 Write Data, RPLSET, SUSPA# Valid Delay	7	27	4-4, 4-5A	C_L = 50 pF, Note 5
T12a	D15-D0 Write Data Hold Time	2		4-5B	
T13	D15-D0 Write Data, RPLSET, SUSPA# Float Delay	4	22	4-6	Note 3
T14	HLDA Valid Delay	4	22	4-6	C_L = 50 pF
T15	NA#, SUSP#, FLUSH#, KEN#, A20M# Setup Time	5		4-3	
T16	NA#, SUSP#, FLUSH#, KEN#, A20M# Hold Time	3		4-3	
T19	READY# Setup Time	9		4-3	
T20	READY# Hold Time	4		4-3	
T21	D15-D0 Read Data Setup Time	7		4-3	
T22	D15-D0 Read Data Hold Time	5		4-3	
T23	HOLD Setup Time	9		4-3	
T24	HOLD Hold Time	3		4-3	
T25	RESET Setup Time	8		4-7	
T26	RESET Hold Time	3		4-7	
T27	NMI, INTR Setup Time	6		4-3	Note 4
T28	NMI, INTR Hold Time	6		4-3	Note 4
T29	PEREQ, ERROR#, BUSY# Setup Time	6		4-3	Note 4
T30	PEREQ, ERROR#, BUSY# Hold Time	5		4-3	Note 4

AC Characteristics Notes:

1. Input clock can be stopped, therefore minimum CLK2 frequency is 0 MHz.
2. These parameters are not tested. They are guaranteed by design characterization.
3. Float condition occurs when maximum output current becomes less than I_{LI} in magnitude. Float is not 100% tested.
4. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
5. T12 minimum time is not 100% tested.
6. SUSPA# floats only in response to activation of FLT#. SUSPA# does not float during a hold acknowledge state.

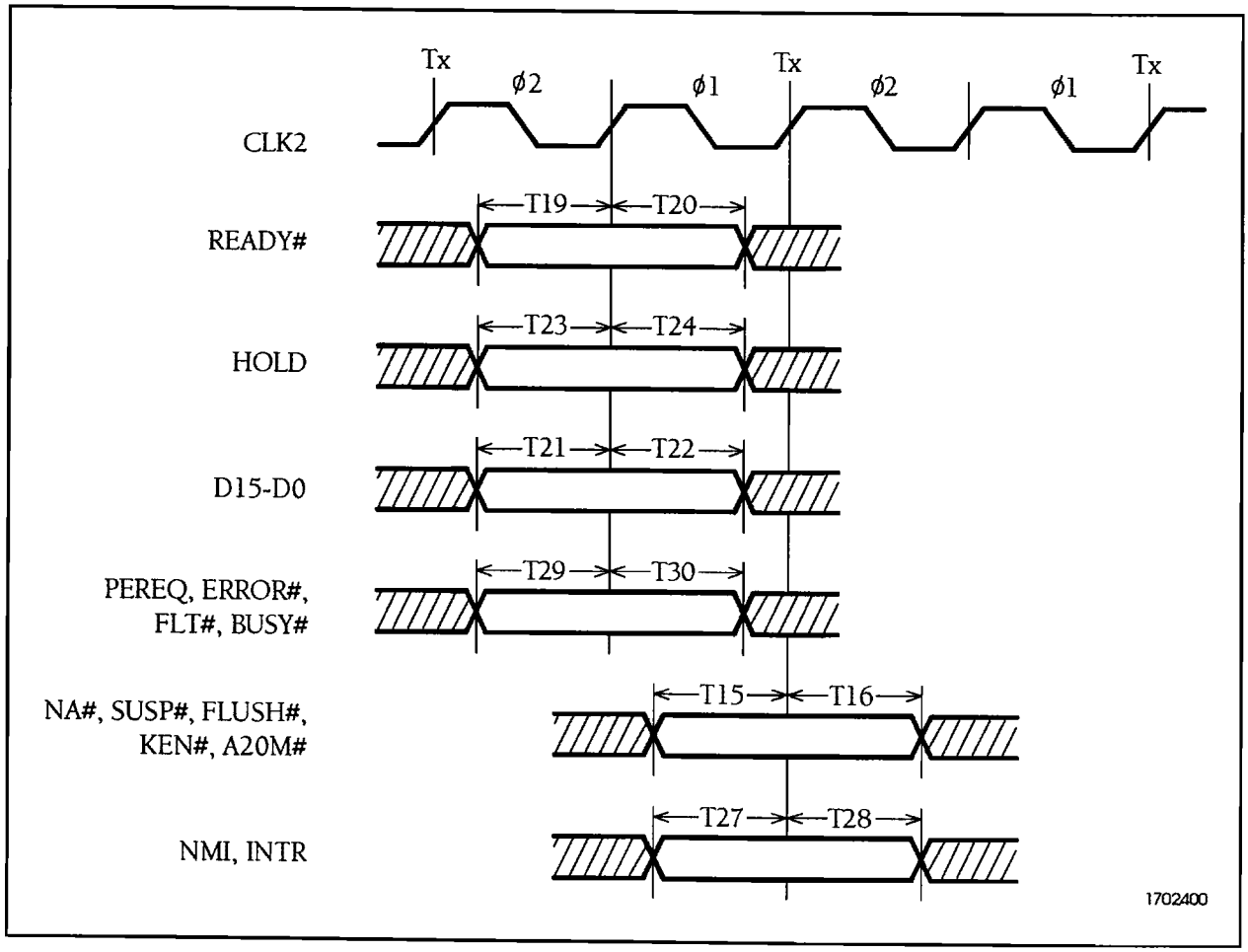

Figure 4-3. Input Signal Setup and Hold Timing

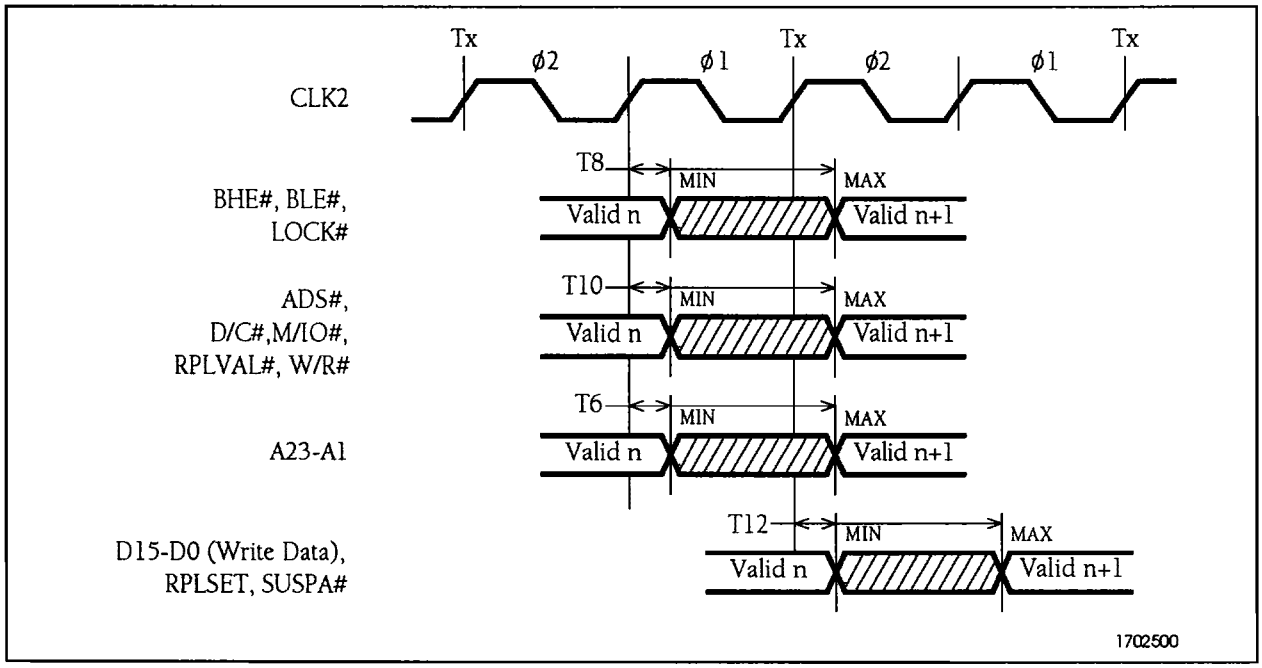

Figure 4-4. Output Signal Valid Delay Timing

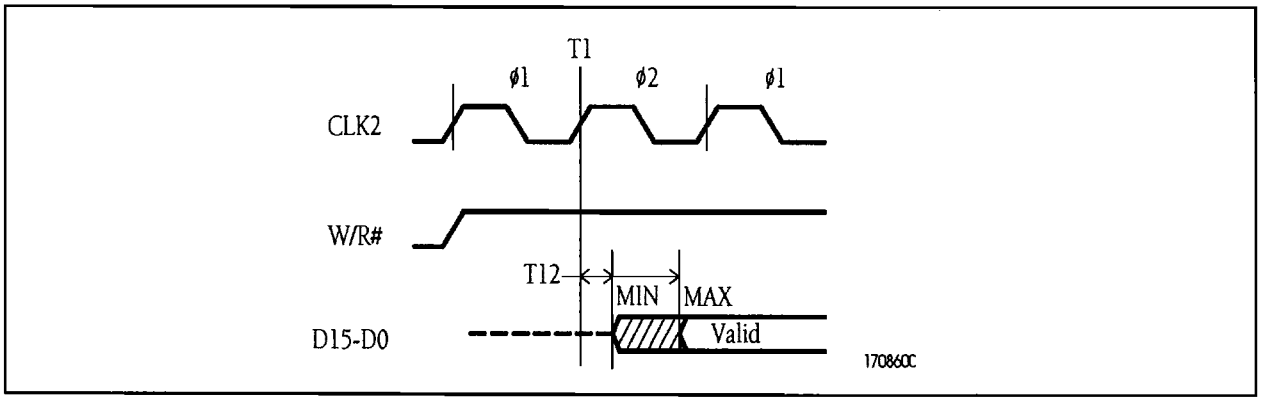

Figure 4-5A. Data Write Cycle Valid Delay Timing

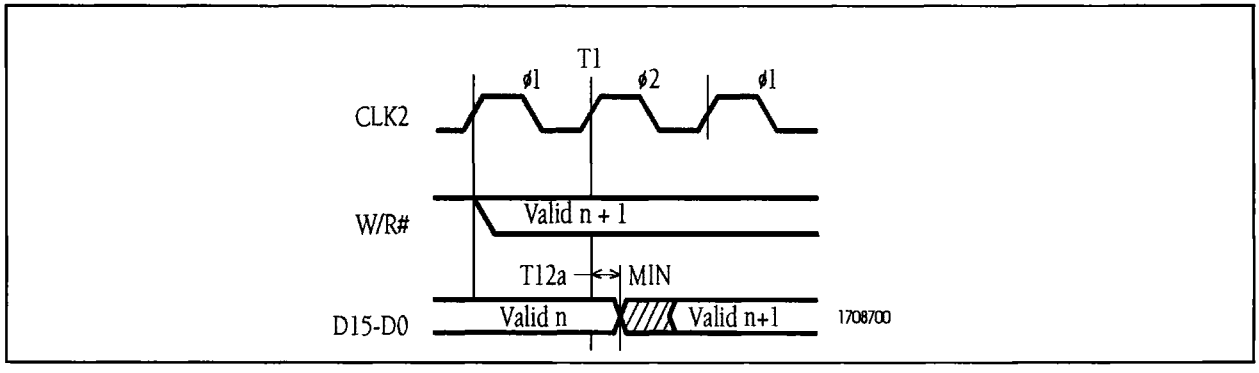

Figure 4-5B. Data Write Cycle Hold Timing

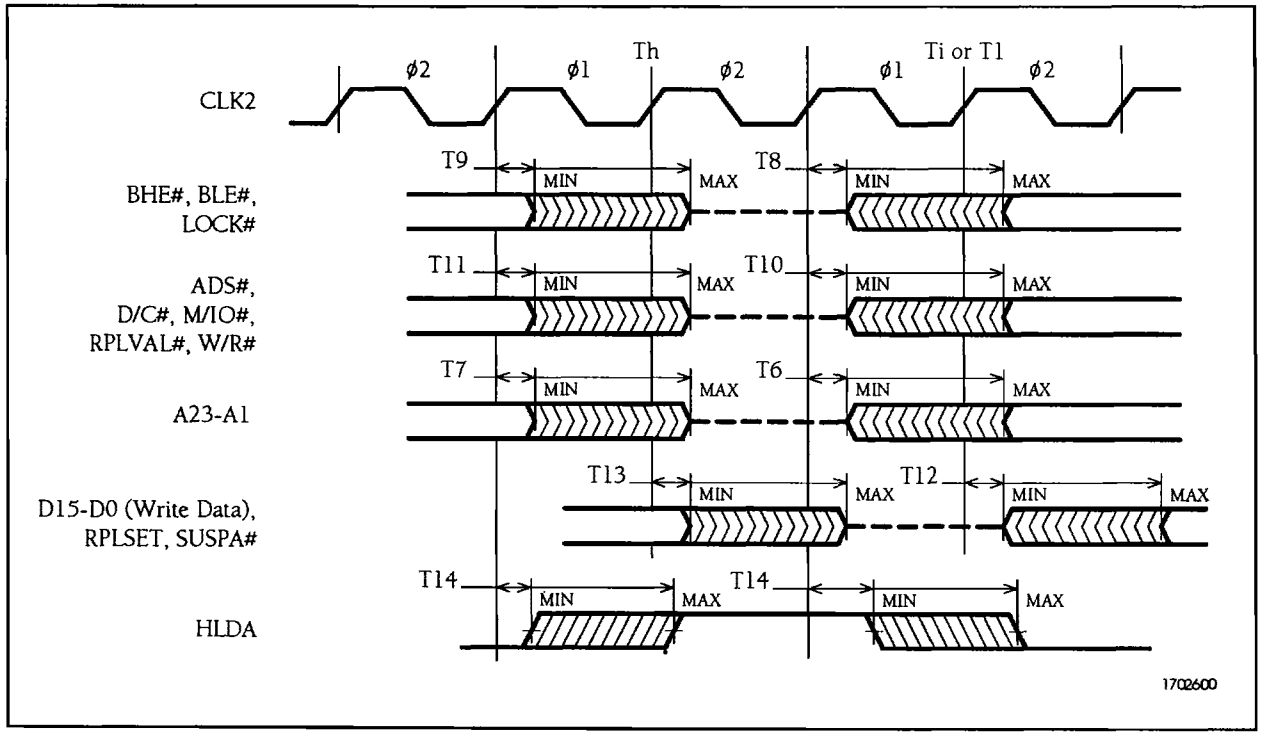

Figure 4-6. Output Signal Float Delay and HLDA Valid Delay Timing

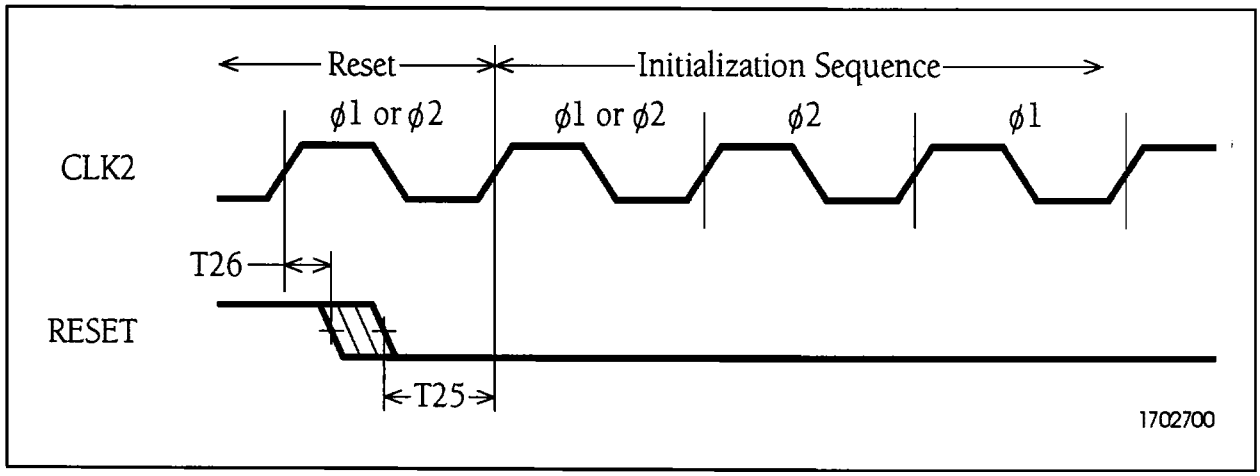

Figure 4-7. RESET Setup and Hold Timing