

**KS54HCTLS  
KS74HCTLS 597**

**8-Bit Shift-Registers with  
Input Latches**

T-46-09-05

**FEATURES**

- 8-Bit Parallel Storage Register Inputs
- Shift Register has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

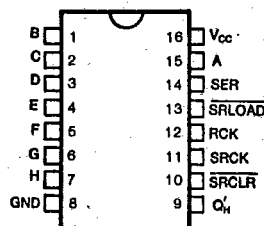
**DESCRIPTION**

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

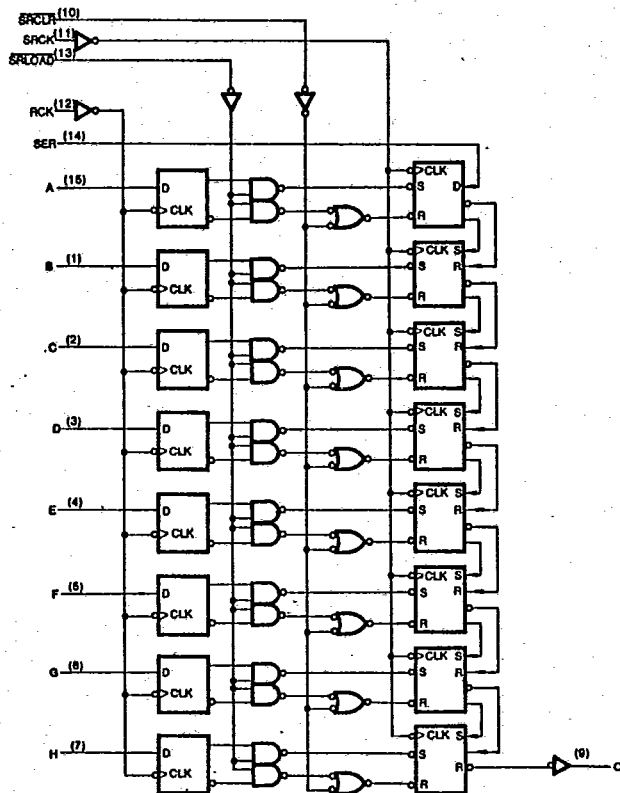
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**KS54HCTLS**  
**KS74HCTLS** **597**

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**Input Latches** T-46-09-05

**FUNCTION TABLE**

| INPUTS |      |       |        |     | FUNCTION   |
|--------|------|-------|--------|-----|--|
| SER    | SRCK | SRCLR | SRLOAD | RCK |  |
| X      | X    | L     | H      | X   | S.R. is cleared to "L"   |
| X      | X    | H     | J      | X   | Input register data is stored into S.R.  |
| L      |      | H     | H      | X   | First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.  |
| H      |      | H     | H      | X   | First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively. |
| X      | X    | X     | X      |     | State of S.R. is not changed.  |
| X      | X    | X     | X      |     | Input data on A~H line is stored into input register   |
| X      | X    | X     | X      |     | Storage register state is not changed.   |

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature Range  
 KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

5

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

| Characteristic                       | Symbol          | Test Conditions  | $T_a = 25^\circ C$ |   |  | Unit                  |         |
|--------------------------------------|-----------------|--|--------------------|---|--|-----------------------|---------|
|                                      |                 |  | Typ                | KS74HCTLS<br>$T_a = -40^\circ C$ to $+85^\circ C$ | KS54HCTLS<br>$T_a = -55^\circ C$ to $+125^\circ C$ |                       |         |
| Minimum High-Level Input Voltage     | $V_{IH}$        |  | 2.0                | 2.0   | 2.0  | V                     |         |
| Maximum Low-Level Input Voltage      | $V_{IL}$        |  | 0.8                | 0.8   | 0.8  | V                     |         |
| Minimum High-Level Output Voltage    | $V_{OH}$        | $V_{IN}=V_{IH}$ or $V_{IL}$<br>$I_O = -20\mu A$<br>$I_O = -4mA$                          | $V_{CC}$<br>4.2    | $V_{CC} - 0.1$<br>3.98                            | $V_{CC} - 0.1$<br>3.84                             | $V_{CC} - 0.1$<br>3.7 | V       |
| Maximum Low-Level Output Voltage     | $V_{OL}$        | $V_{IN}=V_{IH}$ or $V_{IL}$<br>$I_O = 20\mu A$<br>$I_O = 4mA$<br>$I_O = 8mA$             | 0                  | 0.1<br>0.26<br>0.39                               | 0.1<br>0.33<br>0.5                                 | 0.1<br>0.4            | V       |
| Maximum Input Current                | $I_{IN}$        | $V_{IN}=V_{CC}$ or GND   |                    | $\pm 0.1$   | $\pm 1.0$  | $\pm 1.0$             | $\mu A$ |
| Maximum Quiescent Supply Current     | $I_{CC}$        | $V_{IN}=V_{CC}$ or GND<br>$I_{OUT}=0\mu A$   |                    | 8.0   | 80.0   | 160.0                 | $\mu A$ |
| Additional Worst Case Supply Current | $\Delta I_{CC}$ | per input pin<br>$V_I = 2.4V$<br>other inputs:<br>at $V_{CC}$ or GND<br>$I_{OUT}=0\mu A$ |                    | 2.7   | 2.9  | 3.0                   | mA      |

KS54HCTLS  
KS74HCTLS **597****8-Bit Shift-Registers with  
Input Latches T-46-09-05****AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS597

| Characteristic  | Symbol                     | Conditions†         | $T_a = 25^\circ\text{C}$<br>$V_{CC} = 5.0\text{V}$ |                   | KS74HCTLS  | KS54HCTLS   | Unit |    |
|---|----------------------------|---------------------|--|-------------------|--|---|------|----|
|   |                            |                     |  |                   | $T_a = -40^\circ\text{C to } +85^\circ\text{C}$<br>$V_{CC} = 5.0\text{V} \pm 10\%$ | $T_a = -55^\circ\text{C to } +125^\circ\text{C}$<br>$V_{CC} = 5.0\text{V} \pm 10\%$ |      |    |
|   |                            |                     | Typ  | Guaranteed Limits |  |   |      |    |
| Maximum Clock Frequency                                 | $f_{max}$                  |                     | 35   | 25                | 20   | 20  | MHz  |    |
| Maximum Propagation Delay,<br>SRCK† to Q <sub>H</sub>   | $t_{PLH}$                  | $C_L = 50\text{pF}$ | 15   | 18                | 25   | 30  | ns   |    |
|   | $t_{PHL}$                  |                     | 15   | 18                | 25   | 30  |      |    |
| Maximum Propagation Delay,<br>SRLOAD† to Q <sub>H</sub> | $t_{PLH}$                  |                     | 18   | 24                | 30   | 36  | ns   |    |
|   | $t_{PHL}$                  |                     | 18   | 24                | 30   | 36  |      |    |
| Maximum Propagation Delay,<br>SRCLR† to Q <sub>H</sub>  | $t_{PHL}$                  |                     |  | 17                | 22   | 28  | 33   | ns |
| Maximum Propagation Delay,<br>RCK† to Q <sub>H</sub>    | $t_{PLH}$                  |                     | $C_L = 50\text{pF}$<br>SLOAD=Low                   | 21                | 29   | 35  | 42   | ns |
|   | $t_{PHL}$                  | 21                  |  | 29                | 35   | 42  |      |    |
| Minimum<br>Pulse Width                                  | RCK or SRCK<br>High or Low | $t_w$               | 12   | 16                | 20   | 24  | ns   |    |
|   | SRCLR† or<br>SRLOAD Low    |                     | 12   | 16                | 20   | 24  |      |    |
| Minimum<br>Setup Time                                   | SRCLR† before<br>SRCK†     | $t_{su}$            | 12   | 16                | 20   | 24  | ns   |    |
|   | RCK† before<br>SRCK†††     |                     | 24   | 32                | 40   | 48  |      |    |
|   | SER before<br>SRCK†        |                     | 12   | 16                | 20   | 24  |      |    |
|   | A thru H before<br>RCK†    |                     | 12   | 16                | 20   | 24  |      |    |
| Minimum Hold Time                                       | $t_h$                      |                     | -3   | 0                 | 0  | 0   | ns   |    |
| Maximum Input Capacitance                               | $C_{IN}$                   |                     | 5  |                   |  |   | pF   |    |
| Power Dissipation Capacitance*                          | $C_{PD}$                   |                     |  |                   |  |   | pF   |    |

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

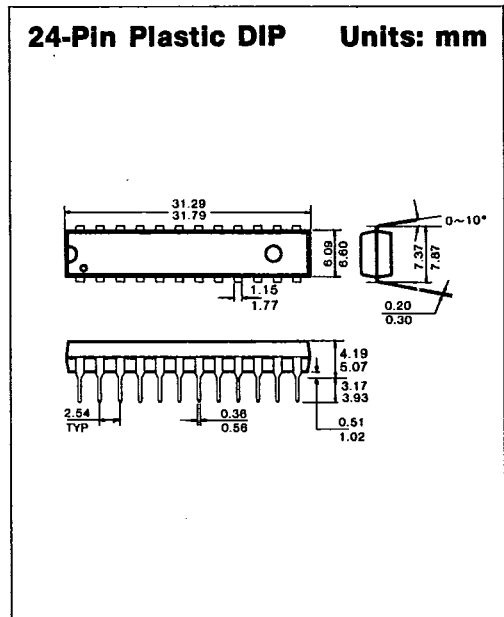
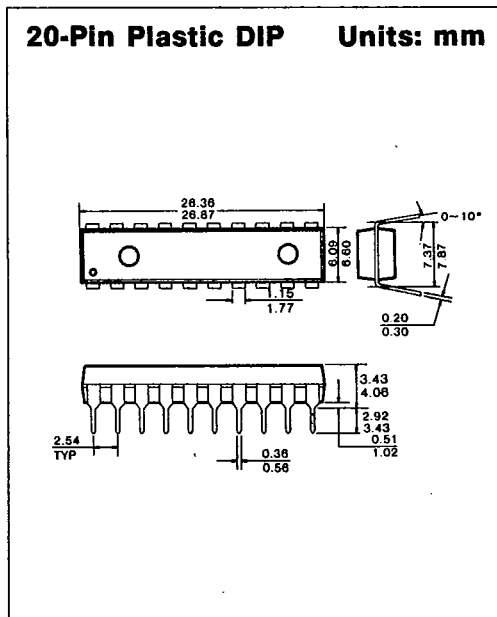
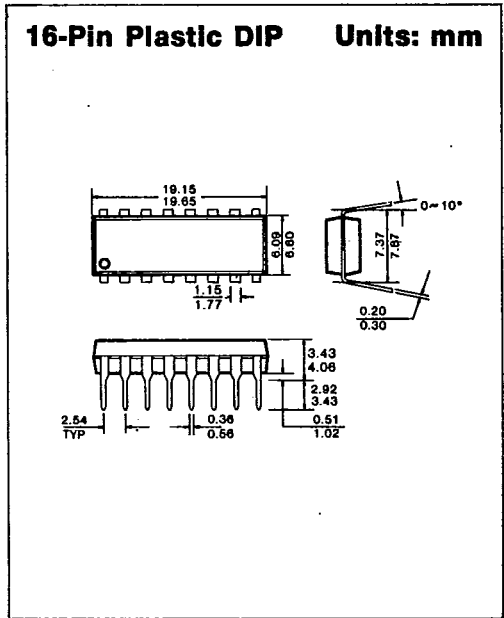
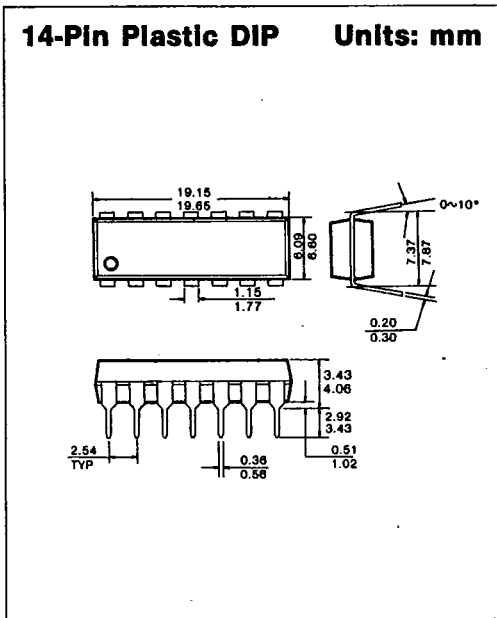
†† The RCK† before SRCK† setup time ensures that shift register will see stable data coming from the register output.



**PACKAGE DIMENSIONS**

T-90-20

**1. PLASTIC PACKAGES**



7



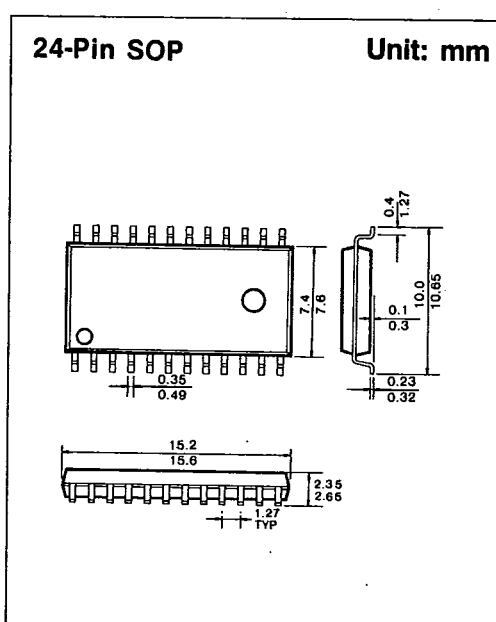
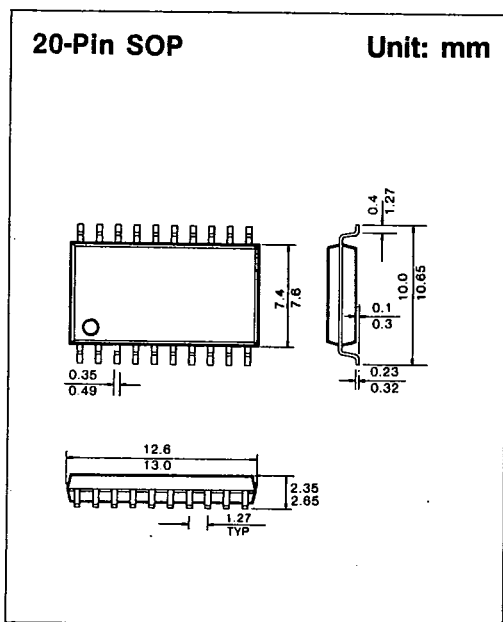
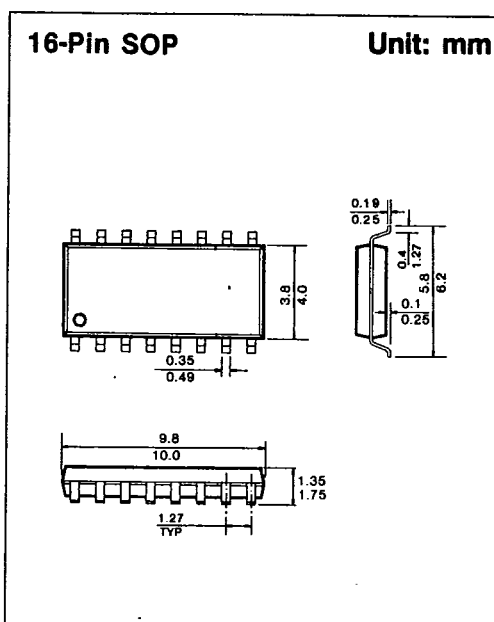
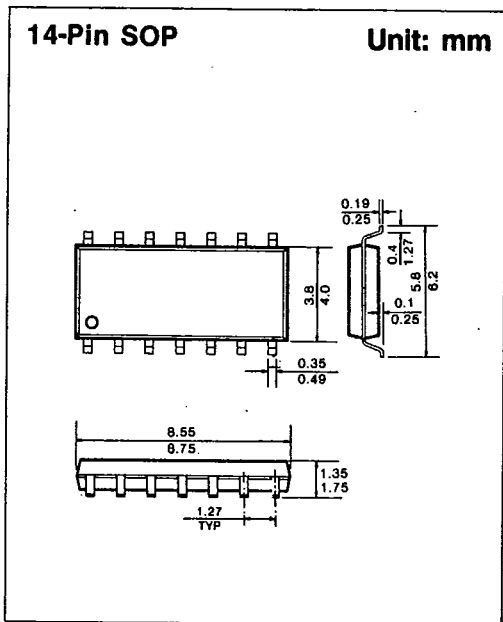
SAMSUNG SEMICONDUCTOR

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**PACKAGE DIMENSIONS**

T-90-20



**PACKAGE DIMENSIONS**

T-90-20

**2. CERAMIC PACKAGES**

**14-Pin Ceramic DIP Units: mm**

| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | —           | 5.08  |
| B              | 0.38        | 0.58  |
| B <sub>1</sub> | 1.40        | 1.78  |
| C              | 0.20        | 0.38  |
| D              | 18.16       | 19.56 |
| E              | 8.10        | 7.49  |
| E <sub>1</sub> | 7.82        | 10.03 |
| F              | 2.54        |       |
| L              | 3.18        | 4.19  |
| Q              | 0.51        | 1.02  |
| S              | 1.91        | 2.29  |

**16-Pin Ceramic DIP Units: mm**

| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | —           | 5.08  |
| B              | 0.38        | 0.58  |
| B <sub>1</sub> | 1.40        | 1.78  |
| C              | 0.20        | 0.38  |
| D              | 19.05       | 19.94 |
| E              | 8.10        | 7.49  |
| E <sub>1</sub> | 7.82        | 10.03 |
| F              | 2.54        |       |
| L              | 3.18        | 4.19  |
| Q              | 0.51        | 1.02  |
| S              | 0.51        | 1.14  |

**20-Pin Ceramic DIP Units: mm**

| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | 4.06        | 5.08  |
| B              | 0.38        | 0.53  |
| B <sub>1</sub> | 1.14        | 1.52  |
| C              | 0.20        | 0.38  |
| D              | 25.78       | 26.33 |
| E              | 8.10        | 8.60  |
| E <sub>1</sub> | 7.77        | 7.95  |
| F              | 2.54        |       |
| L              | 3.73        | 4.01  |
| Q              | 0.38        | 0.89  |
| S              | 0.51        | 1.14  |

**24-Pin Ceramic DIP Units: mm**

| Dim            | Millimeters |       |
|----------------|-------------|-------|
|                | Min         | Max   |
| A              | 4.06        | 5.08  |
| B              | 0.38        | 0.53  |
| B <sub>1</sub> | 1.14        | 1.52  |
| C              | 0.20        | 0.38  |
| D              | 31.50       | 32.84 |
| E              | 7.24        | 7.75  |
| E <sub>1</sub> | 7.77        | 7.98  |
| F              | 2.54        |       |
| L              | 3.73        | 4.01  |
| Q              | 0.508       | 1.776 |
| S              | 1.85        | 1.93  |

7