

4 M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE BUFFERED TYPE

Description

The MC-454BC72 is a 4,194,304 words by 72 bits synchronous dynamic RAM module on which 18 pieces of 16 M SDRAM : μ PD4516821 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Clock frequency and Burst cycle time

Family	Clock frequency (MAX.)	Burst cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
★ MC-454BC72-A10	100 MHz	10 ns	6.20 W	130 mW
★ MC-454BC72-A12	83 MHz	12 ns	5.55 W	(CMOS level input)

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- ★ Single +3.3 +0.3/-0.15 V power supply
- LVTTTL compatible
- 2,048 refresh cycles / 32 ms
- Burst termination by Burst Stop command and Precharge command
- 200-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Buffered type

The information in this document is subject to change without notice.

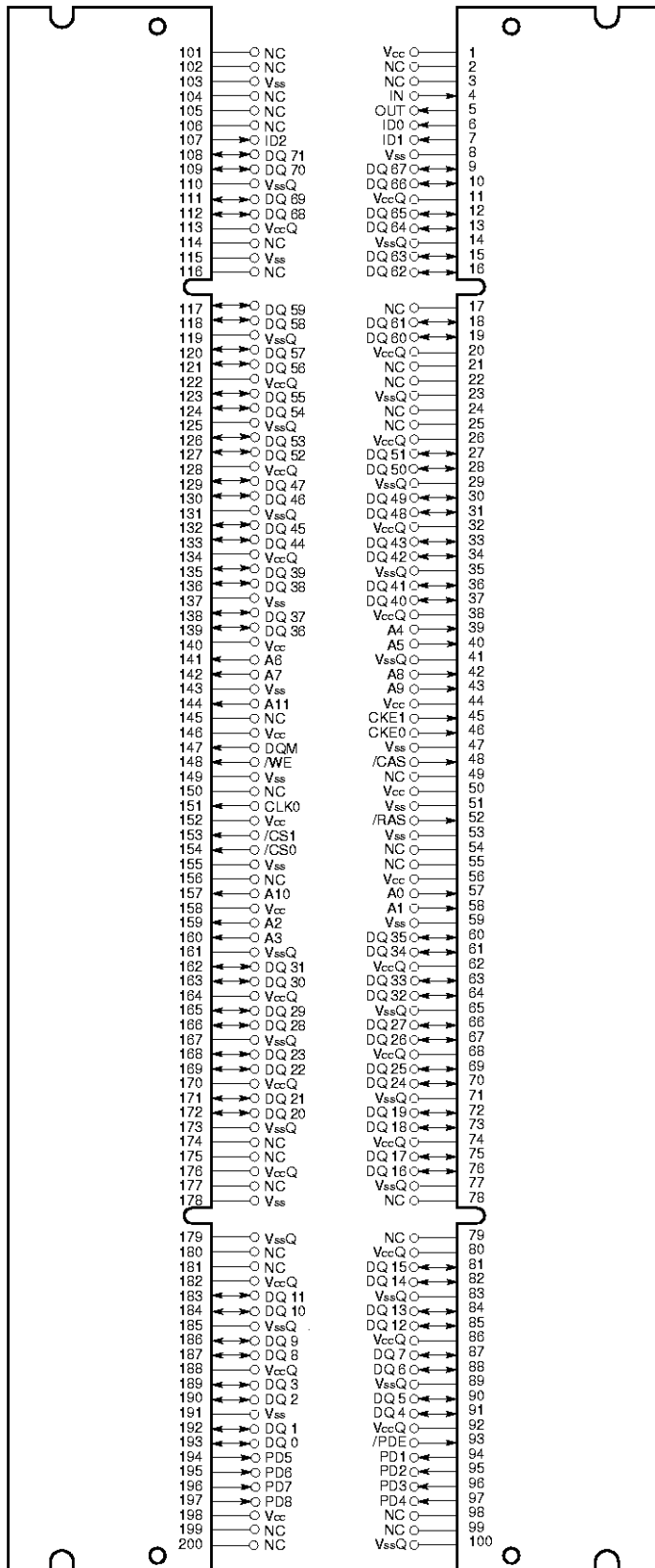
Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-454BC72F-A10	100 MHz	200-pin Dual In-line Memory Module (Socket Type)	18 pieces of 16M SDRAM : μPD4516821 (400mil TSOP (II))
MC-454BC72F-A12	83 MHz	Edge connector : Gold plated	[Double side]

Pin Configuration

200-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plated)

[MC-454BC72F]



PD and ID Table

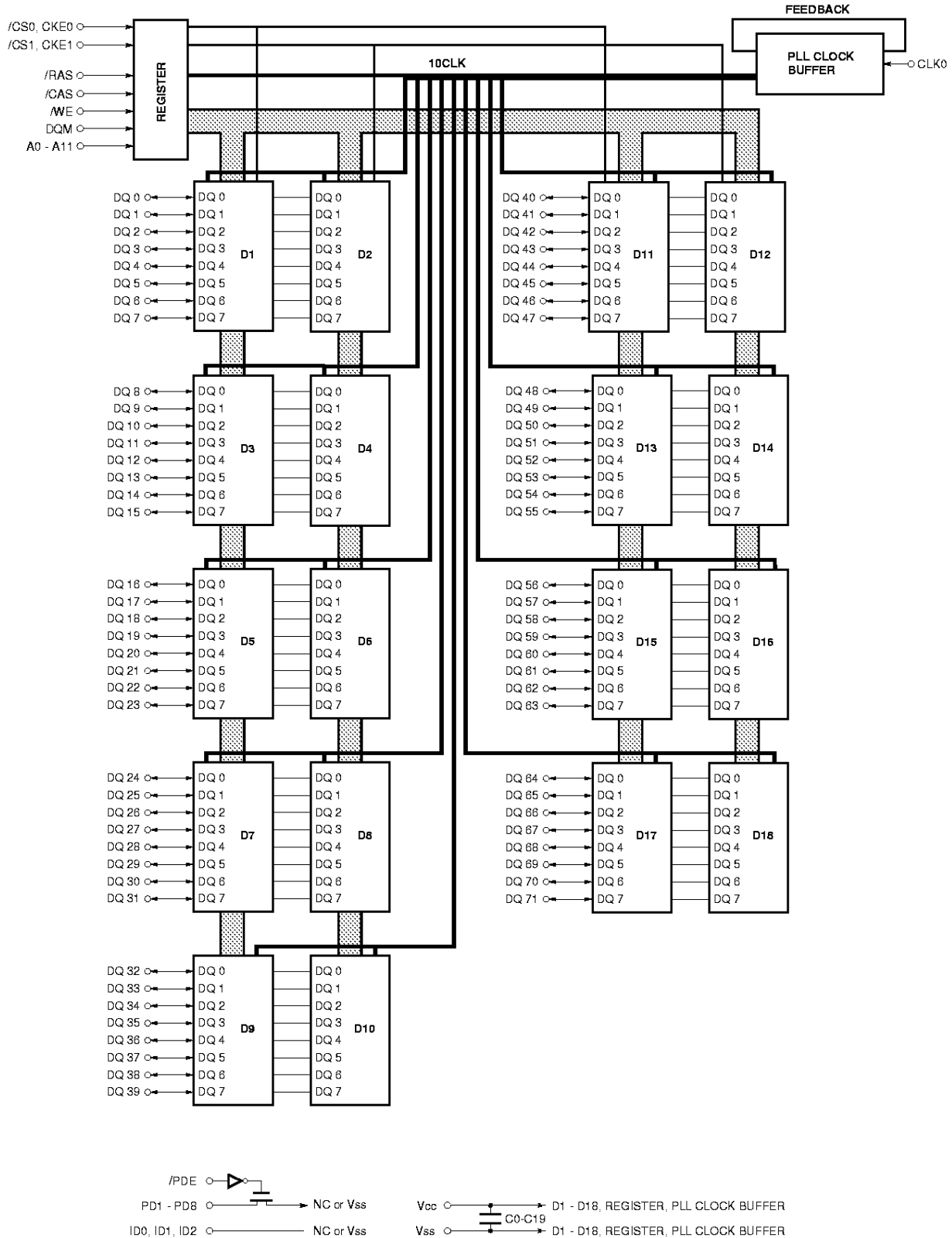
Pin name	Pin No.	Speed	
		10 ns	12 ns
PD1	94	H	H
PD2	95	L	L
PD3	96	L	L
PD4	97	L	L
PD5	194	H	L
PD6	195	L	H
PD7	196	H	H
PD8	197	H	H
ID0	6	H	H
ID1	7	L	L
ID2	107	L	L

Remark

- PD : PD and ID must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will either be open (NC) or driven to Vss via on-board buffer circuits.
- ID : IDs will either be open(NC) or connected directly to Vss without a buffer.

- A0 - A11 : Address Inputs
- [Row : A0 - A10, Column : A0 - A8]
- DQ0 - DQ71 : Data Inputs/Outputs
- CLK0 : Clock Input
- CKE0, CEK1 : Clock Enable Input
- /CS0, /CS1 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQM : DQ Mask Enable
- /PDE : Presence Detect Enable
- PD1 - PD8 : Presence Detect Pins
- ID0 - ID2 : Identify Pins
- IN, OUT : Unbuffered Physical Detect Input/Output (separate)
- Vcc : Power Supply
- VccQ : Power Supply for Data Input/Output
- Vss : Ground
- VssQ : Ground for Data Input/Output
- NC : No Connection

Block Diagram



Remarks 1. A $10\Omega \pm 5\%$ resistor shall be wired in series with DQ0 - DQ71 near the card edge connector. All clock line outputs from the PLL CLOCK BUFFER shall be equal length.

2. D1 - D18 : μ PD4516821 (1M word \times 8 bits \times 2 banks)

Electrical Specifications (Preliminary)

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μ s and then, execute **Power on sequence and Auto Refresh** before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC}		-1.0 to +4.6	V
Voltage on input pin relative to GND	V _T		-1.0 to +4.6	V
Short circuit output current	I _o		50	mA
Power dissipation	P _D		20	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in **Absolute Maximum Ratings** could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to **Absolute Maximum Rating** conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.15	3.3	3.6	V
High level input voltage	V _{IH}		2.0		4.6	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

★

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A11, CKE0, CKE1, /CS0, /CS1, /RAS, /CAS, /WE, DQM			15	pF
	C _{I2}	CLK0			8	
Data input/output capacitance	C _{I/O}	DQ0 - DQ71			15	pF

★ DC Characteristics (Recommended Operating Conditions unless otherwise noted)

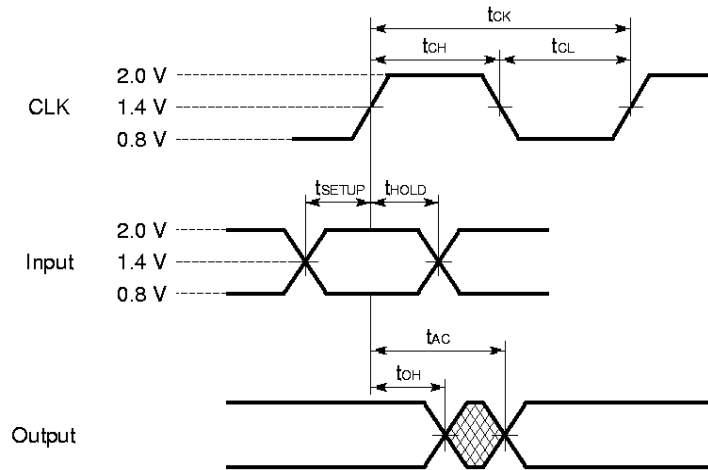
Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC(MIN)} , I _O = 0 mA	/CAS latency = 2		1,272	mA 1
			/CAS latency = 3		1,317	
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX)} , t _{CK} = 15 ns		54	mA 2	
	I _{CC2PS}	CKE ≤ V _{IL(MAX)} , t _{CK} = ∞		36		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN)} , Input signals are changed one time during 30 ns.		450	mA 2	
	I _{CC2NS}	CKE ≥ V _{IH(MIN)} , t _{CK} = ∞ Input signals are stable.		108		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX)} , t _{CK} = 15 ns		54	mA 2	
	I _{CC3PS}	CKE ≤ V _{IL(MAX)} , t _{CK} = ∞		36		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN)} , Input signals are changed one time during 30 ns.		504	mA 2	
	I _{CC3NS}	CKE ≥ V _{IH(MIN)} , t _{CK} = ∞ Input signals are stable.		180		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN)} I _O = 0 mA	/CAS latency = 2	-A10	1,452	mA 3
				-A12	1,272	
			/CAS latency = 3	-A10	1,722	
				-A12	1,542	
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN)}		1,362	mA 4	
Self refresh current	I _{CC6}	CKE ≤ 0.2 V		36	mA 2	
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V	-10	+10	μA	
High level output voltage	V _{OH}	I _O = -2.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +2.0 mA		0.4	V	

- Notes**
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.
 - V_{CC} - 0.2 V ≤ V_{IH(CLK)} ≤ V_{IH(MAX)}, 0 V ≤ V_{IL} ≤ 0.2 V
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.
 - I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

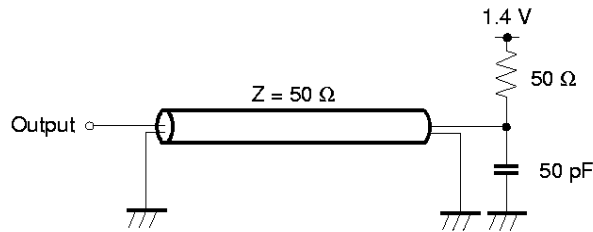
- AC measurements assume $t_r = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL} .
- If t_r is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN)}$ and $V_{IL(MAX)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter	Symbol	-A10		-A12		Unit	Note	
		MIN.	MAX.	MIN.	MAX.			
Clock cycle time	/CAS latency = 3	t _{CK3}	10	(100 MHz)	12	(83 MHz)	ns	
	/CAS latency = 2	t _{CK2}	15	(67 MHz)	18	(55 MHz)	ns	
Access time from CLK	/CAS latency = 3	t _{AC3}		8.5		9.5	ns	1
	/CAS latency = 2	t _{AC2}		9.5		12.5	ns	1
Input CLK duty cycle			40	60	40	60	%	
Data-out hold time	t _{OH}		3.5		3.5		ns	1
Data-out low-impedance time	t _{LZ}		0		0		ns	
Data-out high-impedance time	t _{HZ}		3.5	8.0	3.5	8.0	ns	
Data-in setup time	t _{DS}		3.0		3.5		ns	
Data-in hold time	t _{DH}		1.5		2.0		ns	
Address setup time	t _{AS}		3.5		3.5		ns	
Address hold time	t _{AH}		0.5		0.5		ns	
CKE setup time	t _{CKS}		3.5		3.5		ns	
CKE hold time	t _{CKH}		0.5		0.5		ns	
CKE setup time (Power down exit)	t _{CKSP}		3.0		3.5		ns	
Command (/CS0, /CS1, /RAS, /CAS, /WE, DQM) setup time	t _{CMS}		3.5		3.5		ns	
Command (/CS0, /CS1, /RAS, /CAS, /WE, DQM) hold time	t _{CMH}		0.5		0.5		ns	

Note 1. Output load



Asynchronous Characteristics

Parameter	Symbol	-A10		-A12		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period	t _{RC}	100		102		ns	
ACT to PRE command period	t _{RAS}	60	120,000	72	120,000	ns	
PRE to ACT command period	t _{RP}	30		30		ns	
Delay time ACT to READ/WRITE command	t _{RCD}	30		30		ns	
ACT(one) to ACT(another) command period	t _{RRD}	20		24		ns	
Data-in to PRE command period	t _{DPL}	-1CLK + 10		-1CLK + 12		ns	
Data-in to ACT(REF) command	/CAS latency = 3 /CAS latency = 2	t _{DAL3}	1CLK + 30		1CLK + 30	ns	
period (Auto precharge)		t _{DAL2}	30		30	ns	
Mode register set cycle time	t _{RSC}	20		20		ns	
Transition time	t _T	1	30	1	30	ns	
Refresh time	t _{REF}		32		32	ms	

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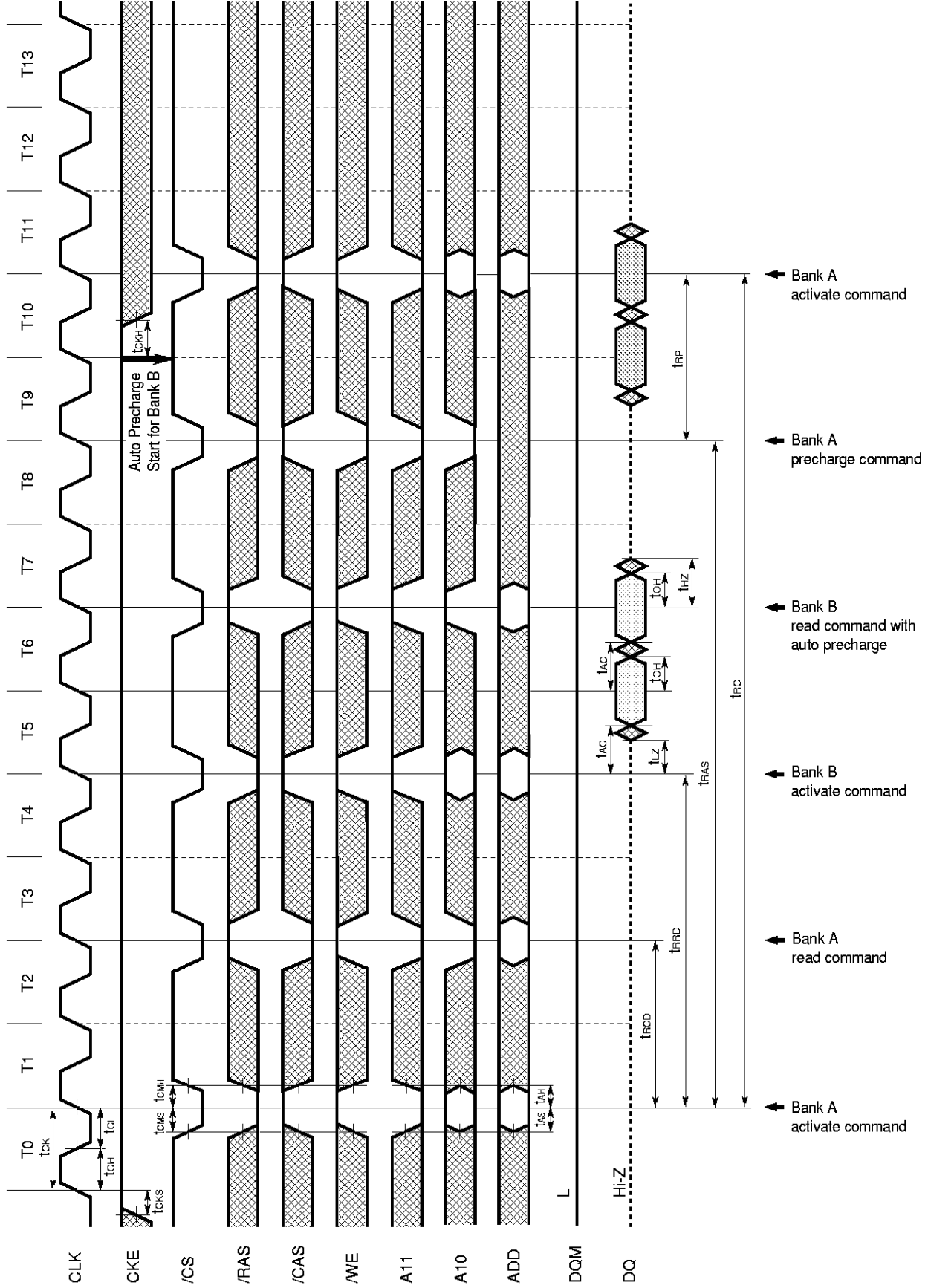
Relationship between Frequency and Latency

Speed version	-A10		-A12	
Clock cycle time [ns]	10	15	12	18
Frequency [MHz]	100	67	83	55
/CAS latency + 1 cycle	3 + 1	2 + 1	3 + 1	2 + 1
[t _{RCD}]	3	2	3	2
/RAS latency (/CAS latency + [t _{RCD}])	7	5	7	5
[t _{RC}]	10	7	9	6
[t _{RAS}]	6	4	6	4
[t _{RRD}]	2	2	2	2
[t _{RP}]	3	2	3	2
[t _{DPL}]	0	0	0	0
[t _{DAL}]	4	2	4	2

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Remark All internal signals (A0-A11, /CS0, /CS1, CKE0, CKE1, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

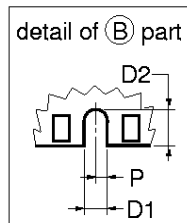
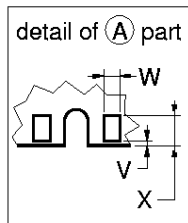
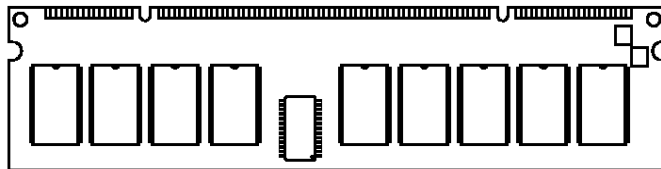
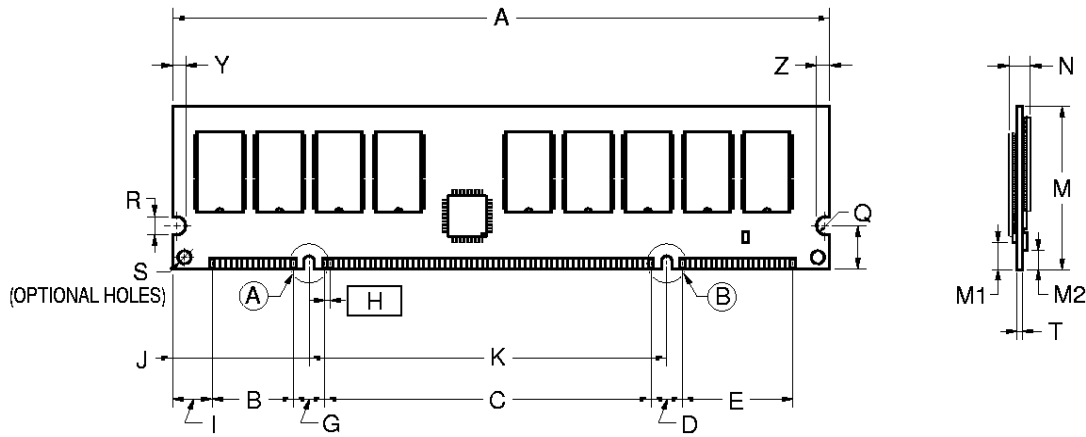
★ AC Parameters for Read Timing (Burst length = 2, /CAS latency = 2)



Remark All internal signals (A0 - A11, /CS0, /CS1, /CAS0, /CAS1, /RAS, /RAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

Package Drawing

200 PIN DUAL IN-LINE MODULE (SOKET TYPE)



ITEM	MILLIMETERS	INCHES
A	153.7±0.13	6.051 ^{+0.006} _{-0.005}
B	19.05	0.750
C	77.47	3.050
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	26.67	1.050
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.91	0.351
J	31.130	1.226
K	83.82	3.300
L	10.0	0.394
M	38.1±0.13	1.500±0.006
M1	5.78 MIN.	0.227 MIN.
M2	5.45 MIN.	0.214 MIN.
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.00±0.10	0.157 ^{+0.005} _{-0.004}
S	φ 3.0	φ 0.118
T	1.27±0.1	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS device must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.