Advance Information/
Preliminary Data

CA3218

T-77-07-09

TV Horizontal/Vertical Countdown Digital Sync System

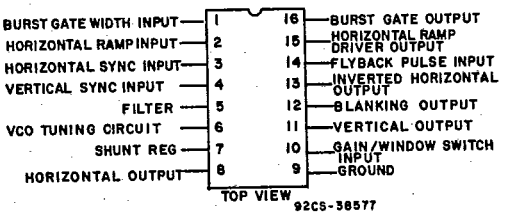
Features:
- *Horizontal oscillator*
- *Vertical countdown*
- *Composite blanking output*
- *Burst-gate output*
- *Horizontal ramp generator*
- *Internal shunt regulator*

The RCA - CA3218E* is a video sync system designed for use in television, monitor or video display products. The CA3218E contains a horizontal phase-locked oscillator and vertical countdown. It also features composite blanking and burst-gate outputs which, when externally summed, produce the sandcastle pulse necessary for the operation of most chroma/luma circuits.

The CA3218E is intended for use in 525-line systems and operates with standard or nonstandard input signals. An automatic mode-recognition circuit forces operation into the nonsynchronous mode for nonstandard sync input signals.

The CA3218E is supplied in a 16-lead dual-in-line plastic package (E suffix).

*Formerly RCA Developmental Type No. TA11419.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY CURRENT, PIN 7	50 mA
INPUT VOLTAGE (ALL INPUTS)	−1 V to V^+ + 1 V
DEVICE DISSIPATION:	
Up to T_A = 85°C	900 mW
Above T_A = 85°C	derate linearly 14 mW/°C
AMBIENT-TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

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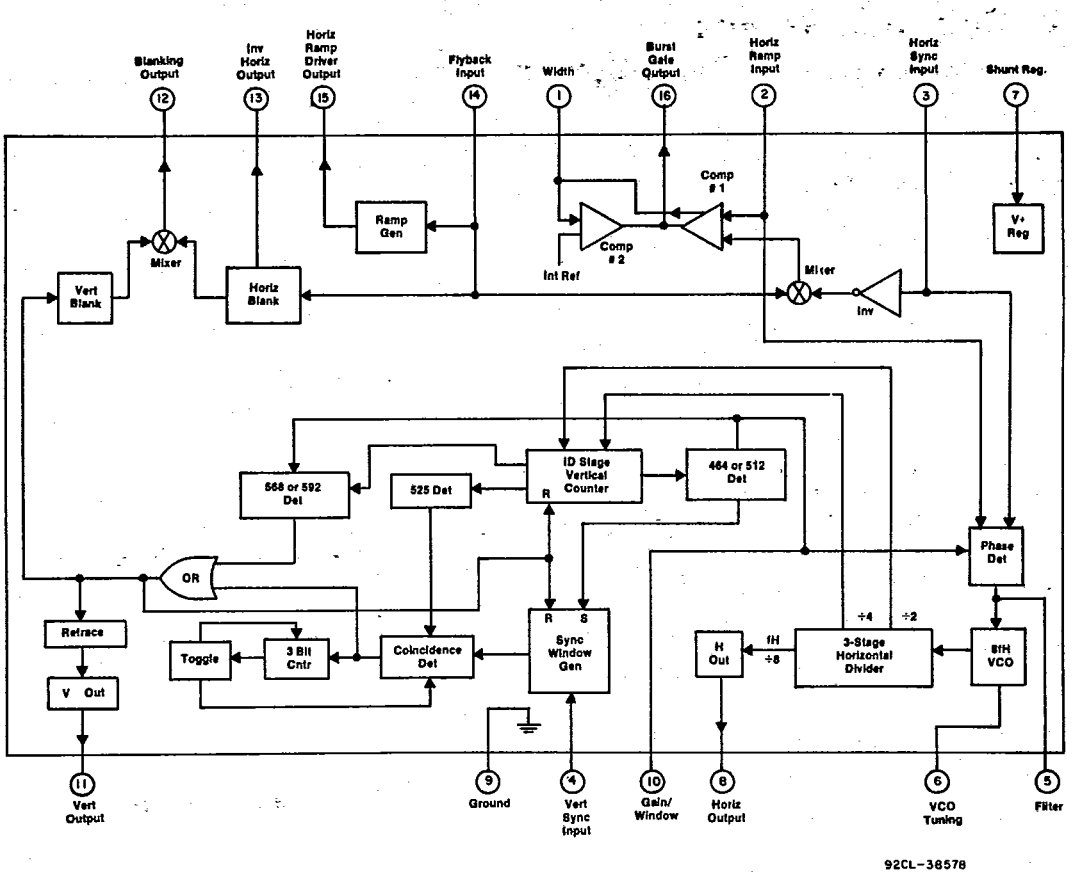

Fig. 1 - Functional block diagram.

CIRCUIT OPERATION (See Fig. 1)

The master oscillator operates at 8 times the horizontal rate, fH, as determined by the external LC connected between pins 5 and 6. The master oscillator is divided by 2, 4, and 8 and is then fed to the horizontal output amplifier and also to a 10-stage vertical countdown circuit. Horizontal AFC is performed by comparing the horizontal ramp input signal on pin 2, derived from the flyback pulse, to the horizontal sync signal on pin 3, producing a correction voltage. The correction voltage then is applied to the master oscillator to phase lock the system.

The divide by 2 and 4 outputs are used to drive a 10-stage counter for the vertical circuits. The use of the countdown system and associated logic circuits assures good noise immunity and the deletion of the vertical hold control.

The Gain/Window switch input on pin 10 is a logic input which controls the digital window in which the system looks for the occurrence of a vertical sync pulse; it also adjusts the phase detector gain for the two corresponding vertical windows. The 464th (Pin 10=Low) or the 512th (Pin 10=High) clock pulse (at 2fH) from the horizontal divider is used to set the start of the vertical sync window. The end of the sync window occurs at the 592nd (Pin 10=Low) or the 568th (Pin 10=High) clock pulse. If the incoming vertical sync pulse occurs regularly at the same time the 525th clock pulse occurs, it is used to generate the start of the vertical blanking and vertical sweep; the system is in the standard sync mode. If the incoming vertical sync pulse is absent (removed by noise, for example), the 10-stage counter will continue to provide an output pulse at the 525th clock pulse; a 3-bit counter will count the number of fields where no sync pulse occurred coincident with the 525th clock pulse. If no coincidence is detected in 8 sequential fields, the 3-bit counter energizes the toggle which shifts the mode of operation from standard sync to nonstandard sync.

In the nonstandard sync mode vertical scan is initiated by the incoming vertical sync pulse. Nonstandard sync operation results when the incoming vertical sync pulse occurs regularly within the vertical sync window; 464 to 592 counts (Pin 10=Low) or 512 to 568 counts (Pin 10=High) but not at the 525th count (Standard Sync Mode). In the nonstandard sync mode if no sync pulse is present, the system will free run at a frequency determined by the 592 (Pin 10=Low) or 568 (Pin 10=High) count.

The CA3218E generates a composite blanking signal and a burst-gate (key pulse) which, when summed externally, produce the sandcastle pulse necessary for the operation of most Chroma/Luminance integrated circuits. Also generated by the CA3218E is an inverted horizontal sync signal on pin 13 which can be used to drive the CA3224E Automatic Picture Tube Bias integrated circuit.

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Electrostatic Protection*
The SCR ESD-EOS protection structures used on the CA3218E are shown schematically in Fig. 6. These structures have proven to be highly effective enabling circuits to be protected in excess of 4 KV. The horizontal and vertical outputs (pins 8 and 11) are simply protected with internal diodes since their output transistors are large; these pins are also capable of withstanding 4 KV ESD. Although ESD-EOS protection is included in the CA3218E, proper circuit board layout and grounding techniques should be observed.

*For further information on CA3218E protection structures, refer to: "Using SCR's as Transient Protection Structures in Integrated Circuits", by L. R. Avery, RCA ICAN-7304 Reprint.

ELECTRICAL CHARACTERISTICS, AT +25 TO +70° C
TEST CONDITIONS SHOWN IN FIG. 3 UNLESS OTHERWISE SPECIFIED.

CHARACTERISTIC	PIN	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Supply Current	7	Adjust 24-V Supply for 7 V on Pin 7	7	—	14	mA
Regulator Voltage	7		7.4	—	8.6	V
Saturation Voltages						
Horiz. Output &	8		0	—	0.4	V
Inv. Horiz. Output	13		0	—	0.2	
Vert. Output	11		0	—	0.175	
Blanking Output &	12		0	—	0.08	
Burst Gate Output	16		15547	—	15854	Hz
Horiz. Ramp Output	15		-300	—	+300	Hz
Horiz. V_{co} Free-Running Frequency	8	No Sync Applied S1 = B	9.5	—	10.5	μs
Horiz. V_{co} Oscillator Pull-In	8	For 15734 ± 1 Hz	1140	—	1148	
Blanking Width			2.98	—	3.42	
Horizontal	12	Std NTSC Sync Applied	20	—	215	ns
Vertical	12	Std NTSC Sync Applied	31.4	—	32.1	μs
Burst Gate Width	16	Std NTSC Sync Applied	504	—	516	μs
Burst Gate Delay	16	From End of Horiz. Sync (Pin 3) To Start of Burst Gate (Pin 16)	—	10	—	V_{p-p}
Horiz. Pulse Width	8	Std NTSC Sync Applied	—	10	—	V_{p-p}
Vert. Pulse Width	11	Std NTSC Sync Applied				
Horiz. Sync Input	—					
Vert. Sync Input	—					

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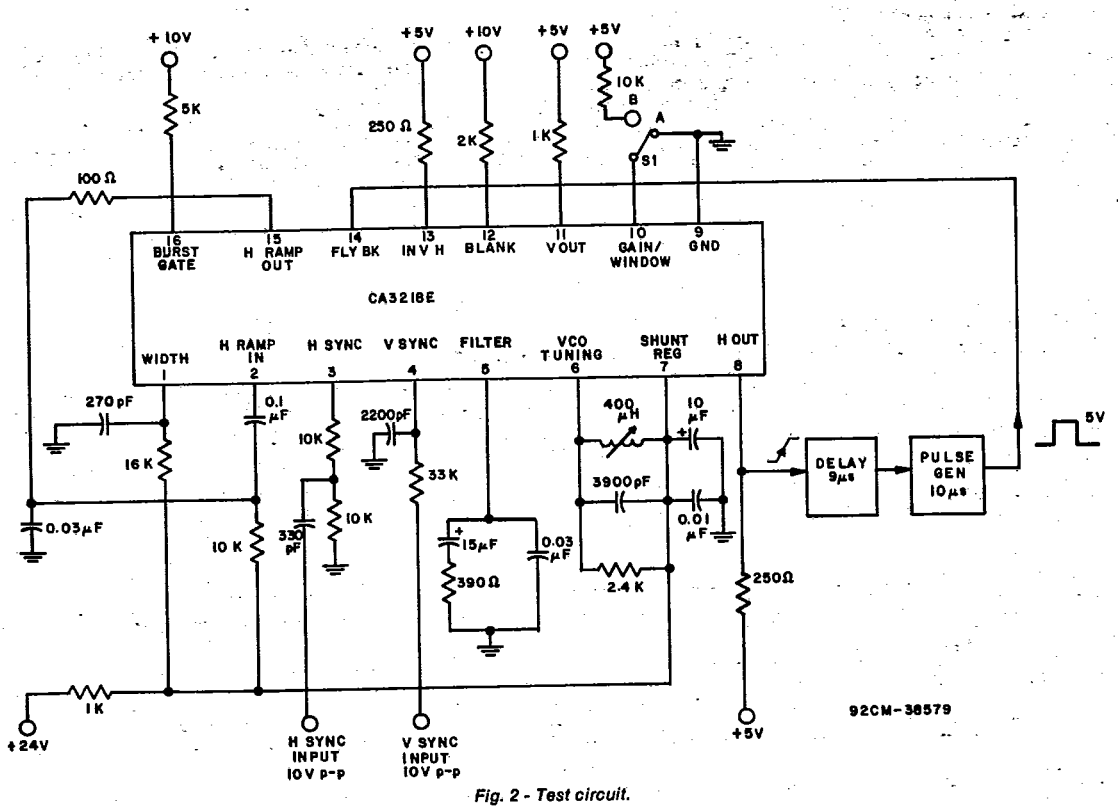

Fig. 2 - Test circuit.

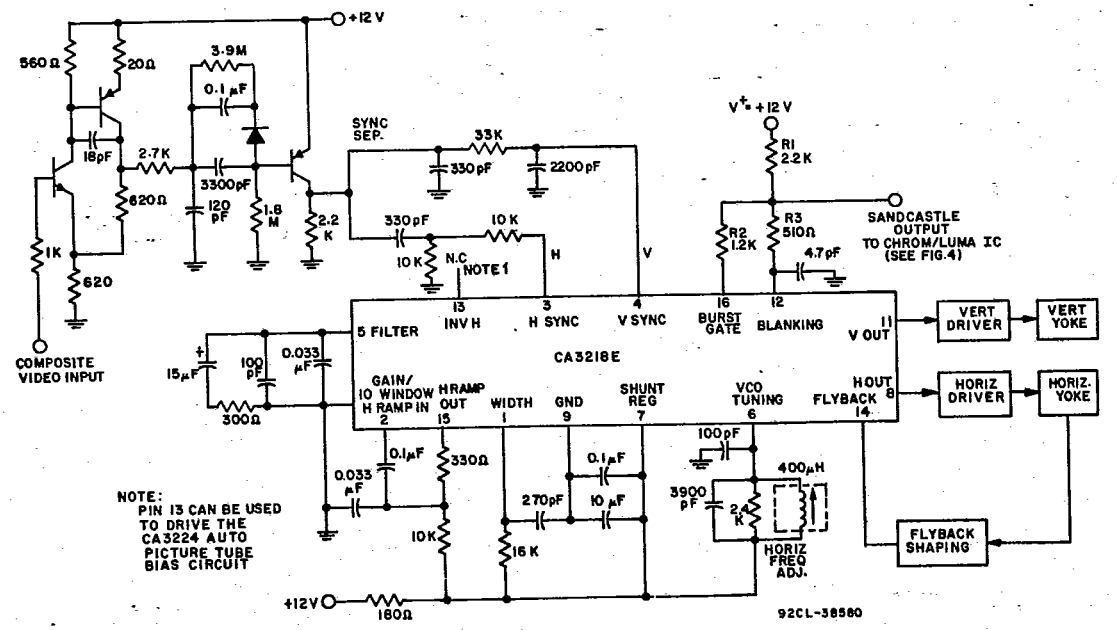

Fig. 3 - Typical application circuit.

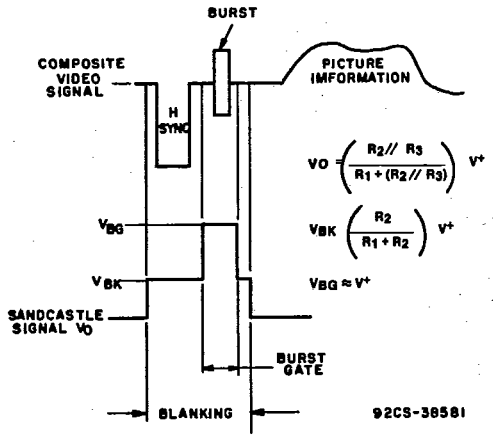

Fig. 4 - Sandcastle signal.

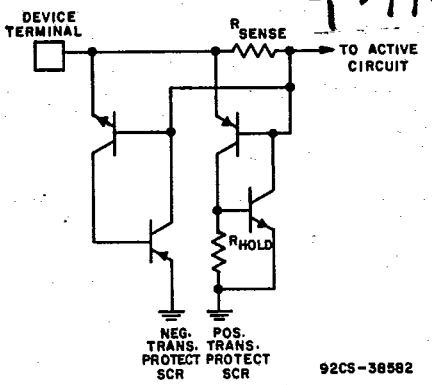

Fig. 5 - ESD protection structure.