ADC4355/ADC4356/ ADC4357

Low Noise, Low Distortion, High Speed, 16-Bit Sampling A/D Converters

Designed for High Performance Applications

Introduction

The Analogic ADC435X series of products consists of high speed, low noise, low distortion, 16-bit A/D converters. The ADC4355 and ADC4357 are sampling A/D converters that have throughput rates of 100 kHz and 200 kHz respectively; the ADC4356 is a 7 µs buffered A/D converter. Designed for high performance applications, they are pin-compatible to the industry standard Analogic MP2735A and AM40516 A/D converters. The ADC435X converters are ideally suited for applications where high speed, true 16-bit linearity, and excellent frequency domain features are a must, such as spectroscopy, professional digital audio, telecommunications, ATE, and medical imaging.

The ADC435X series features excellent differential nonlinearity of ±1/2 LSB, a low 35 µV rms noise, and optional bipolar or unipolar 10V input ranges. The ADC435X series utilizes a 3-pass subranging architecture that both minimizes parts count and yields unprecedented stability, linearity, and accuracy. To achieve its superior performance, the ADC435X relies on a proprietary reference D/A converter that has inherent 16-bit accuracy and linearity. Use of a CMOS flash A/D converter eliminates the –5V requirement, an inconvenience in most high speed 16-bit ADCs. With TTL and CMOS-compatibility, tri-state data outputs, self-contained reference and timing circuitry, the ADC435X series offers easy system integration conveniently packaged in a 3" x 4" fully shielded module.

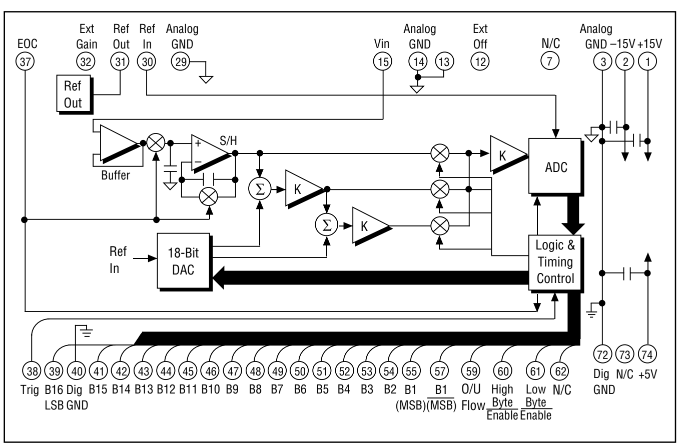
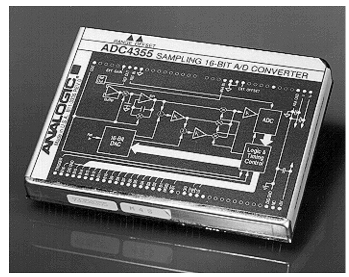


Figure 1. ADC4355/ADC4356/ADC4357 Functional Block Diagram and Pinout.



Features

- ❑ 16-Bit Resolution
- ❑ No Missing Codes
- ❑ Wide Dynamic Range: 96 dB
- ❑ Signal to Noise Ratio: 95 dB
- ❑ Peak Distortion: –110 dB (1 kHz)
- ❑ Total Harmonic Distortion: –103 dB (1 kHz)
- ❑ ±0.5 LSB Differential Non-Linearity
- ❑ 200 kHz Throughput Rate (ADC4357)
- ❑ 100 kHz Throughput Rate (ADC4355)
- ❑ Ease of Use
- ❑ Built-In S/H Amplifier (ADC4355/57)
- ❑ TTL Compatibility
- ❑ No –5V Requirement
- ❑ High Input Impedance
- ❑ Electromagnetic/Electrostatic Shielding

Applications

- ❑ Professional Audio Encoding
- ❑ Digital Telecommunications
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Spectroscopy
- ❑ Medical Data Acquisition
- ❑ Satellite Communications
- ❑ Multiplexed Data Acquisition

ADC4355/ADC4356/ ADC4357

***Specifications*[1]**

	ADC4355/ADC4356			ADC4357			
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
ANALOG INPUT							
Input Range [2]							
Unipolar	0		+10	0		+10	V
Bipolar	-5		+5	-5		+5	V
Input Bias Current		0.5 µA	2 µA		1 nA	50 nA	
Input Capacitance		10			10		pF
Input Resistance	100			100			MΩ
Max. Input without Damage		±Supplies			±Supplies		
DIGITAL INPUTS							
Logic Levels	LSTTL/CMOS-Compatible			LSTTL/CMOS-Compatible			
Logic "0"			0.8			0.8	V
Logic "1"	2.0			2.0			V
Trigger	Positive Edge Triggered			Positive Edge Triggered			
Loading			1			1	LSTTL
Pulse Width	50			50			ns
High Byte Enable	Active Low, B1-B8, $\overline{B1}$			Active Low, B1-B8, $\overline{B1}$			
Low Byte Enable	Active Low, B9-B16			Active Low, B9-B16			
Propagation Delay with 1 TTL Load		20	50		20	50	ns
DIGITAL OUTPUTS							
Logic Levels							
Logic "0"			+0.4			+0.4	V
Logic "1"	+2.4			+2.4			V
Fan-Out			1			0.1	TTL Load
Output Coding	Binary Offset, Binary, Two's Complement, Complementary Data (see ordering guide)			Binary Offset, Binary, Two's Complement Complementary Data (see ordering guide)			
End of Conversion (EOC)	High during conversion, data valid 10 ns min. prior to falling edge			High during conversion, data valid 10 ns min. prior to falling edge			
Over/Under Flow	Active high at ±FS, not tri-stateable			Active high at ±FS, not tri-stateable			
REFERENCE							
Voltage Output		-6.5			–6.5		V
Load [3]			1			1	mA
Input Loading							
±5V Input	720Ω // 10 µF, -1.5 mA typ.			720Ω // 10 µF, -1.5 mA typ.			
0V to +10V Input	607Ω // 10 µF, -3.5 mA typ.			607Ω // 10 µF, -3.5 mA typ.			
Max Input W/O Damage	+0.5		-8.5	+0.5		-8.5	V
DYNAMIC CHARACTERISTICS							
Maximum Throughput Rate	100			200			kHz
A/D Conversion Time	7				4		µs
S/H Acquisition Time		3			1		µs
S/H Aperture Delay		30	60		30	60	ns
S/H Aper. Jitter		200	400		100	200	ps RMS
S/H Feedthrough [4]		-96	-90		-96	-90	dB
Sig. to Noise Ratio [5]	92	95		86	90		dB
Peak Distortion [6]							
±5V Input @ 1 kHz		-110	-100				dB
±5V Input @ 10 kHz					-100	-95	dB
±5V Input @ 20 kHz		-105	-96				dB
±5V Input @ 80 kHz					-90		dB
Total Harm. Dist. [7]							
±5V Input @ 1 kHz		-103	-94				dB
±5V Input @ 10 kHz					-94	-88	dB
±5V Input @ 20 kHz		-100	-94				dB
±5V Input @ 80 kHz					-87		dB

	ADC4355/ADC4356			ADC4357			
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
TRANSFER CHARACTERISTICS							
Resolution	16			16			Bits
Quantization Error			±0.5			±0.5	LSB
Int. Nonlinearity			±0.003			±0.003	% FSR
Diff. Nonlinearity		±0.25	±0.5		±0.5	±0.75	LSB
No Missing Codes	Guaranteed from 0°C to 60°C			Guaranteed from 0°C to 60°C			
Offset Error (8)			±1			±1	mV
Gain Error (8)			±0.01			±0.01	% FSR
Noise							
ADC4355		35					µV rms
ADC4356		25					µV rms
ADC4357					60		µV rms
External Offset Adjust		7.6			7.6		mV/V
External Gain Adjust		3.3			3.3		mV/V
STABILITY (0°C T0 60°C)							
Differential Nonlinearity			±0.5			±0.5	ppm /°C
Offset Voltage			±10			±10	ppm FSR/°C
Gain			±10			±10	ppm FSR/°C
Warm-Up Time			5			5	Mins.
Supply Rejection							
Offset		±5	±10		±5	±10	ppm FSR/%
Gain		±5	±10		±5	±10	ppm FSR/%
POWER REQUIREMENTS (10)							
±15V Supplies (9)	±11.65		±15.45	±11.65		±15.45	V
+5V Supply	+4.75		+5.25	+4.75		+5.25	V
±15V Current Drain							
ADC4355		58					mA
ADC4356		51					mA
ADC4357					62		mA
+5V Current Drain		55			55		mA
Power Consumption							
ADC4355		2.0					W
ADC4356		1.8					W
ADC4357					2.2		W
ENVIRONMENTAL & MECHANICAL							
Temperature Range							
Rated Performance	0		60	0		60	°C
Storage	-25		80	-25		80	°C
Relative Humidity							
Non-condensing	0 to 85 % up to 60°C			0 to 85 % up to 60°C			
	Dimensions 3" x 4" x 0.44"			Dimensions 3" x 4" x 0.44"			
	(76.2 x 127 x 11.18 mm)			(76.2 x 127 x 11.18 mm)			
Shielding	Electromagnetic 5 Sides			Electromagnetic 5 Sides			
	Electrostatic 6 Sides			Electrostatic 6 Sides			
Case Potential	Ground			Ground			

NOTES:

1. Unless otherwise noted, all specifications apply at 25°C and power supplies are ±15V and +5V.
2. See ordering guide for factory-set input ranges.
3. Reference load must remain constant during conversion. DC load 1mA max.
4. Measured with a 20 kHz full scale sine wave input.
5. Signal-to-Noise Ratio represents the ratio between the rms value of the signal and the total rms noise below the Nyquist Rate. The total rms noise is computed by: (l) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonically related frequency bins; and (3) computing the rms noise from the sum of (l) and (2).
6. Peak Distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the signal. Note that in computing Peak Distortion, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 5.
7. Total Harmonic Distortion represents the ratio between the rms sum of all harmonics up to the 100th harmonic and the rms value of the signal. Note that in computing THD, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 5.
8. Externally adjustable to zero.
9. For the 0V to +10V input voltage range, the minimum analog supply voltage is ±14.55V.
10. Analogic highly recommends the use of linear power supplies with its high performance, high resolution A/D converters. However, if system requirements provide only a +5V supply and limited space, the use of the Analogic SP7015 DC-to-DC converter will provide a low noise solution which will not degrade the ADC4355/ADC4356/ADC4357 performance.

Specifications subject to change without notice.

SPECIFICATIONS

Output Coding and Trim Procedure

Figure 2 shows the output coding of the ADC435X A/D converter. The symbol * in Figure 2 indicates a bit that is undergoing a 0/1 or 1/0 code transition at the indicated analog input voltage.

To trim the offset of the ADC435X, apply 76 µV to the analog input. Adjust the offset trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

To trim the gain of the ADC435X apply +4.999924V for the bipolar option or +9.999772V for the unipolar option. Adjust the gain trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

In addition to the internal offset and gain potentiometers, provisions have been made to externally null out DC errors by use of potentiometers or DACs. A 10V swing from a DAC on Pin 12 produces a 33 mV offset shift; a 10V swing on Pin 32 produces a 76 mV gain shift.

Timing Considerations

The timing diagram of Figure 3 shows the timing characteristics of the ADC435X A/D converter. Numbers in parentheses are figures for the ADC4357. Upon a low-to-high transition of the trigger input, the end of conversion (EOC) line also switches high. The EOC line in turn switches the internal sample-and-hold amplifier to the Hold mode; the S/H amplifier remains in the Hold mode for the duration of the A/D conversion period. At the end of the 7 µs (4 µs) A/D conversion period, the EOC line goes low and switches the sample-and-hold amplifier to the Sample mode. At the 100 kHz (200 kHz) throughput rate shown in Figure 3, the sample-and-hold amplifier then has 3 µs (1 µs) to sample (acquire) a new signal level for the next conversion cycle. The TTL-level Trigger input should have a minimum pulse width of 50 ns. Note that the data for a given conversion cycle becomes valid approximately 10 ns prior to the high-to-low transition of the EOC line.

Layout Considerations

Because of the extremely high resolution of the ADC435X A/D converter, it is necessary to pay careful attention to the printed circuit layout for the device. It is, for example, important to separate the analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or

TRUTH TABLE

INPUT VOLTAGE	DIGITAL OUTPUTS	
	COMP. OFFSET BINARY	STRAIGHT OFFSET BINARY
	MSB LSB	MSB LSB
BIPOLAR		
5.000000V	0000000000000000	OVERFLOW
4.999924V	000000000000000*	OVERFLOW
4.999848V	0000000000000001	1111111111111111
+0.000152V	0111111111111111	1000000000000001
+0.000076V	****************	100000000000000*
0.000000V	1000000000000000	1000000000000000
-4.999695V	1111111111111110	0000000000000010
-4.999771V	111111111111111*	00000000000000**
-4.999848V	1111111111111111	0000000000000001
-5.000000V	OVERFLOW	0000000000000000
UNIPOLAR		
9.999848V	0000000000000000	1111111111111111
9.999772V	000000000000000*	111111111111111*
9.999695V	0000000000000001	1111111111111110
5.000000V	0111111111111111	1000000000000000
4.999924V	****************	****************
4.999848V	1000000000000000	0111111111111111
0.000152V	1111111111111110	0000000000000001
0.000076V	111111111111111*	000000000000000*
0.000000V	1111111111111111	0000000000000000

Figure 2. Output coding for the ADC435X.

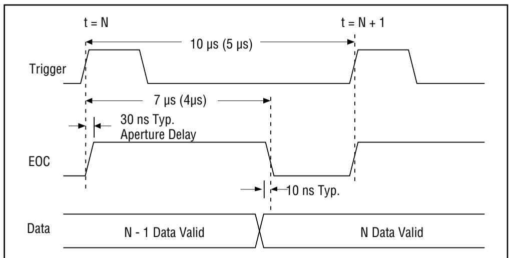


Figure 3. ADC435X Timing Diagram.

"glitchy", and these glitches can have adverse effects on the performance of a 16-bit A/D converter if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution the size of the voltage step between one code transition and the succeeding one is only 153 µV, so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed circuit board. Note that the ground-potential metal case used for the ADC435X provides shielding against electromagnetic interference on five sides and against electrostatic interference on six sides.

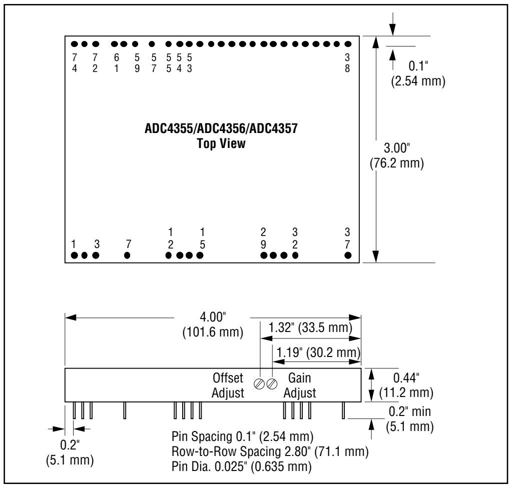


Figure 4. ADC435X Outline Drawing & Pinouts.

Principles of Operation

To understand the operating principles of the ADC435X A/D converter, refer to Figure 5. The simplified block diagrams in Paths a, b, and c in Figure 5 illustrate the three successive passes in the sub-ranging conversion scheme of the ADC435X. For all three passes, the lines labeled “From Input” come either from the output of the sample-and-hold amplifier (in the ADC4355/ADC4357) or from the output of the input buffer amplifier (in the ADC4356). In the first pass (a), a switched-gain amplifier attenuates the input signal by a factor of five. It thus converts the 10V full-scale range of the input to the 2V full-scale range of the 6-bit flash A/D converter. The 6-bit A/D converter then digitizes the six MSBs of the input signal. The outputs of the A/D converter drive the six MSBs of the D/A converter. Although not shown (for reasons of clarity) in Figure 5, the six output lines of the A/D converter are actually latched into the logic circuitry of a specialized gate array that drives the input lines of the D/A converter.

In the second pass (b), a difference amplifier subtracts the D/A converter’s output voltage from the input voltage, then amplifies this difference by a factor of 3.2. The switched-gain amplifier now has a gain of two, and thus amplifies the difference voltage further. The output of the switched-gain amplifier again provides the input signal for the 6-bit flash A/D converter. The A/D converter’s outputs are latched into the gate array that supplies the next lower-order bits of the D/A converter. In the gate array, the A/D converter's MSB in the second pass “overlaps” the LSB from the first pass. The resolution of the A/D conversion in the second pass is thus 11 bits (not 12) .

In the third pass (c), the gain of 3.2 difference amplifier subtracts the D/A converter’s output voltage from the input voltage. In this pass, an amplifier with a gain of 32 provides additional amplification of the difference signal. The six outputs of the 6-bit flash A/D converter are latched into the gate array; the MSB of this conversion cycle "overlaps" the LSB of the previous cycle. The effective resolution of the conversion is thus 5 + 5 + 6, or 16 bits. Using the “overlap” structure, logic circuitry in the gate array adds the digital words produced in the three passes and produces the corrected output word. This digital error-correction technique thus provides an output word that is accurate and linear to within the full resolution of the A/D converter. The

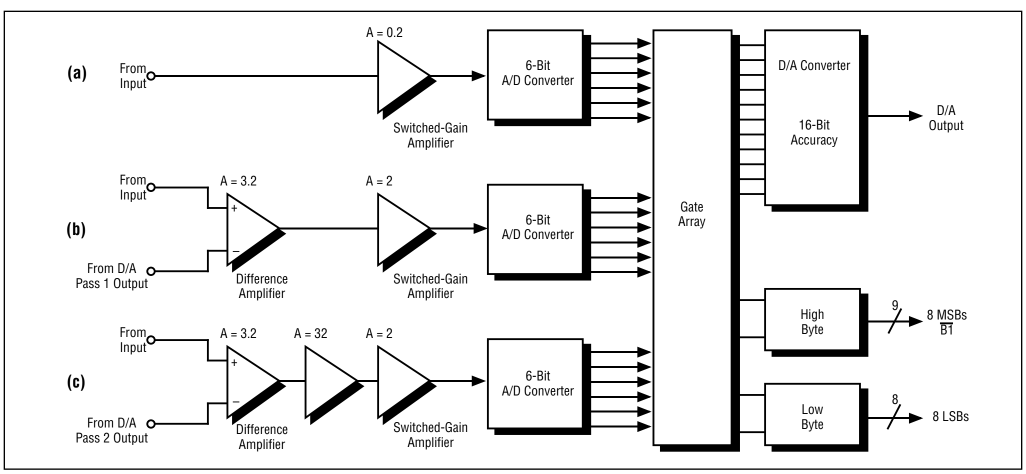


Figure 5. Operating Principle of the ADC435X.

method helps to compensate for any gain and linearity errors in the amplifying circuitry as well as in the 6-bit flash A/D converter. Without the error-correction technique, it would be necessary that all the components in the ADC435X — the difference amplifier, the switched-gain amplifier, and the 6-bit flash A/D converter — be accurate and linear to a 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it clearly would be impractical to achieve in production. The key to the ADC435X's conversion scheme is the 16-bit-linear D/A converter, which serves as a reference element for the conversion passes as well as for the error-correction mechanism.

The ADC435X has a tri-state output structure. Users can enable the eight MSBs, eight LSBs, or both by using the High-Byte Enable and Low-Byte Enable pins (both pins are active low). This feature makes it possible to transfer data from the ADC435X to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered (see Figure 6).

Typical Application

Figure 6 shows a typical application circuit for the ADC4356 16-bit A/D converter. This circuit provides simultaneous sampling of eight bipolar analog-input channels. Simultaneous sampling is a necessity in conversion systems in which the phase, as well as amplitude, relationship between different signals is an important parameter. One example is in seismic measurements, in which it is crucial to know the phase relationship between the signals generated by different sensors. This application circuit performs simultaneous sampling by "freezing" the signal levels of eight analog-input channels at the same instant of time. The differential multiplexer then presents these signal levels, either sequentially or in any user-programmed order, to the ADC4356 A/D converter via a differential amplifier. Although the input signals to this circuit are essentially single-ended, the use of a differential multiplexer and a differential amplifier eliminates the possibility of errors arising from common mode voltages.

The minicomputer or microprocessor in Figure 6 provides the sequence and timing information to the control logic. The control logic then performs the task of switching the sample-and-hold amplifiers from Sample to Hold mode and vice-versa, selecting the appropriate input channel and triggering the ADC4356 A/D converter. By using two resistors with each SHA2410 sample-and-hold amplifier, a user can program the SHA2410s to provide the gain required to match the input signals to the ±5V full-scale range of the ADC4356 A/D converter. In the application circuit of Figure 6, for example, the four inputs shown have full-scale ranges of ±1, ±2, ±3, and ±5V. The eighth input channel has the proper full-scale range of ±5V, so gain-setting resistors are not required. Because the SHA2410s provide the sample-and-hold function in this circuit, the ADC4356, which does not include a sample-and-hold amplifier, is an appropriate choice.

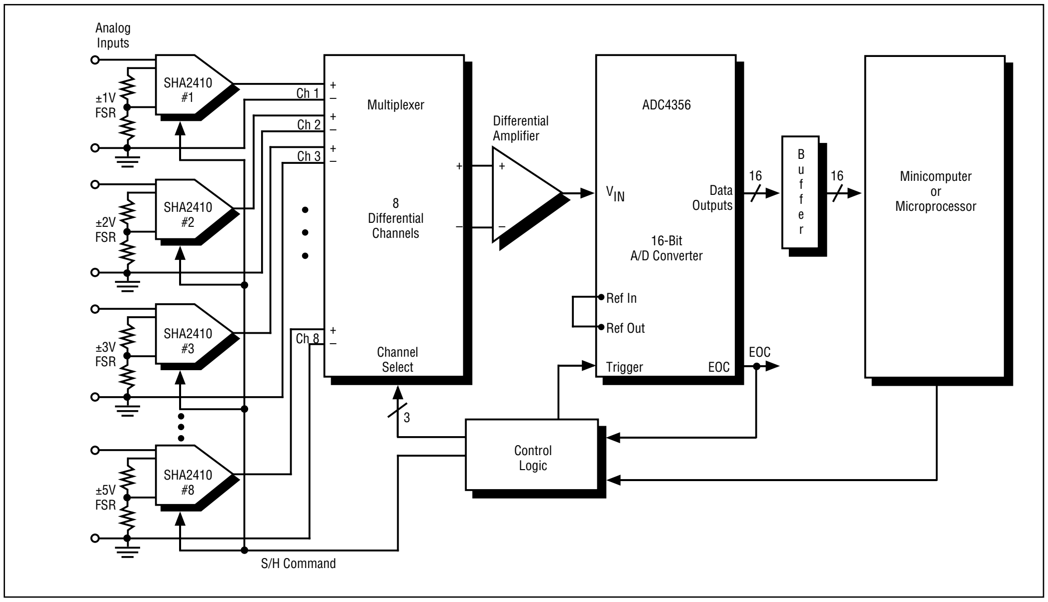


Figure 6. Typical Application Circuit for the ADC4356.

Ordering Guide

ADC435_-M__

5	100 kHz Sampling	
6	7 µs Buffered A/D Converter	
7	200 kHz Sampling ADC	
1	0V to +10V Input	
4	±5V Input	
S	Straight Data	
C	Complementary Data	

DC-to-DC Converter **SP7015**