DS3572-2.2

MA31755

16-BIT FEEDTHROUGH ERROR DETECTION & CORRECTION UNIT (EDAC)

The MA31755 is a 16 bit Error Detection and Correction Unit intended for use in high integrity systems for monitoring and correcting data values retrieved from memory. The EDAC is placed in the data bus between the processor and the memory to be protected. Extra check bits added at each memory location are programmed transparently by the EDAC during a processor write cycle. The entire checkword and data combination is verified on read cycles. If any one bit in the incoming data stream is at fault the EDAC can correct the fault transparently, presenting the corrected 16-bit value to the processor. An error in two bits can be detected but cannot be corrected. Both the correctable and uncorrectable error conditions are signalled to the system to allow the processor to take action as required. Parity is passed through the device unchanged as data bus bit 16.

Tri-statable bus transceivers with a high drive capability are incorporated at the MD and CB busses which allows the usual bus driver devices to be removed and reduces the overall timing overhead imposed on the data bus. Although designed primarily for MA31750 application, this part may be used in almost any 16-bit processor system requiring high data integrity.

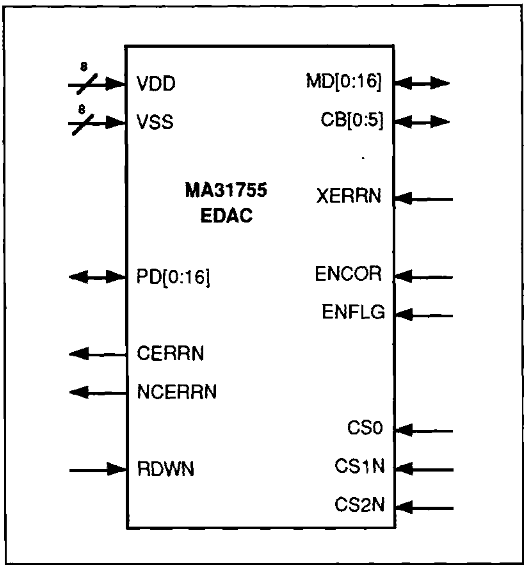


Figure 1: Chip Signals

FEATURES

- Fast Feedthrough (35ns Detect and Correct Cycle)
- 16-Bit Operation with 6 Check Bits
- Radiation Hard CMOS/SOS Technology
- Feedthrough Operation
- Error Corrected/Uncorrected Flags
- High Drive Capability on Memory Busses

1. PIN DESCRIPTIONS

POWER

VDD x8	Input	-	Supply - 5V nominal (all must be connected)
VSS x8	Input	-	Circuit 0V reference (all must be connected)

BUSSES

PD[0:16]	I/O	Active High	Processor data bus + parity bit (bit 16)
MD[0:16]	I/O	Active High	Memory data bus + parity bit (bit 16)
CB[0:5]	I/O	Active High	Memory check bit bus

ERROR FLAGS AND CONTROL

CERRN	Output	Active Low	Asserted low when a correctable (1 bit) error occurs (ENFLG must be asserted high)
NCERRN	Output	Active Low	Asserted low when an uncorrectable error occurs (ENFLG must be asserted high)
XERRN	Input	Active Low	External error feedthrough to NCERRN line.
ENCOR	Input	Active High	Enables correction of data when high. Data is passed through uncorrected when this line is low.
ENFLG	Input	Active High	Enables the flagging of incorrect data when high. When this line is low the two error flag lines are held inactive.

DEVICE AND BUFFER CONTROL

CS2N	Input	Active Low	Enables device and output buffers.
CS1N	Input	Active Low	Enables device and output buffers.
CS0	Input	Active High	Enables device and output buffers.
RDWN	Input	-	High indicates a read cycle, low indicates a write cycle.

2. FUNCTIONAL DESCRIPTION

2.0 GENERAL

The EDAC is of feedthrough type with 16 data bits, 1 parity bit and 6 check bits, giving the ability to correct all single bit errors and detect all double bit errors. Errors in more than two bits may result in any combination of error flags being raised and the data may be arbitrarily modified by the correction circuitry.

The EDAC is placed in the data bus between the processor and the memory to be protected. It forms the interface between the 23-bit memory bus and the 17-bit processor bus. Tri-statable bus transceivers with a high drive capability are incorporated at both busses.

2.1 TESTING THE EDAC AND MEMORY SYSTEM

No specific hardware for testing is provided by the MA31755 since this would compromise the speed performance of the part in normal operation. However, it is possible to fully test the EDAC function and the generation of the error signals without this. The system should provide a means by which the check bit memory may be dynamically write-enabled and disabled - this may be provided by gating write strobe on the check bit memory with a latched control bit. By writing first with check bits enabled, then with them disabled, suitable seed values may be constructed which have the required pattern of bits to test each feature of the EDAC operation. A similar approach may be taken when testing the check bit memory.

By disabling the EDAC (asserting ENCOR low) the processor may have direct access to the unmodified 17-bit data from the memory. Suitable test patterns may be applied to test each memory location as required.

2.2 BUS CONTROL

There are four signals which control the drive status of the EDAC external busses: RDWN, CS2N, CS1N and CS0. The relationship to each other and to the EDAC busses is shown in Figure 2 below. The timing of these signals is shown in Figures 6 and 7.

RDWN	CS2N	CS1N	CS0	Bus state	
				Processor	**Memory**
X	High	X	X	Tristate	Tristate
X	X	High	X	Tristate	Tristate
X	X	X	Low	Tristate	Tristate
High	Low	Low	High	Output	Input
Low	Low	Low	High	Input	Output

Figure 2: Bus Control

2.3 INTERNAL OPERATION

2.3.1 Check Bit Generation

On write cycles the processor data word, PD[0:15], and the processor parity bit ,PD[16], are passed directly to the memory data bus, MD[0:15], and the memory parity bit, MD[16].

The check bits, CB[0:5], are derived by 6 parity generators operating on sets of 8 bits of the processor data word, PD[0:15], as shown in Figure 3 below:

CB	Parity	PD															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Even			X	X				X	X	X	X	X				X
1	Even		X			X	X	X	X		X		X			X	
2	Odd	X			X			X				X		X	X	X	X
3	Odd		X	X			X						X	X	X	X	X
4	Even	X				X	X	X	X	X		X			X		
5	Even	X	X	X	X	X				X	X			X			

Figure 3: Check Bit Generation

2.3.2 Syndrome Generation

The syndrome generation logic checks the sense of the check bits with respect to the memory data word. Six 9-input parity checkers generate the syndrome bits, SY[0:5], according to figure 4 below:

SY	Parity	MD																CB					
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0	1	2	3	4	5
0	Even			X	X				X	X	X	X	X				X	X					
1	Even		X			X	X	X	X		X		X			X			X				
2	Odd	X			X			X				X		X	X	X	X			X			
3	Odd		X	X			X						X	X	X	X	X				X		
4	Even	X				X	X	X	X	X		X			X							X	
5	Even	X	X	X	X	X				X	X			X									X

Figure 4: Syndrome Generation

If there are no errors in the memory data word, MD[0:15], or the check bits, CB[0:5], then all of the syndrome bits, SY[0:5], will be set low.

A single bit error in the memory data word, MD[0:15], will cause 3 syndrome bits to be set high. However, a single bit error in the check bits, CB[0:5], will cause only 1 syndrome bit to be set high. A two bit error in the memory data word and/or the check bits will cause either 2, 4, 5 or 6 syndrome bits to be set.

Three or more errors in the memory data word and/or the check bits will cause an undefined number of syndrome bits to be set. This will cause the operation of the device in respect of the states of CERRN, NCERRN and data on the PD bus to be unpredictable.

2.3.3 Correction

With no syndrome bits set data will pass through from the MD bus to the PD bus unchanged. When a single bit error occurs in the memory data word, MD[0:15], the three syndrome bits which are set identify which data bit is in error. The correction logic decodes these syndrome bits and will correct the error provided the correction enable input, ENCOR, is high.

2.3.4 Flag Generation

The correctable error flag,CERRN, is driven low whenever 1 or 3 syndrome bits are set and flags are enabled (ENFLG=1).

The non-correctable error flag, NCERRN, is driven low whenever 2, 4, 5 or 6 Syndrome bits are set and flags are again enabled (ENFLG=1). NCERRN will also be driven low should the external error input, XERRN, be driven low at any time. Note: this external error feedthrough from XERRN to NCERRN operates independently of ENFLG and the Chip Select inputs (CS0, CS1N & CS2N).

Flags are enabled provided the ENFLG input is high and the device is selected. Note: the flags are not disabled on write cycles and therefore can indicate errors on write operations caused by faults on the Memory Data Bus and the Check Bit Bus.

2.3.5 Internal Structure

Figure 5 below shows the internal block diagram representing the internal architecture of the MA31755.

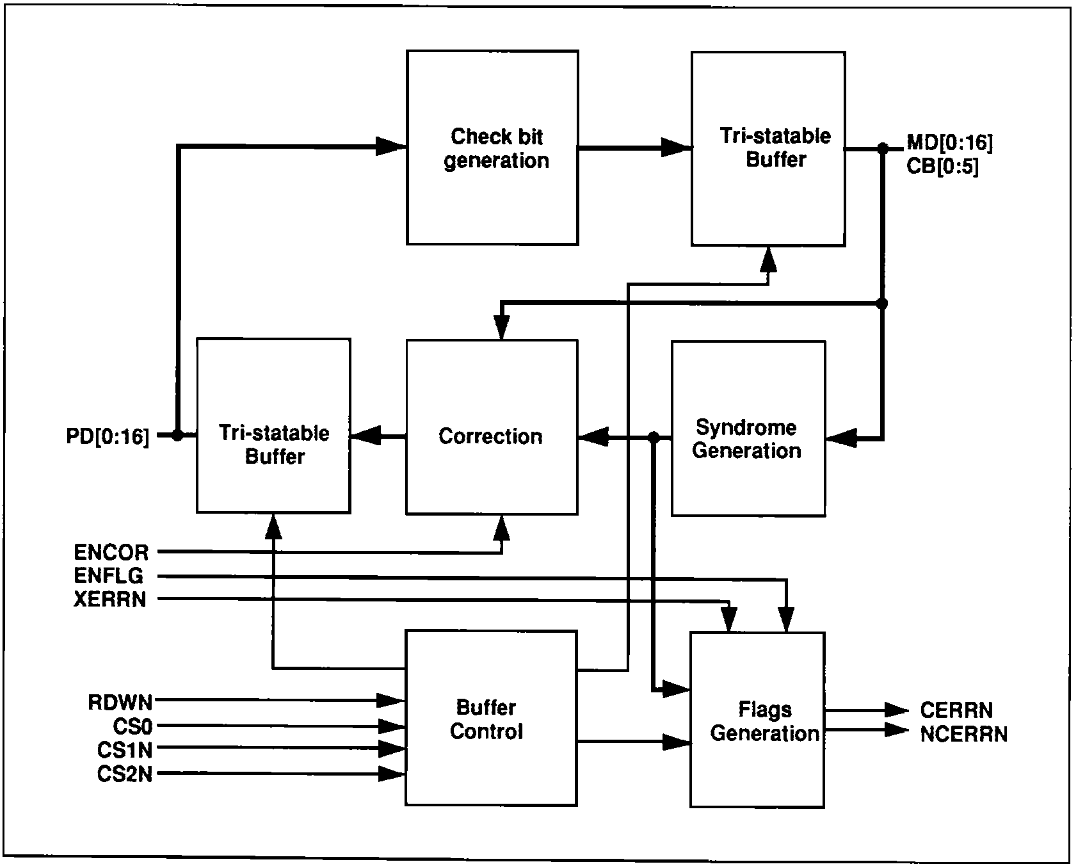


Figure 5: Block Diagram of the Internal Architecture of the MA31755

3. TIMING DIAGRAMS

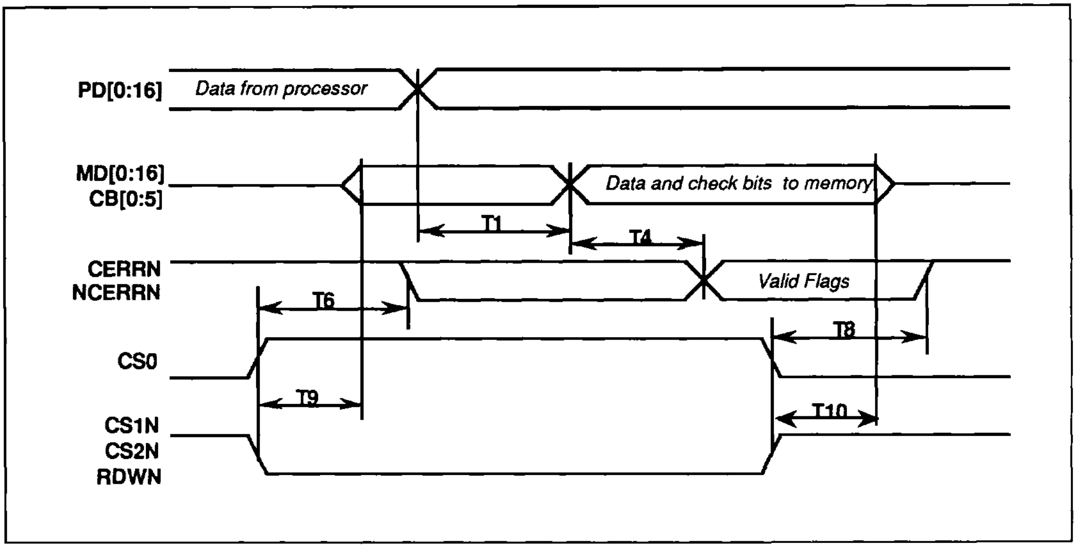


Figure 6 : Processor Write Timings (ENFLG = 1)

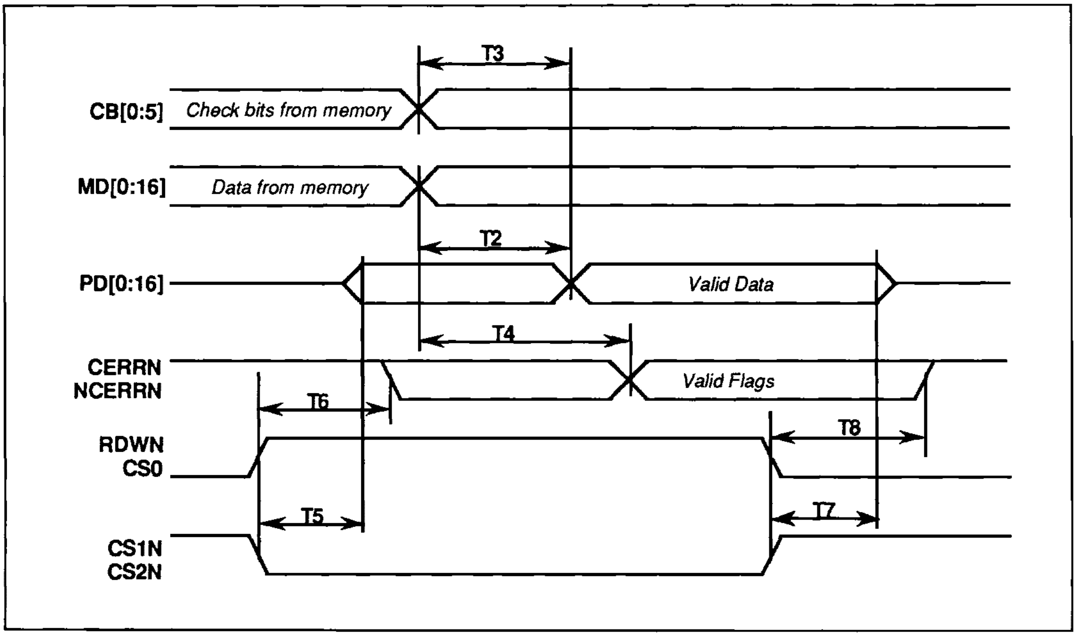


Figure 7: Processor Read Timings (ENCOR and ENFLG=1)

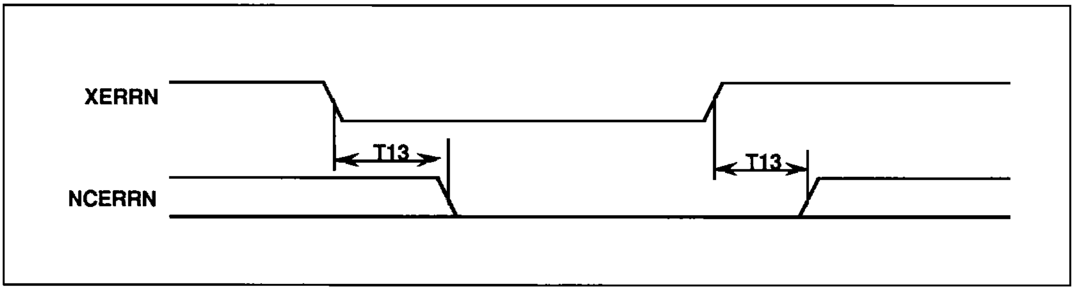


Figure 8: External Error Feedthrough Timing (ENFLG=X ,CS0=X, CS1N /CS2N=X)

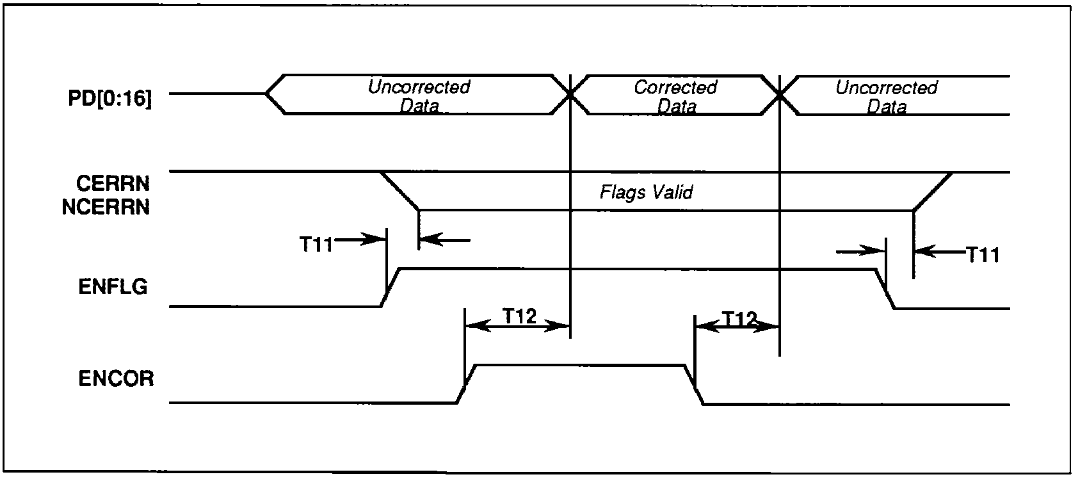


Figure 9: Correction and Error flag enable/disable timings (CS0=1, CS1N/CS2N = 0)

4. AC CHARACTERISTICS

Parameter	Description	Min	Max	Units	Notes
T1	PD[0:16] to MD[0:16] , CB[0:5] valid	-	25	ns	CL = 150pF
T2	MD[0:16] to PD[0:16] valid	-	30	ns	CL = 50pF
T3	CB[0:5] to PD[0:16] valid	-	35	ns	CL = 50pF
T4	MD[0:16] to CERRN and NCERRN valid CB[0:5] to CERRN and NCERRN valid	-	40	ns	CL = 50pF
T5	RDWN, CS0 rising to PD[0:16] driven (processor read) CS1N, CS2N falling to PD[0:16] driven (processor read)	5	20	ns	CL = 50pF
T6	CS0 rising to error flags changing CS1N, CS2N falling to error flags changing	-	25	ns	CL = 50pF
T7	RDWN, CS0 falling to PD[0:16] Hi-Z CS1N,CS2N rising to PD[0:16] Hi-Z	-	30	ns	CL = 50pF
T8	CS0 falling to error flags high CS1N, CS2N rising to error flags high	-	25	ns	CL = 50pF
T9	RDWN, CS1N and CS2N falling to MD[0:16] and CB[0:5] driven (processor write) CS0 rising to MD[0:16] and CB[0:5] driven (processor write)	5	20	ns	CL = 150pF
T10	CS0 falling to MD[0:16] and CB[0:5] Hi-Z RDWN, CS1N, CS2N rising to MD[0:16] and CB[0:5] Hi-Z	5	25	ns	CL = 150pF
T11	ENFLG to CERRN and NCERRN valid	-	20	ns	CL = 50pF
T12	ENCOR to PD[0:16] valid	-	20	ns	CL = 50pF
T13	XERRN to NCERRN valid	-	10	ns	CL = 50pF

Mil-Std-883, method 5005, subgroups 9, 10, 11

Figure 10: Timing Parameters

5. DC CHARACTERISTICS AND RATINGS

Symbol	Description	Min.	Max.	Units
VDD	Supply voltage	-0.5	7	V
VI	Input voltage	-0.3	VDD+0.3	V
TA	Operating temperature	-55	+125	°C
TS	Storage temperature	-65	+150	°C

Figure 11: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Description	Min	Max	Unit	Notes
VOH	Output high voltage	Vdd- 0.5	-	V	IOH = 15mA on MD[0:16] / CB[0:5] IOH = 5mA on other outputs.
VOL	Output low voltage	-	Vss+0.5	V	IOL = -15mA on MD[0:16] / CB[0:5] IOL = -5mA on other outputs.
VIH	Input high voltage	Vdd-1.5	-	V	
VIL	Input low voltage	-	Vss+1.5	V	
IIL, IIH (Note 1)	Input current high/low	-	10	uA	
IOZ (Note 1)	Output tri-state leakage	-	0.1	mA	VO = 0 to VDD
ISS	Standby current	-	10	mA	
IDD	Operating current	-	100	mA	

Conditions VDD = 4.5 to 5.5V, TA = -55 to +125°C

Mil-Std-883, method 5005, subgroups 1, 2, 3

Note 1: Worst case at TA = +125°C, guaranteed but not tested at TA = -55°C.

Figure 12: Operating Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 12 at +25°C
2	Static characteristics specified in Figure 12 at +125°C
3	Static characteristics specified in Figure 12 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figure 10 at +25°C
10	Switching characteristics specified in Figure 10 at +125°C
11	Switching characteristics specified in Figure 10 at -55°C

Figure 13: Definition of Subgroups

6. APPLICATIONS INFORMATION

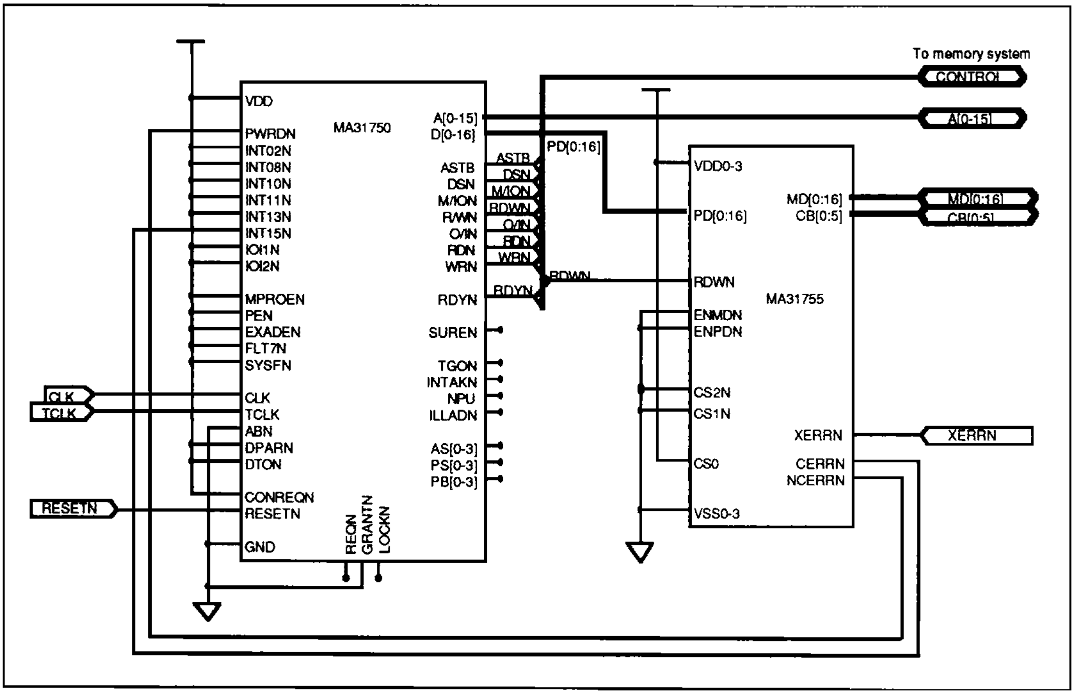


Figure 14: Basic System Diagram for the MA31755 with the MA31750

7. PACKAGING

The device will be supplied in a 68-pin PGA for development with a 68-pin flatpack option for flight parts.

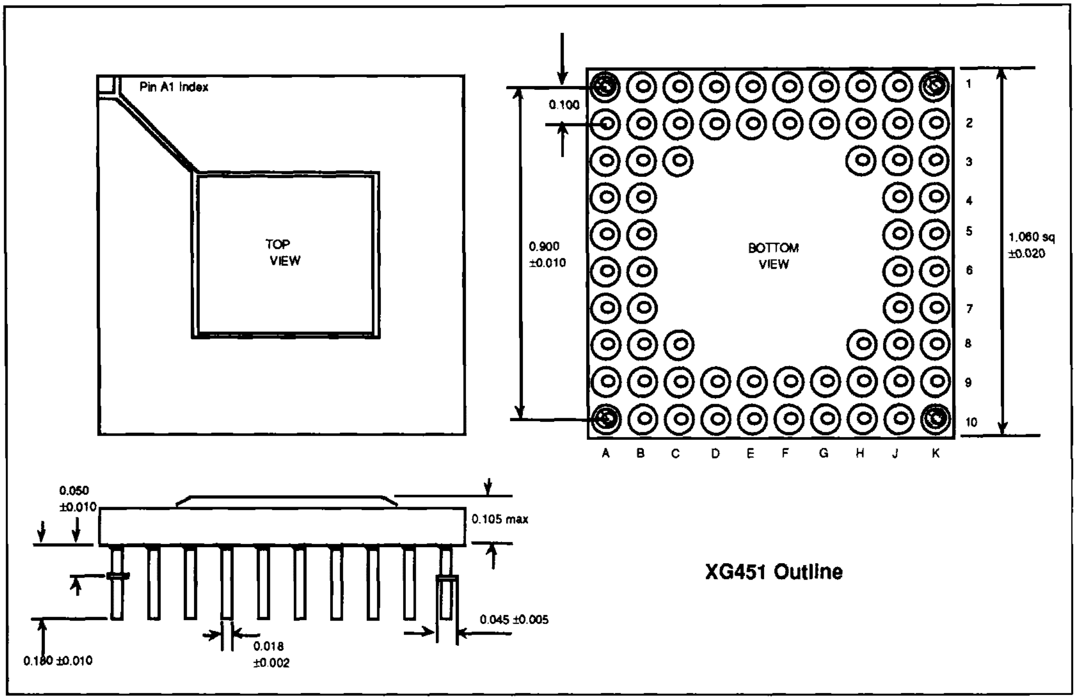


Figure 15: Dimensioned Drawing for the 68-pin PGA Package

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	CB05	C1	CB02	G9	CS0	K3	MD08
A2	NCERRN	C2	CB04	G10	PD00	K4	MD06
A3	RDWN	C3	VDD	H1	MD15	K5	VDD
A4	PD16	C8	VDD	H2	MD12	K6	NC
A5	PD14	C9	PD07	H3	VDD	K7	MD04
A6	VDD	C10	PD04	H8	VDD	K8	MD03
A7	PD13	D1	CB00	H9	ENFLG	K9	MD01
A8	PD11	D2	CB01	H10	CS1N	K10	ENCOR
A9	PD10	D9	PD05	J1	MD13		
A10	PD08	D10	PD03	J2	GND		
B1	CB03	E1	GND	J3	MD10		
B2	GND	E2	NC	J4	MD07		
B3	CERRN	E9	PD02	J5	GND		
B4	XERRN	E10	PD01	J6	MD05		
B5	PD15	F1	VDD	J7	MD02		
B6	GND	F2	NC	J8	MD00		
B7	PD12	F9	GND	J9	GND		
B8	PD09	F10	VDD	J10	CS2N		
B9	GND	G1	MD16	K1	MD11		
B10	PD06	G2	MD14	K2	MD09		

Figure 16: Pinout for the 68-pin PGA Package

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

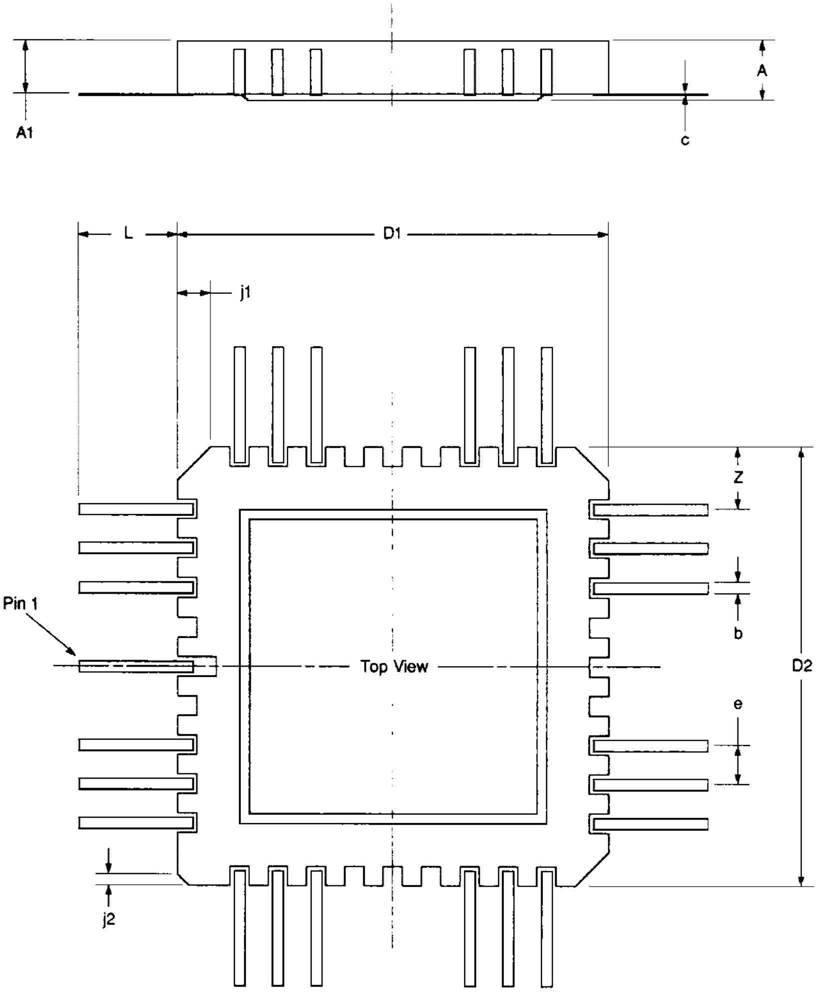


Figure 17: Dimensioned Drawing for the 68-pin Flatpack Package Topbraze

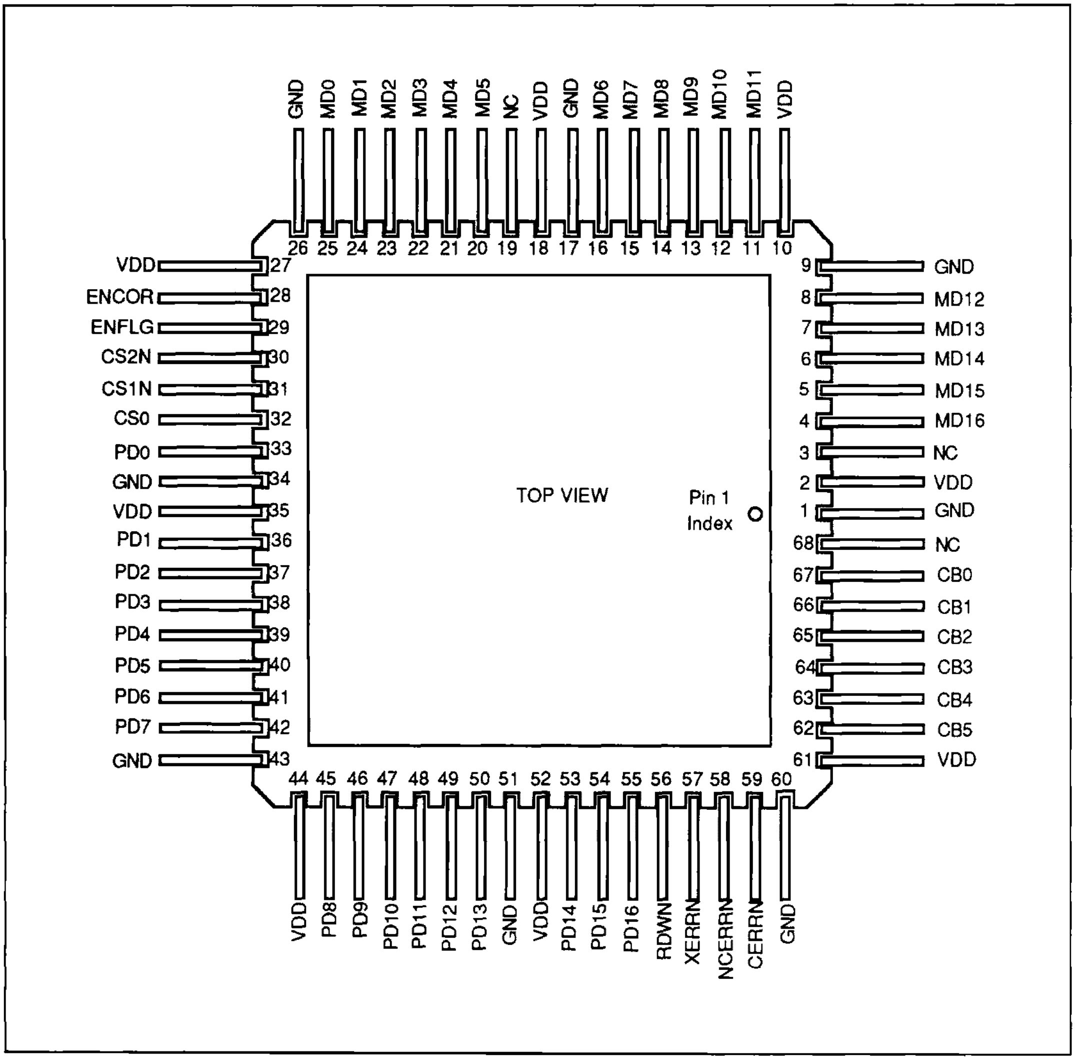


Figure 18: Pinout for the 68-pin Flatpack Package

8. RADIATION TOLERANCE

8.1 TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

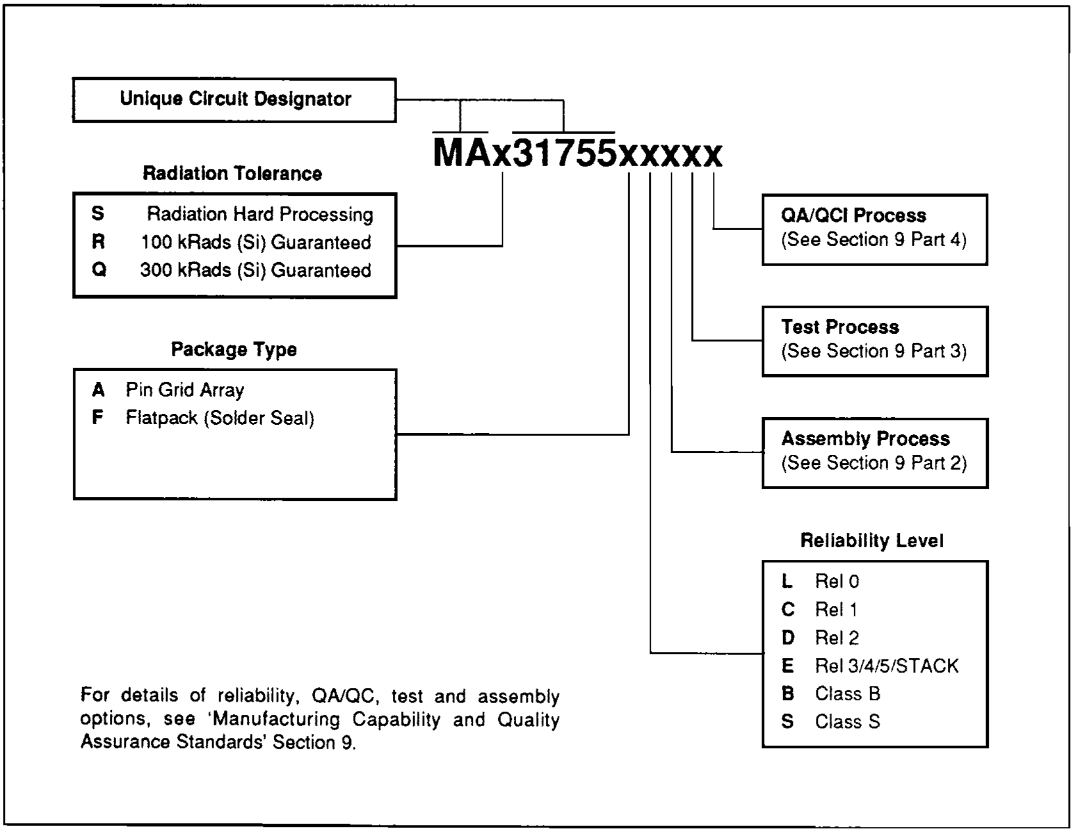
The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)	1x10^6 Rad(Si)
Transient Upset (Survivability)	>10^{11} Rad(Si)/sec
Neutron Hardness (Function to specification)	>10^{15} neutrons/cm^2
Latch-up	Not possible

Figure 19: Radiation Hardness Parameters

9. ORDERING INFORMATION



Unique Circuit Designator

MAx31755xxxxx

Radiation Tolerance

- **S** Radiation Hard Processing
- **R** 100 kRads (Si) Guaranteed
- **Q** 300 kRads (Si) Guaranteed

Package Type

- **A** Pin Grid Array
- **F** Flatpack (Solder Seal)

QA/QCI Process
(See Section 9 Part 4)

Test Process
(See Section 9 Part 3)

Assembly Process
(See Section 9 Part 2)

Reliability Level

- **L** Rel 0
- **C** Rel 1
- **D** Rel 2
- **E** Rel 3/4/5/STACK
- **B** Class B
- **S** Class S

For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.