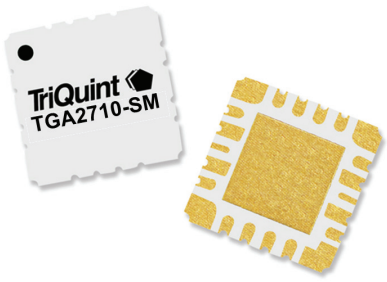
TGA2710-SM

8W 9.5-11.5 GHz Power Amplifier

Applications

- Marine and Air Radar, Traffic Control
- Weather Monitoring
- Port Security
- Point-to-Point Radio
- Communications

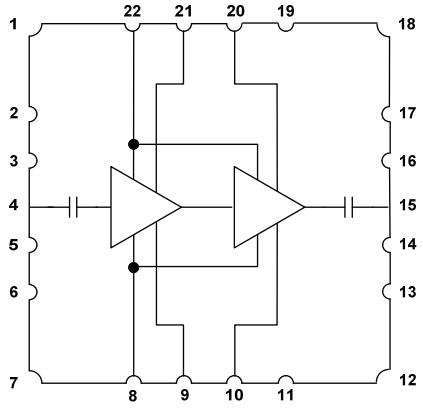


QFN 7x7mm 22L

Product Features

- Frequency Range: 9.5 - 11.5 GHz
- Saturated Output Power: 39 dBm
- Small Signal Gain: 22 dB
- Bias: Vd = 9 V, Idq = 1.05 A, Vg = -0.74 V typical

Functional Block Diagram



General Description

The TriQuint TGA2710-SM provides 22 dB of small signal gain and 8W of output power across 9.5-11.5 GHz. TGA2710-SM is designed using TriQuint's proven standard 0.25µm gate pHEMT 3MI production process.

The TGA2710-SM features a ceramic QFN designed for surface mount to a printed circuit board.

Fully matched to 50 ohms and with integrated DC blocking capacitors on both I/O ports, the TGA2710 -SM is ideally suited to support both commercial and defense related applications

Lead-free and RoHS compliant.

Evaluation Boards are available upon request.

Pin Configuration

Pin #	Symbol
1,2,3,5,6,7,11,12,13,14, 16,17,18,19	Gnd
4	RF In
8	Vg
9	Vd1
10	Vd2
15	RF Out
20	Vd2
21	Vd1
22	Vg

Ordering Information

Part No.	ECCN	Description
TGA2710-SM	3A001.b.2.b	X-band Power Amplifier

Specifications

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, Vd	10 V
Gate Voltage, Vg	-1.2 to 0.5 V
Drain Current, Id	3.85 A
Gate Current range, Ig	-14 to 126 mA
RF Input Power, CW, 50Ω,T = 25ºC	23 dBm
Channel Temperature, Tch	200 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vd		9		V
Idq (no RF drive)		1.05		A
Id_drive (under RF drive)		2.05		A
Vg		-0.74		V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions

Electrical Specifications

Test conditions unless otherwise noted: 25ºC, Vd = 9 V, Idq = 1.05 A, Vg = -0.74 V typical, CW

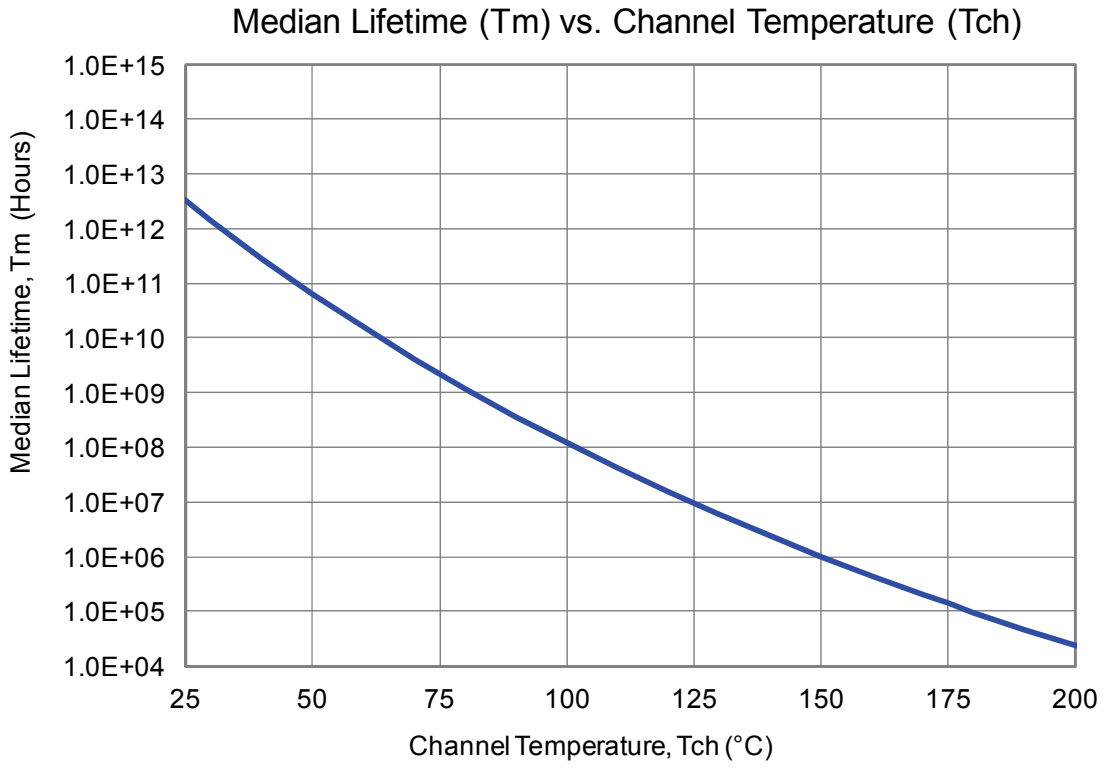
Parameter	Min	Typ	Max	Units
Operational Frequency Range	9.5		11.5	GHz
Small Signal Gain		22		dB
Small Signal Gain Temperature Coefficient		-0.055		dB/ºC
Output Power @ Saturation		39		dBm
Power-Added Efficiency @ Saturation		44		
Output Power @ 1 dB compression		38		dBm
Output Power Temperature Coefficient		-0.013		dB/ºC

Specifications (cont'd)

Thermal and Reliability Information

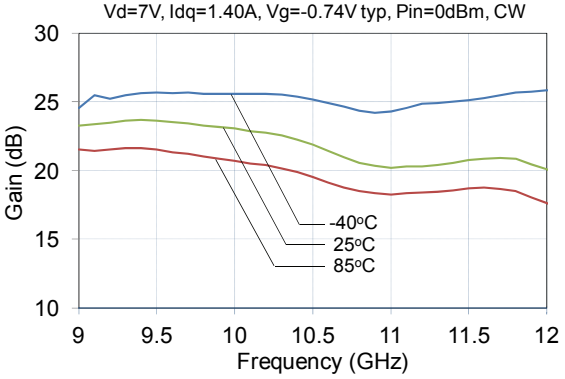
Parameter	Condition	Rating
Channel Temperature (Tch), Median Lifetime (Tm), Thermal Resistance*	Tbase = 85 °C, Vd = 7V, Idq = 1.40 A, Pdiss = 9.8 W, no RF input power, CW	Tch = 161°C Tm = 4.1E+5 Hours θJC = 7.8°C/W
Channel Temperature (Tch), Median Lifetime (Tm), Thermal Resistance*	Tbase = 85 °C, Vd = 7V, Id = 2.02 A, Pdiss = 8.4 W, Pout = 37.6 dBm, CW	Tch = 139°C Tm = 2.6E+6 Hours θJC = 6.4°C/W
Channel Temperature (Tch), Median Lifetime (Tm), Thermal Resistance*	Tbase = 85 °C, Vd = 9V, Idq = 1.05 A, Pdiss = 9.5 W, no RF input power, CW	Tch = 156 °C Tm = 6.1E+5 Hours θJC = 7.5°C/W
Channel Temperature (Tch), Median Lifetime (Tm), Thermal Resistance*	Tbase = 85 °C, Vd = 9V, Id = 2.24 A, Pdiss = 12.4 W, Pout = 38.9 dBm, CW	Tch = 168°C Tm = 2.3E+5 Hours θJC = 6.7°C/W

* Thermal Resistance, θJC, measured to center bottom of package

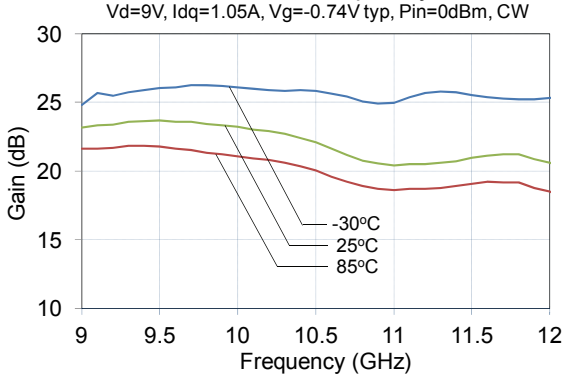


Typical Performance

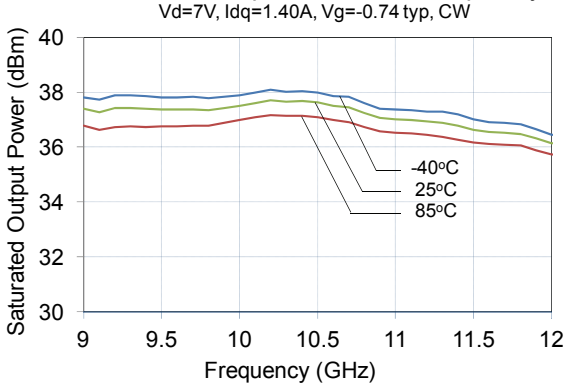
Gain vs. Frequency
Vd=7V, Idq=1.40A, Vg=-0.74V typ, Pin=0dBm, CW



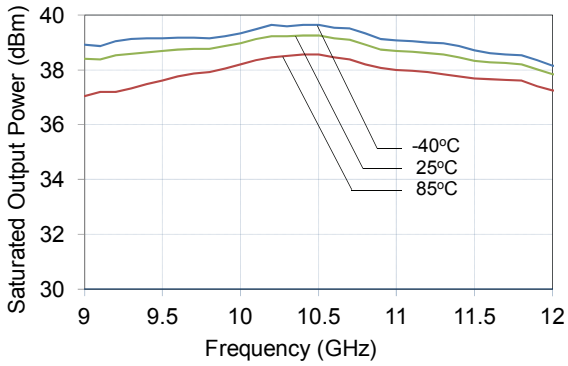
Gain vs. Frequency
Vd=9V, Idq=1.05A, Vg=-0.74V typ, Pin=0dBm, CW



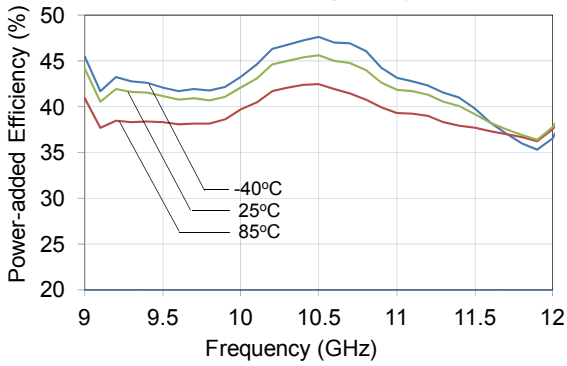
Saturated Output Power vs. Frequency
Vd=7V, Idq=1.40A, Vg=-0.74 typ, CW



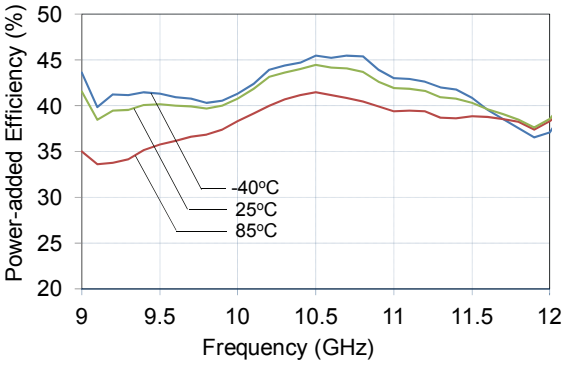
Saturated Output Power vs. Frequency
Vd=9V, Idq=1.05A, Vg=-0.74 typ, CW



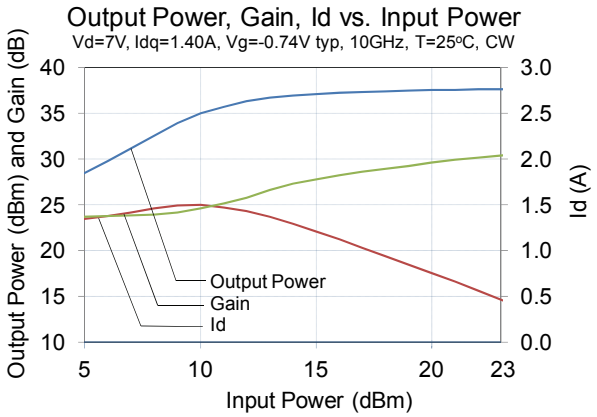
Power-added efficiency vs. Frequency
Vd=7V, Idq=1.40A, Vg=-0.74 typ, CW

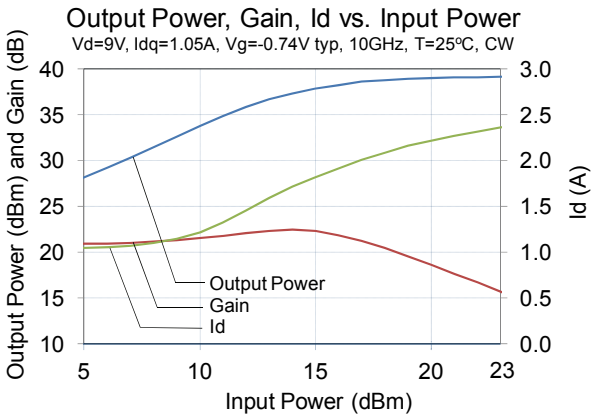


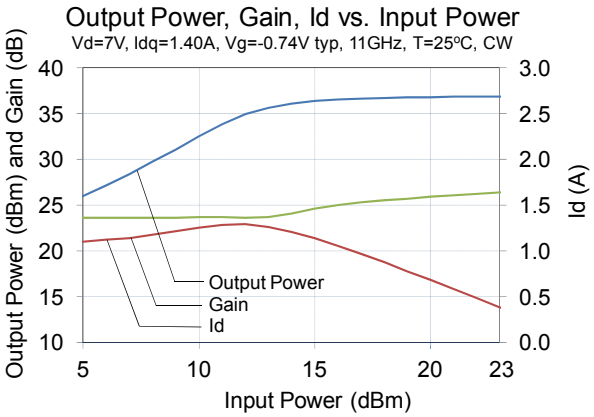
Power-added efficiency vs. Frequency
Vd=9V, Idq=1.05A, Vg=-0.74 typ, CW

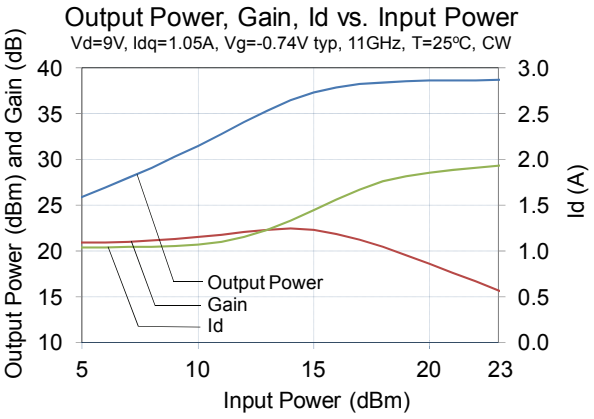


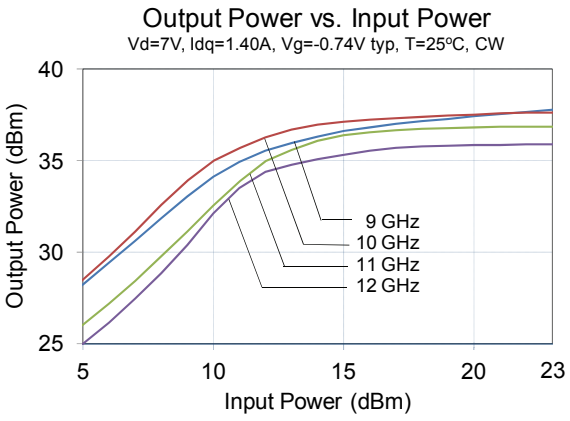
Typical Performance

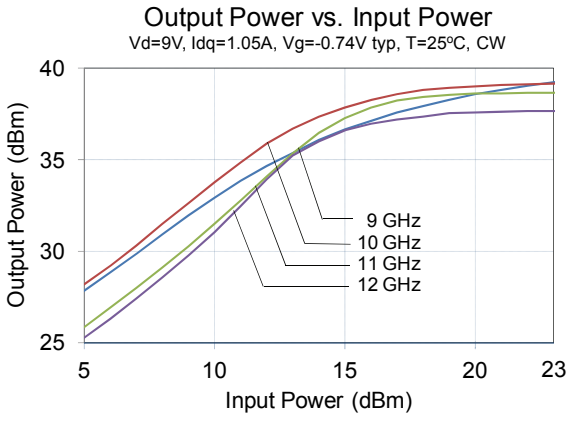




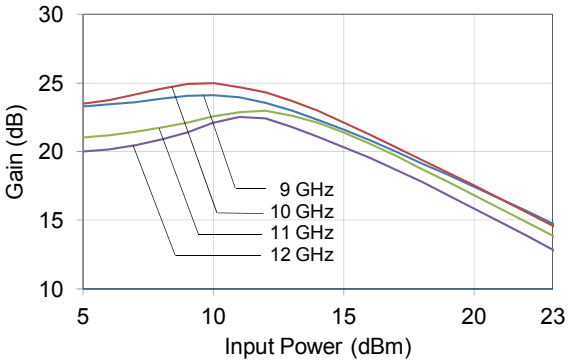




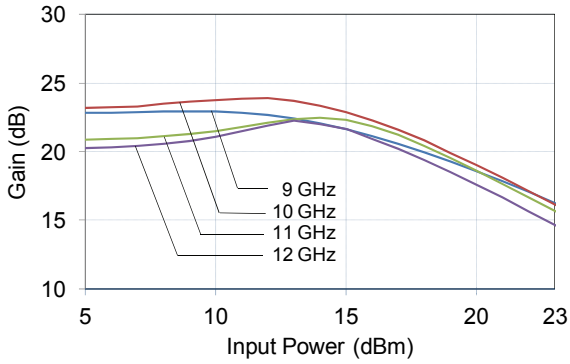




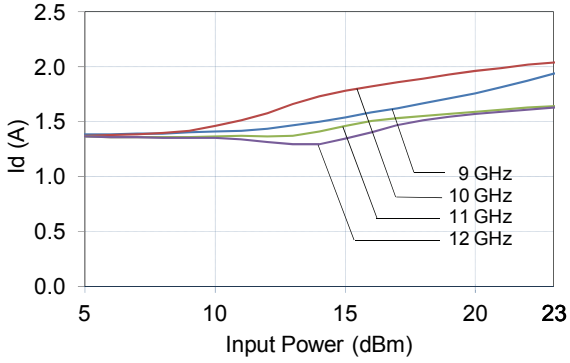
Gain vs. Input Power
Vd=7V, Idq=1.40A, Vg=-0.74V typ, T=25°C, CW



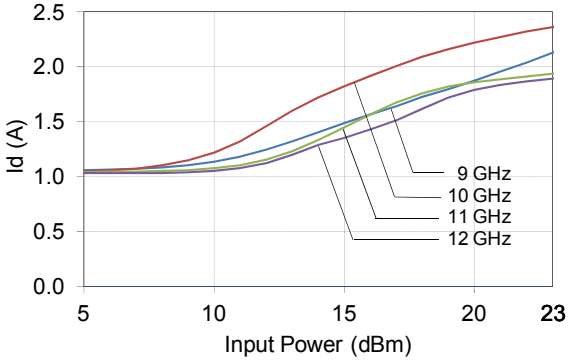
Gain vs. Input Power
Vd=9V, Idq=1.05A, Vg=-0.74V typ, T=25°C, CW



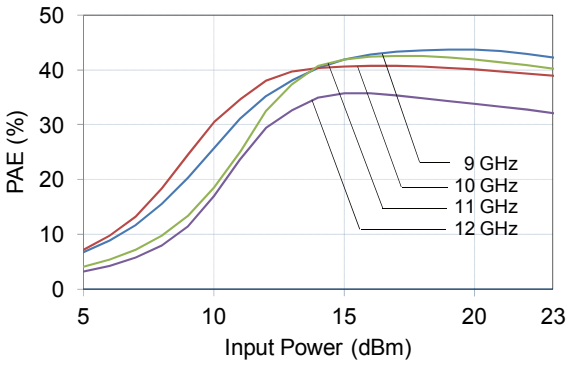
Id vs. Input Power
Vd=7V, Idq=1.40A, Vg=-0.74V typ, T=25°C, CW



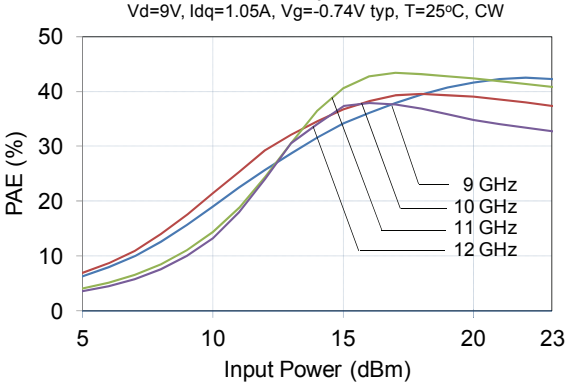
Id vs. Input Power
Vd=9V, Idq=1.05A, Vg=-0.74V typ, T=25°C, CW



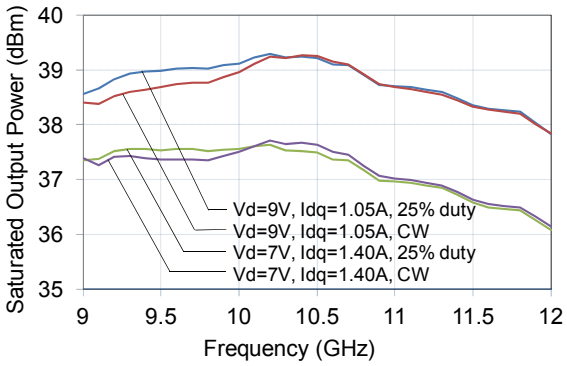
PAE vs. Input Power
Vd=7V, Idq=1.40A, Vg=-0.74V typ, T=25°C, CW



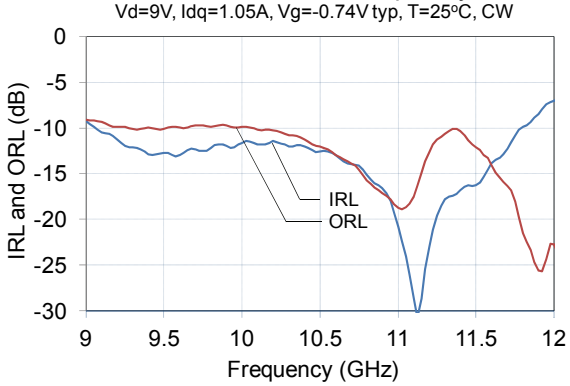
PAE vs. Input Power
Vd=9V, Idq=1.05A, Vg=-0.74V typ, T=25°C, CW



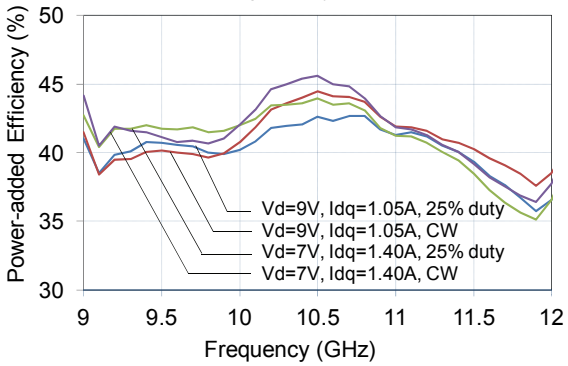
Saturated Output Power vs. Frequency
Vg=-0.74 typ, 25C



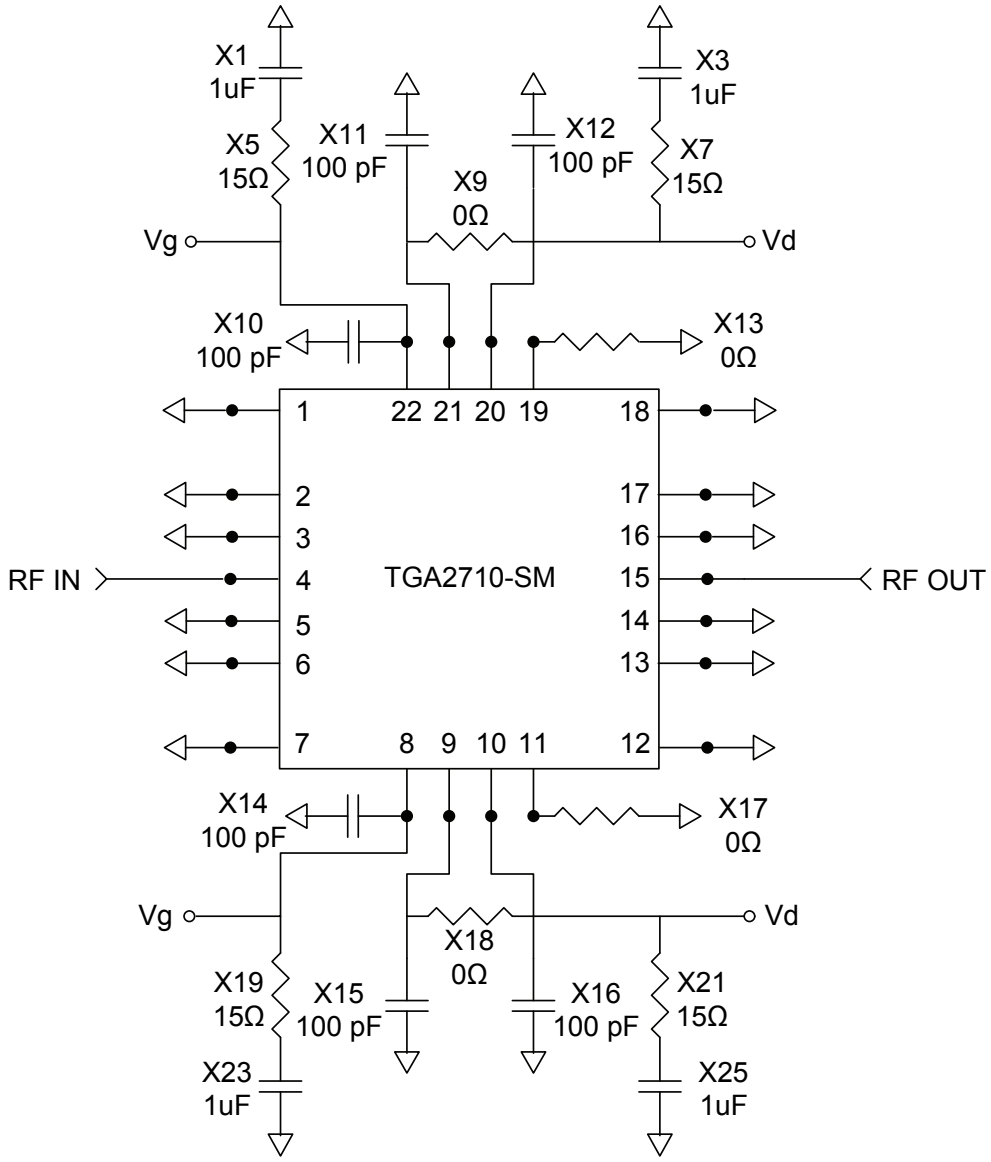
Return Loss vs. Frequency
Vd=9V, Idq=1.05A, Vg=-0.74V typ, T=25ºC, CW



Power-added efficiency vs. Frequency
Vg=-0.74 typ, CW

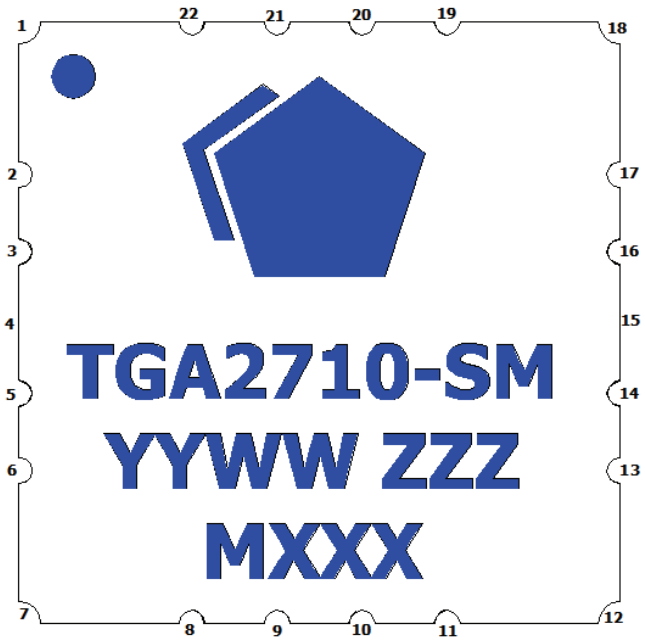


Application Circuit



Bias-up Procedure	Bias-down Procedure
Turn Vg to –1.2 V	Turn off RF signal
Turn Vd to 9 V	Reduce Vg to –1.2 V. Ensure Id ~ 0 mA
Adjust Vg more positive until Idq is 1.05 A. This will be Vg ~ -0.74 V typical	Turn Vd to 0 V
Apply RF signal	Turn Vg to 0 V

Pin Description



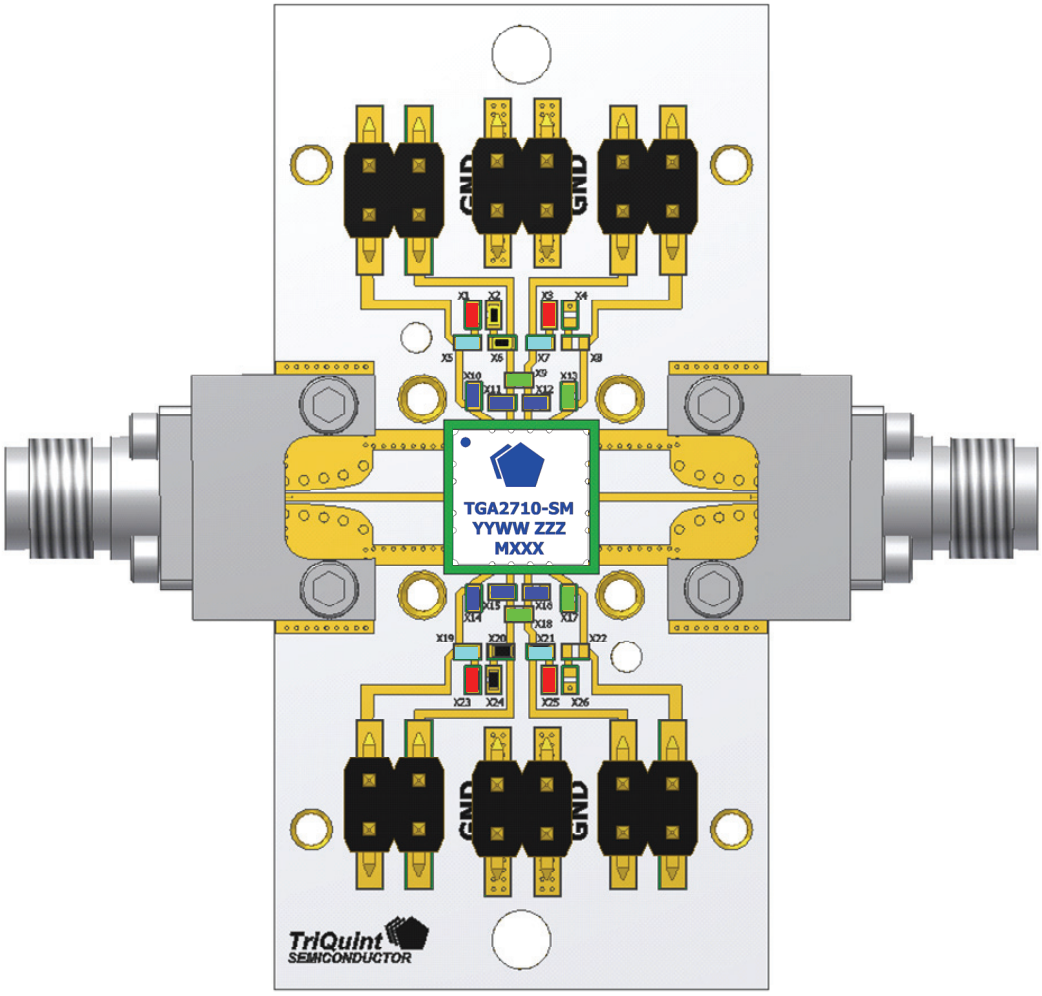
Pin #	Symbol	Description
1,2,3,5,6,7,11,12,13, 14,16,17,18,19	Gnd	Connect to Ground
4	RF In	Input, matched to 50Ω
8	Vg	Gate voltage. Bias network is required
9	Vd1	Drain 1 voltage. Bias network is required
10	Vd2	Drain 2 voltage. Bias network is required
15	RF Out	Output, matched to 50Ω
20	Vd2	Drain 2 voltage. Bias network is required
21	Vd1	Drain 1 voltage. Bias network is required
22	Vg	Gate voltage. Bias network is required

Note: See Application Circuit on page 6 as an example

Evaluation Board Layout

PC Board Layout

Board material is RO4003 0.008" thickness with ½ oz copper cladding.



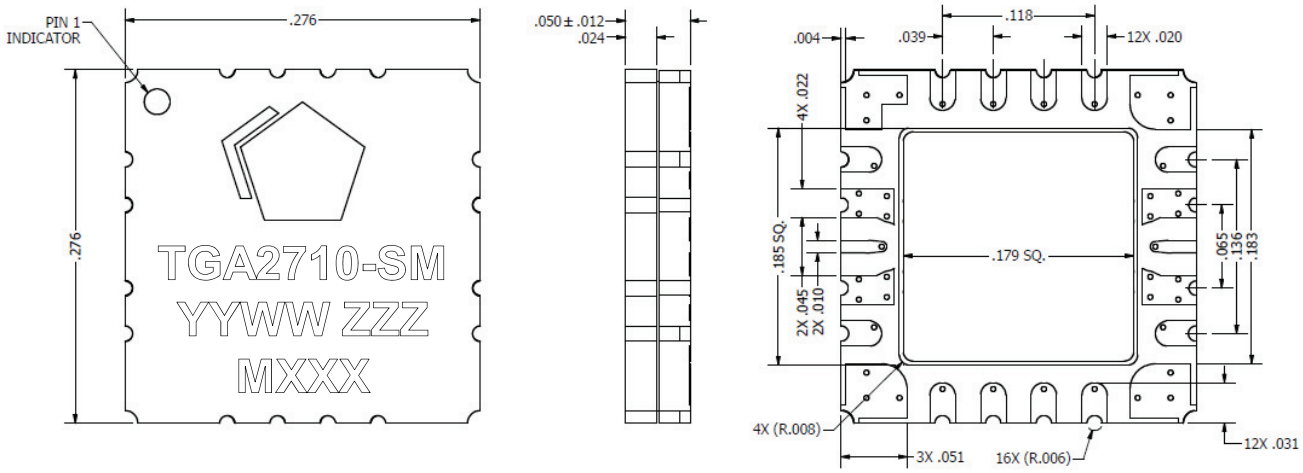
Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
X1,X3,X23, X25	1 uF	Cap, 0402	TDK	C1005XR1C105M
X10,X11, X12,X14, X15,X16	100 pF	Cap, 0402	AVX	04025C101KAT2A
X5,X7,X19, X21	15Ω	Resistor, 0402	Panasonic	ERJ-2GEJ150X
X9,X13,X17, X18	0Ω	Resistor, 0402	Panasonic	ERJ-2GE0R00X

Mechanical Information

Package Information and Dimensions

All dimensions in inches and are +/- 0.006in unless otherwise noted.

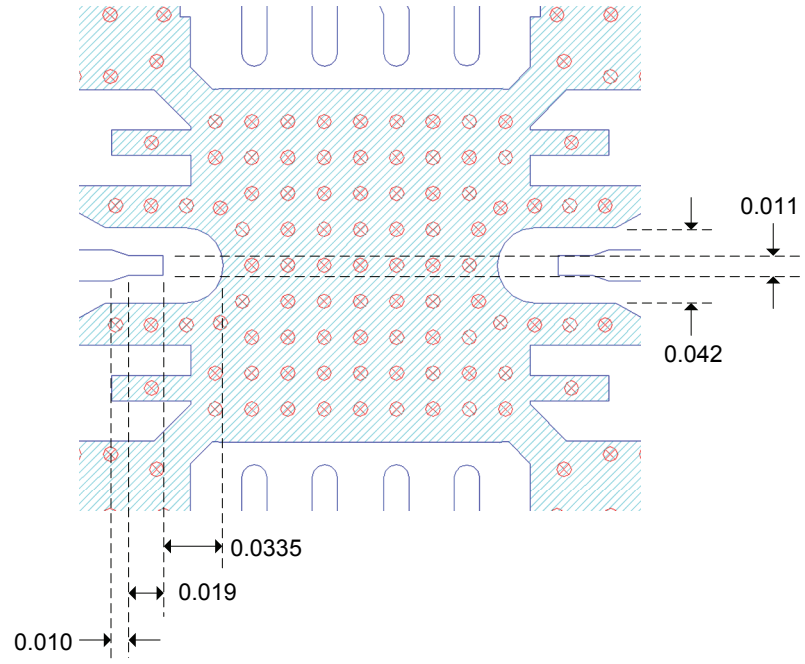


Part marking:

YY	assembly lot start year
WW	assembly lot start week
ZZZ	part serial number
MXXX	batch ID

PCB Mounting Pattern

All dimensions in inches



Notes:

1. The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008in diameter drill, and they are solid filled, copper plated shut or silver filled paste with over plating.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD rating:	TBD
Value:	Passes < TBD V min.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

Solderability

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

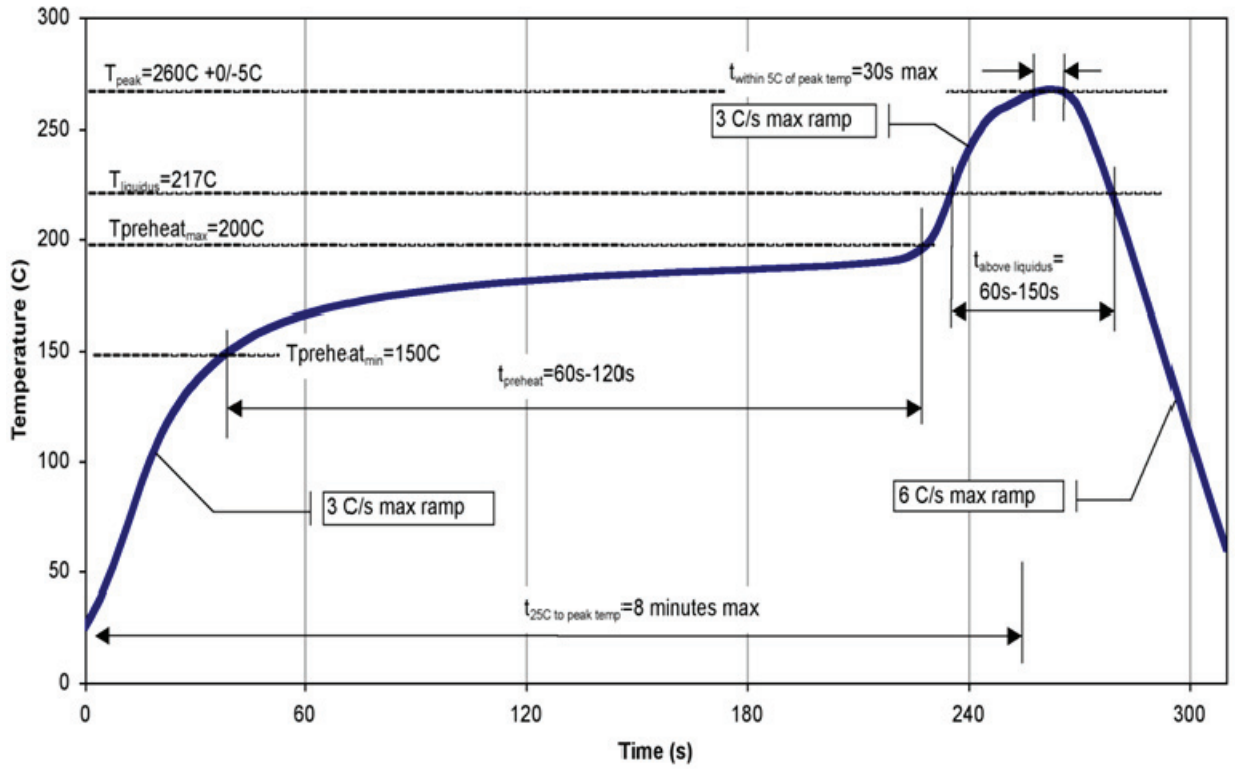
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free

ECCN

US Department of Commerce: 3A001.b.2.b

Recommended Soldering Temperature Profile



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.972.994.8465
Email: info-products@tqs.com **Fax:** +1.972.994.8504

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